SmartFusion2 Pin Descriptions

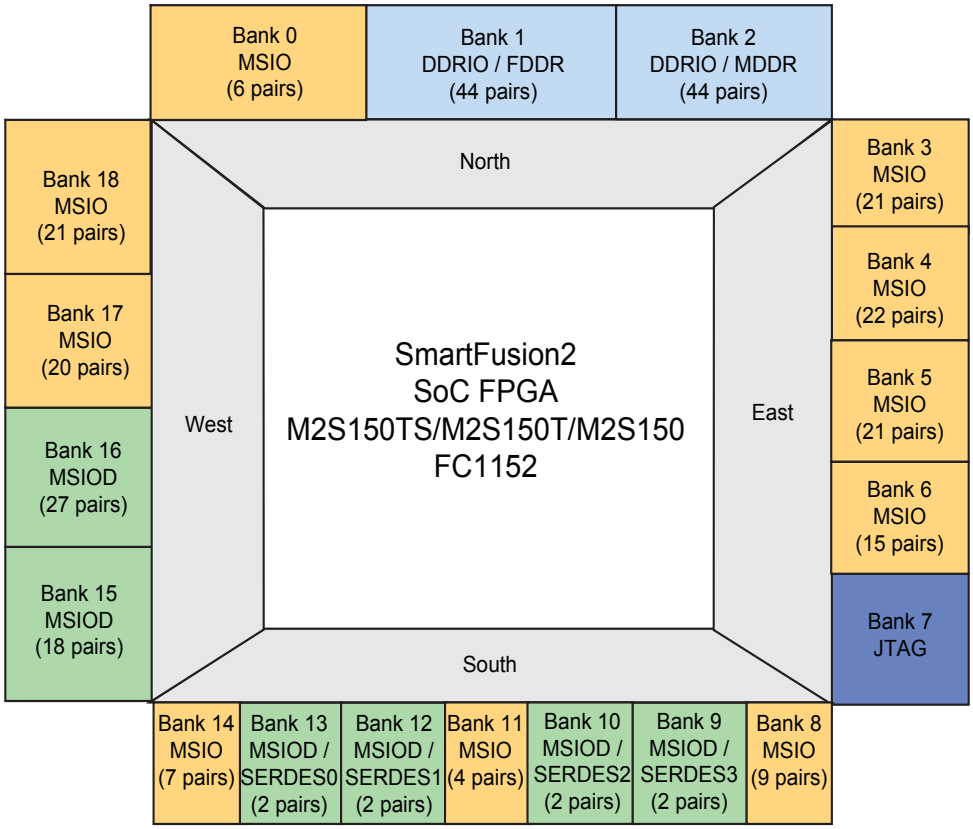
User I/Os

SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) devices feature a flexible I/O structure that supports a range of mixed voltages (1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V) through bank selection. The MSIO, MSIOD, and DDRIO can be configured as differential I/Os or two single-ended I/Os. These I/Os use one I/O slot to implement single-ended standards and two I/O slots for differential standards. The DDRIO is shared between fabric logic and MDDR/FDDR whereas MSIO/MSIOD is shared between MSS peripherals and fabric logic. When an MDDR/FDDR controller or MSS peripheral is not used, the respective I/Os are available to fabric logic.

For functional block diagrams of MSIO, MSIOD, and DDRIO, refer to the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide*.
For supported I/O standards, refer to the "Supported Voltage Standards" table in the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide.*

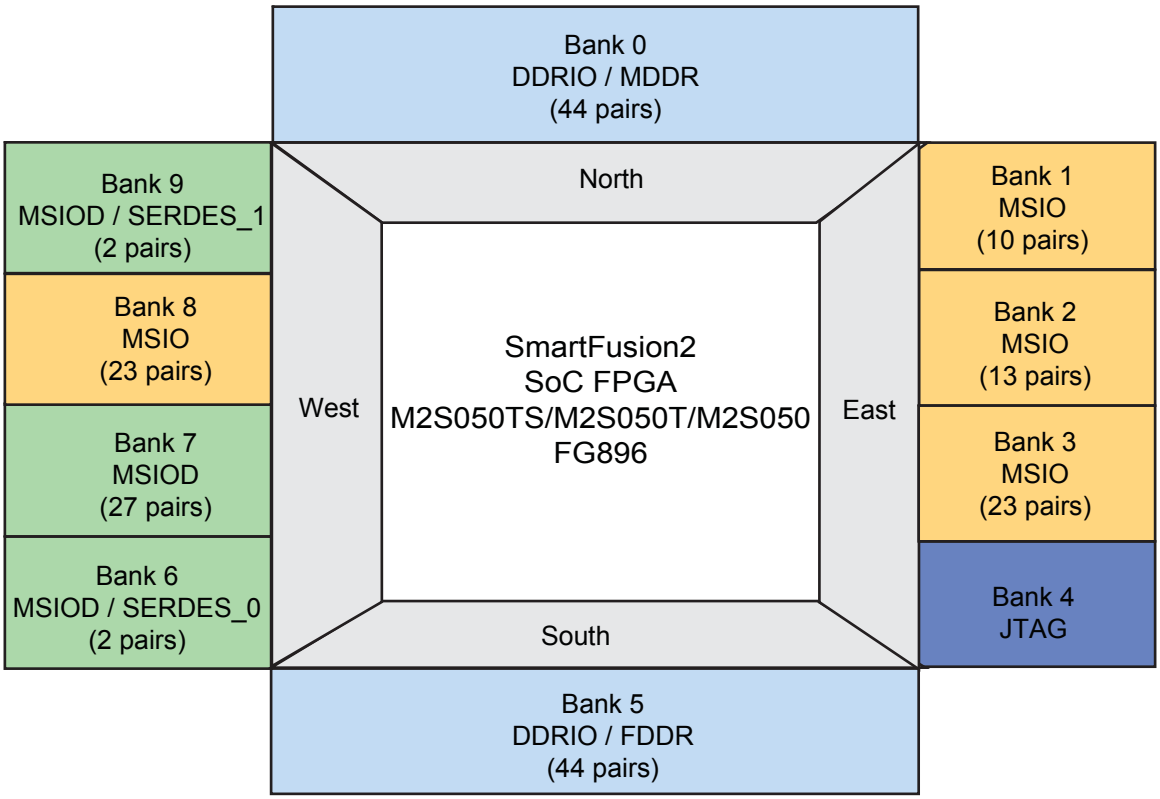
Bank Location Diagrams

I/Os are grouped on the basis of I/O voltage standard. The grouped I/Os of each voltage standard form an I/O bank. Each I/O bank has dedicated I/O supply and ground voltages. Because of these dedicated supplies, only I/Os with compatible standards can be assigned to the same I/O voltage bank.



Note: For M2S150-FC1152 device, SERDES blocks are not available in bank 9, 10, 12, and 13.

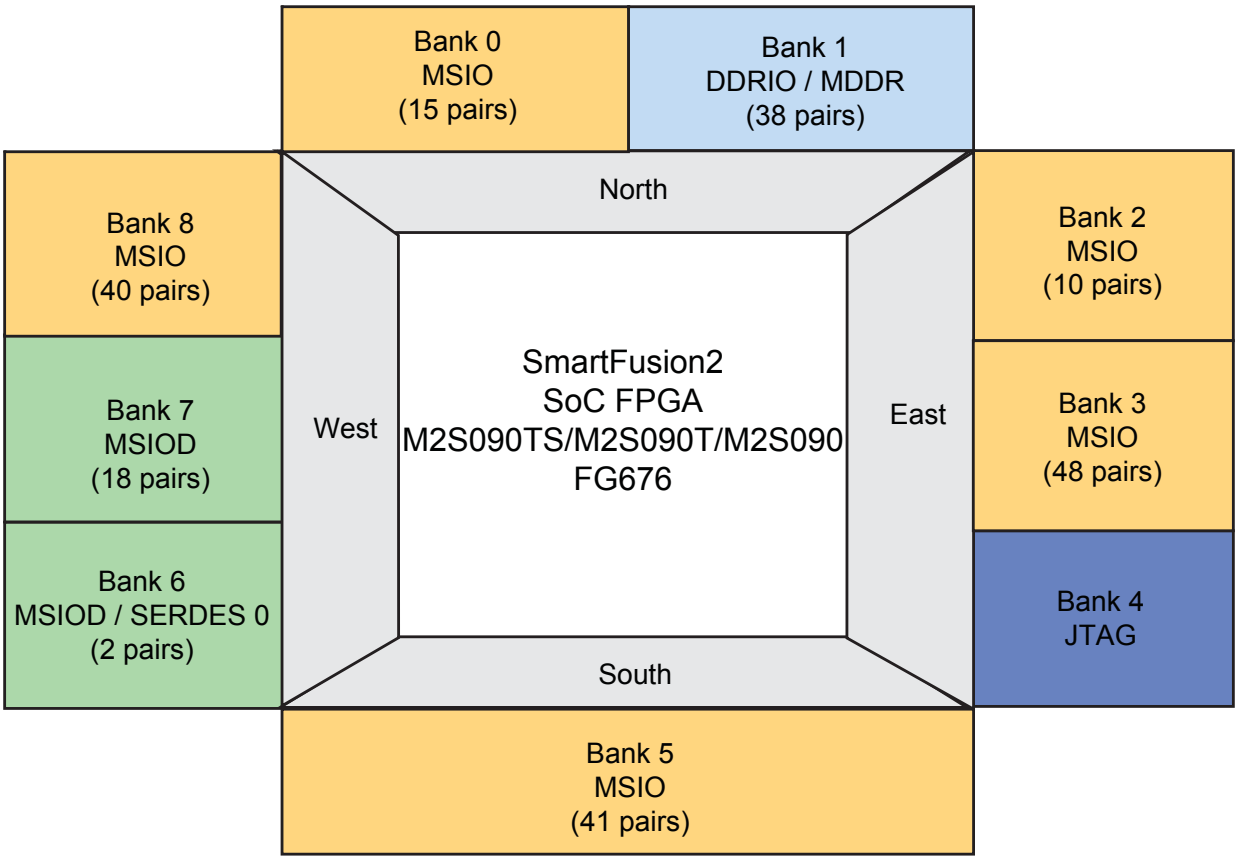
***Figure 1* • SmartFusion2 M2S150TS/M2S150T/M2S150-FC1152 I/O Bank Locations**



Notes:

1. *In bank 1, there are 21 single-ended user I/Os. Pin H27, MSI46NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI46NB1 is an input only pin.*
2. *For M2S050-FG896 device, SERDES blocks are not available in bank 6 and bank 9.*

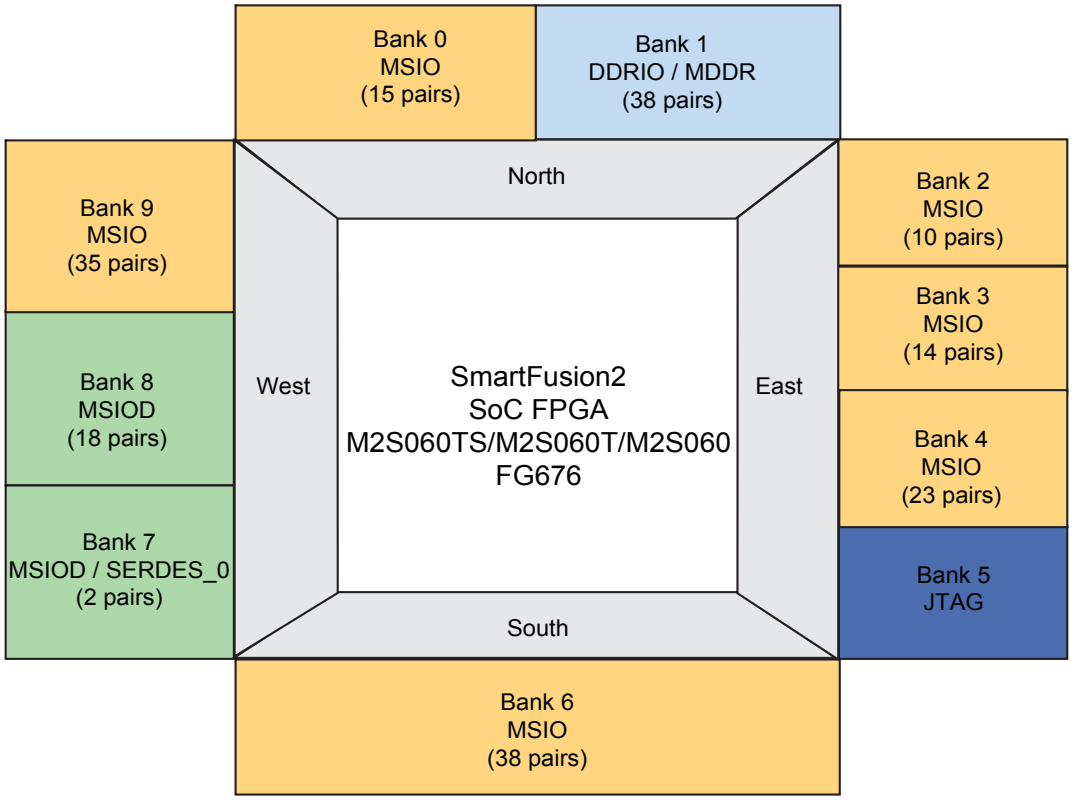
***Figure 2* • SmartFusion2 M2S050TS/M2S050T/M2S050-FG896 I/O Bank Locations**



Notes:

1. *In bank 2, there are 21 single-ended user I/Os. Pin D23, MSI59NB2/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI59NB2 is an input only pin.*
2. *For M2S090-FG676 device, the SERDES block is not available in bank 6.*

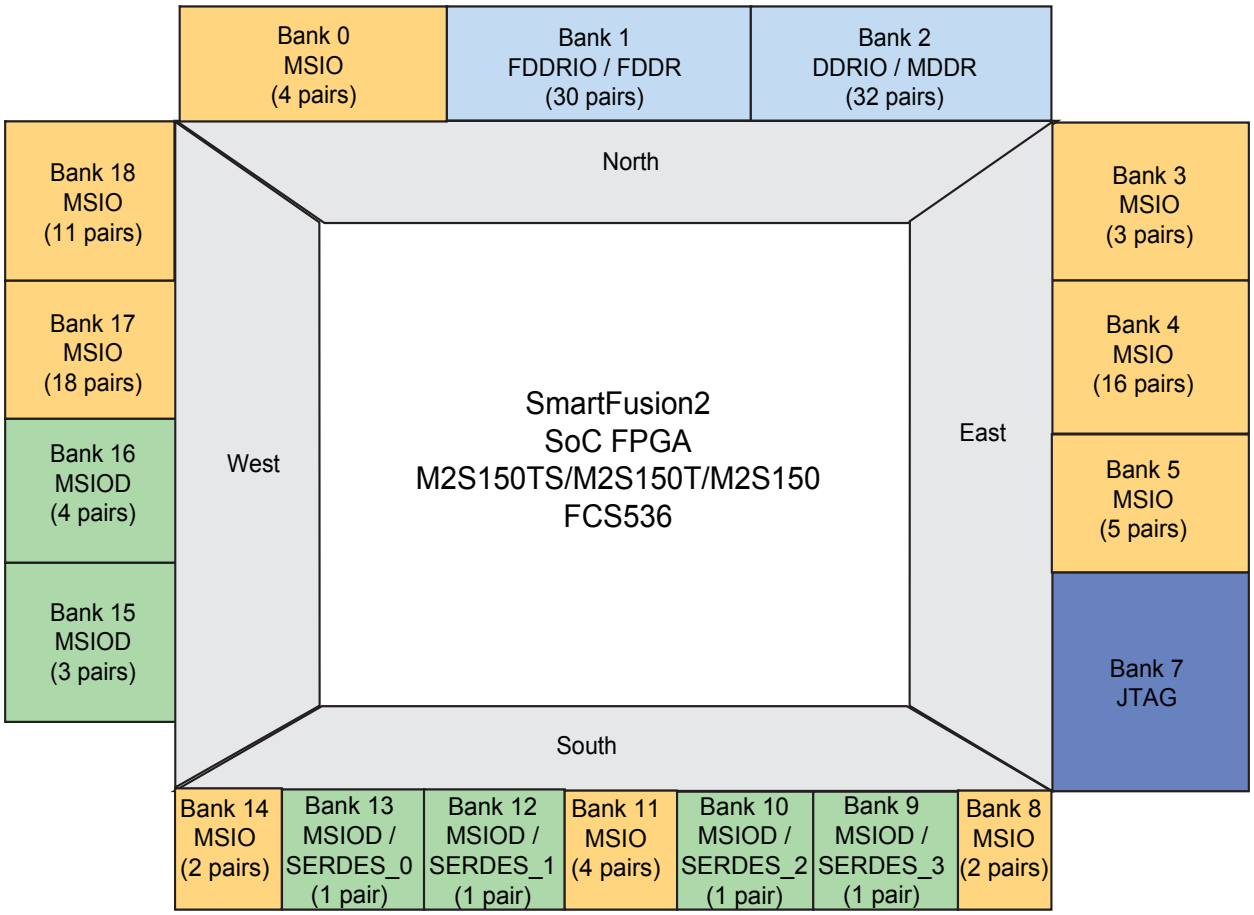
***Figure 3* • SmartFusion2 M2S090TS/M2S090T/M2S090-FG676 I/O Bank Locations**



Notes:

1. *For the M2S060-FG676 device, SERDES block is not available in bank7.*

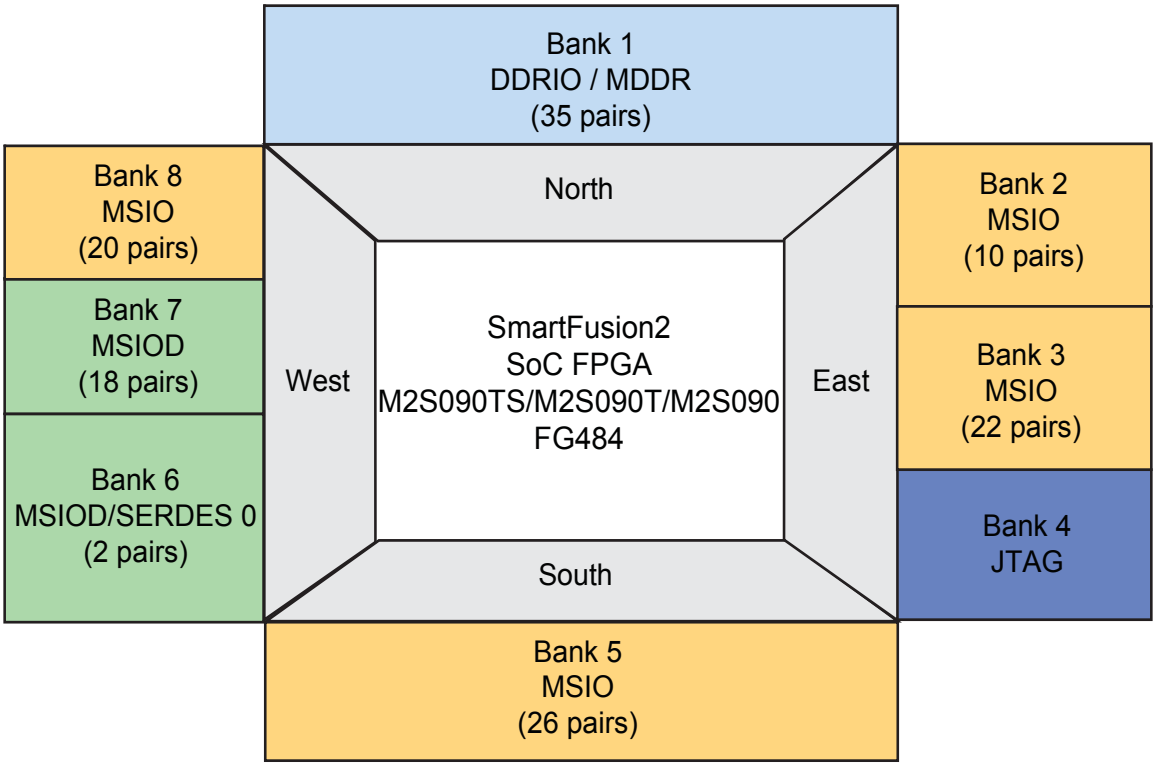
***Figure 4* • SmartFusion2 M2S060TS/ M2S060T/M2S060-FG676 I/O Bank Locations**



Notes:

1. *For the M2S150-FCS536 device, SERDES interface is not available in bank 9, 10,12, and 13.*

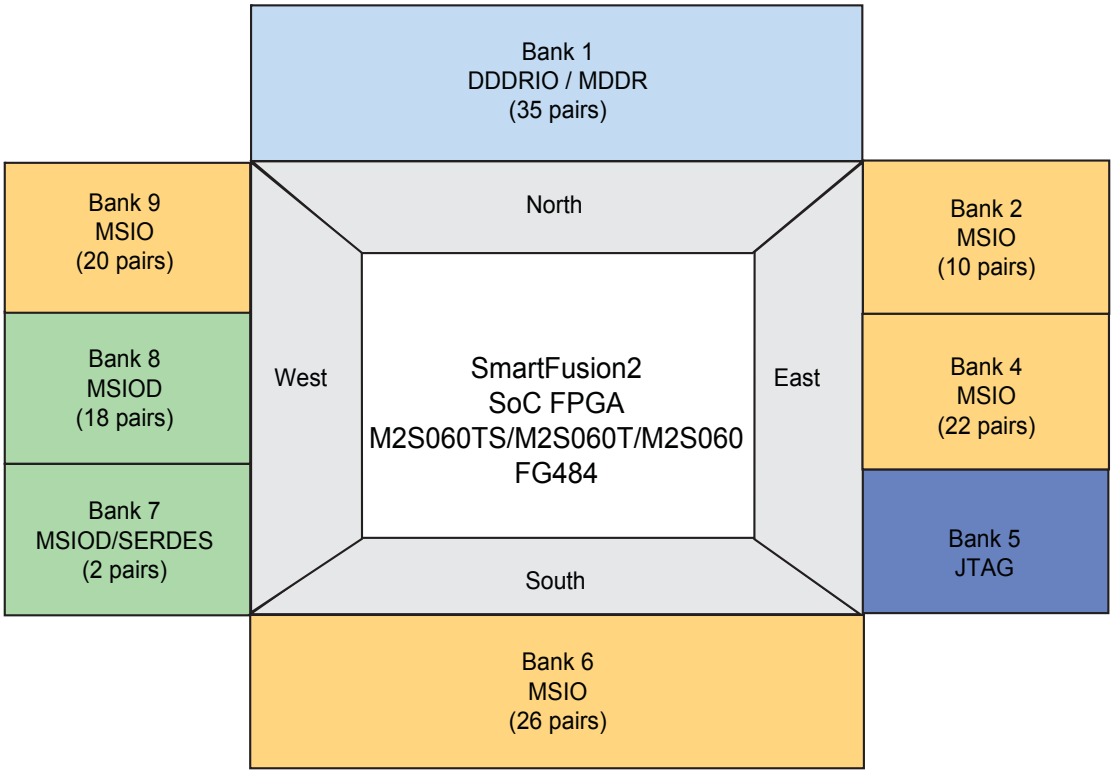
***Figure 5* • SmartFusion2 M2S150TS/M2S150T/M2S150-FCS536 I/O Bank Locations**



Notes:

1. *In bank 2, there are 21 single-ended user I/Os. Pin D21, MSI59NB2/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI59NB2 is an input only pin.*
2. *For M2S090-FG484 device, SERDES block is not available in bank 6.*

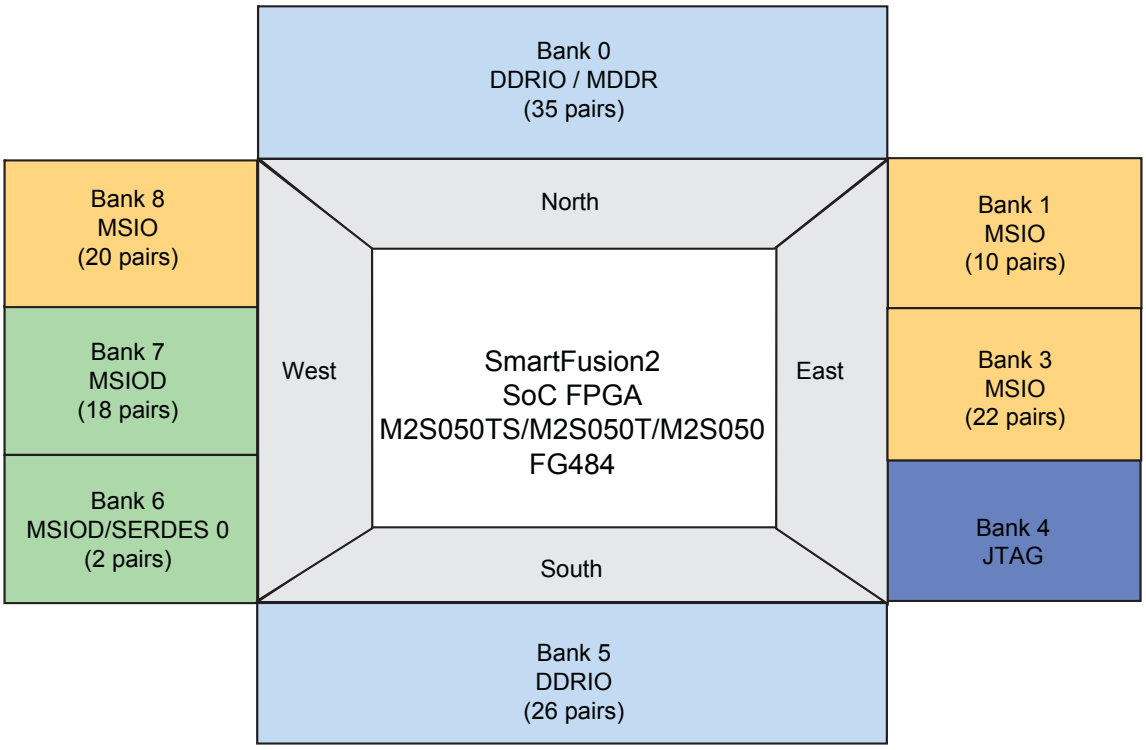
***Figure 6* • SmartFusion2 M2S090TS/M2S090T/M2S090-FG484 I/O Bank Locations**



Notes:

1. *For the M2S060S-FG484 and M2S060-FG484 devices, SERDES block is not available in bank 7.*
2. *In bank 2, there are 21 single-ended user I/Os. Pin D21, MSI47NB2/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI47NB2 is an input only pin.*

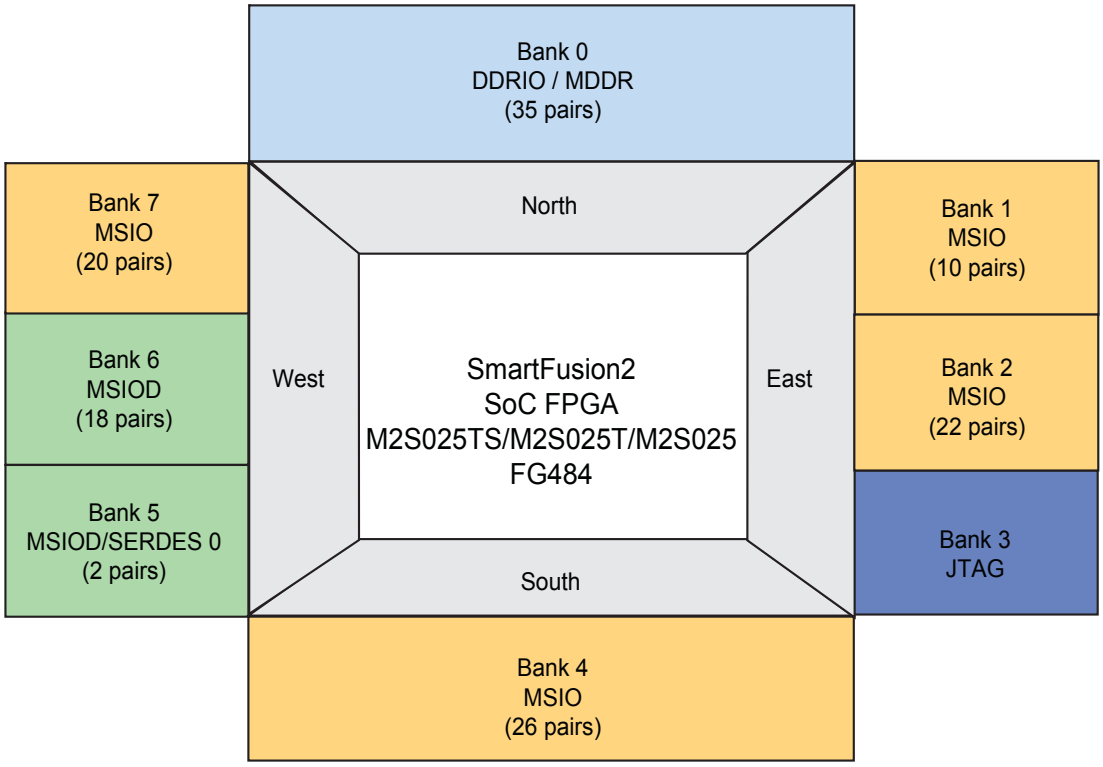
***Figure 7* • SmartFusion2 M2S060TS/M2S060T/M2S060-FG484 I/O Bank Locations**



Notes:

1. *In bank 1, there are 21 single-ended user I/Os. Pin D21, MSI46NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI46NB1 is an input only pin.*
2. *For M2S050-FG484 device, SERDES block is not available in bank 6.*

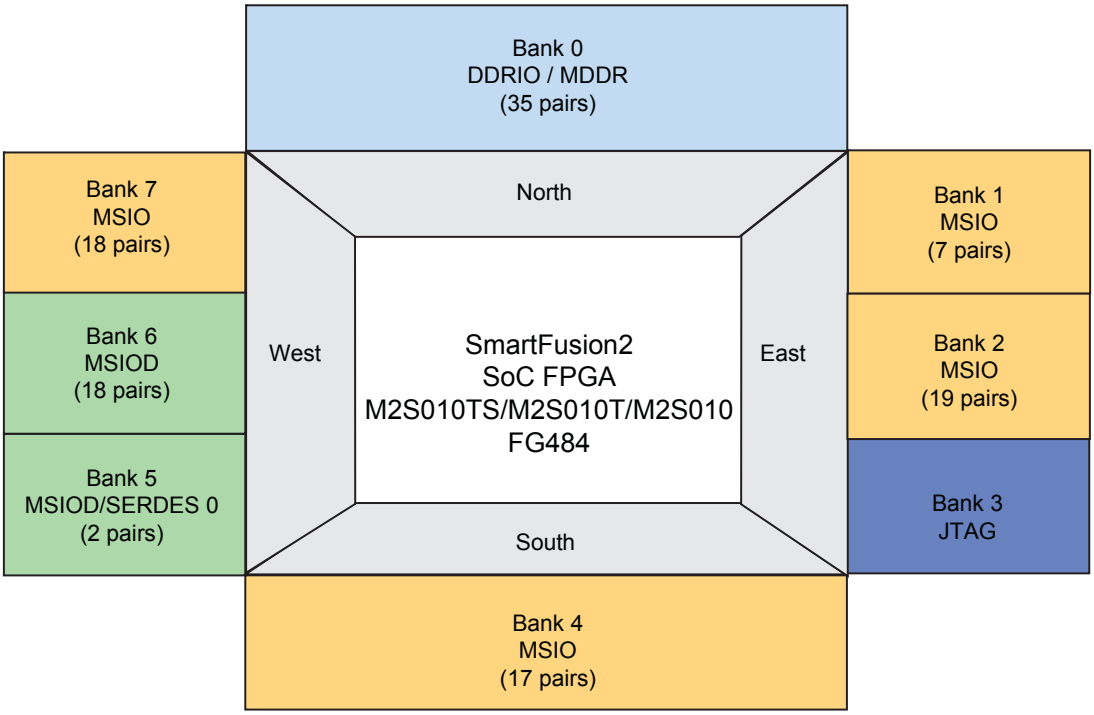
***Figure 8* • SmartFusion2 M2S050TS/M2S050T/M2S050-FG484 I/O Bank Locations**



Notes:

1. *In bank 1, there are 21 single-ended user I/Os. Pin D21, MSI32NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI32NB1 is an input only pin.*
2. *For M2S025-FG484 device, SERDES block is not available in bank 5.*

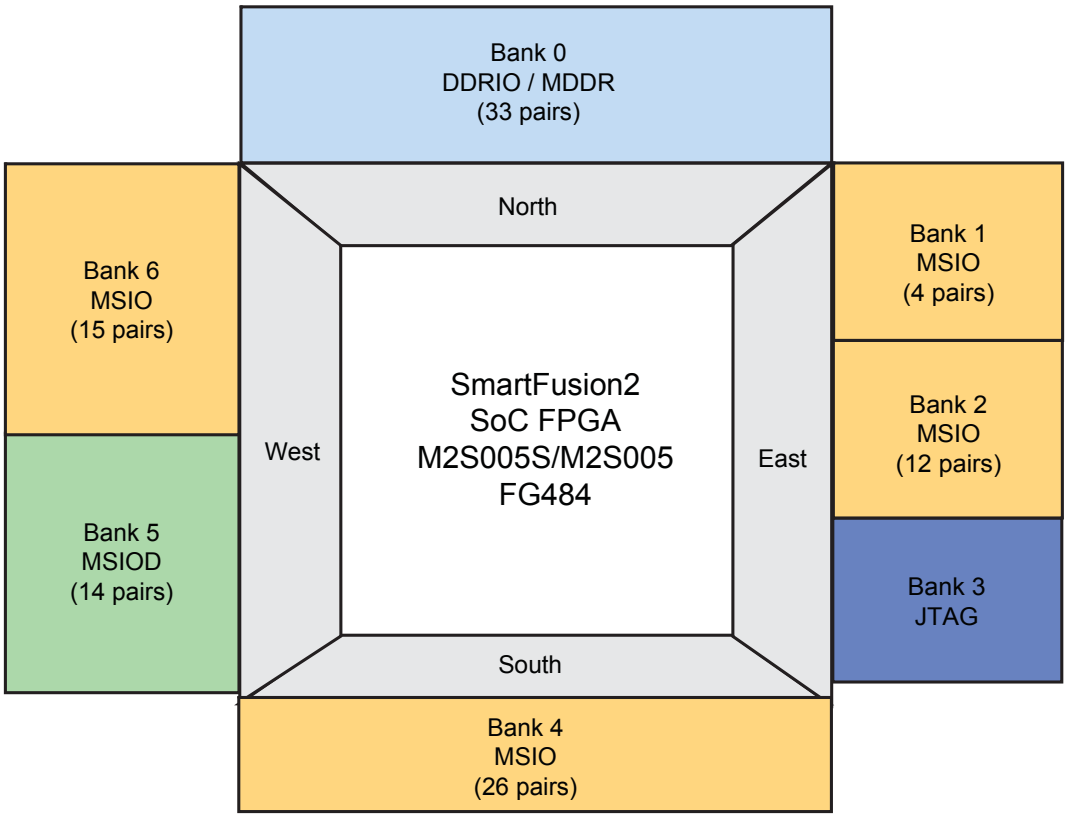
***Figure 9* • SmartFusion2 M2S025TS/M2S025T/M2S025-FG484 I/O Bank Locations**



Notes:

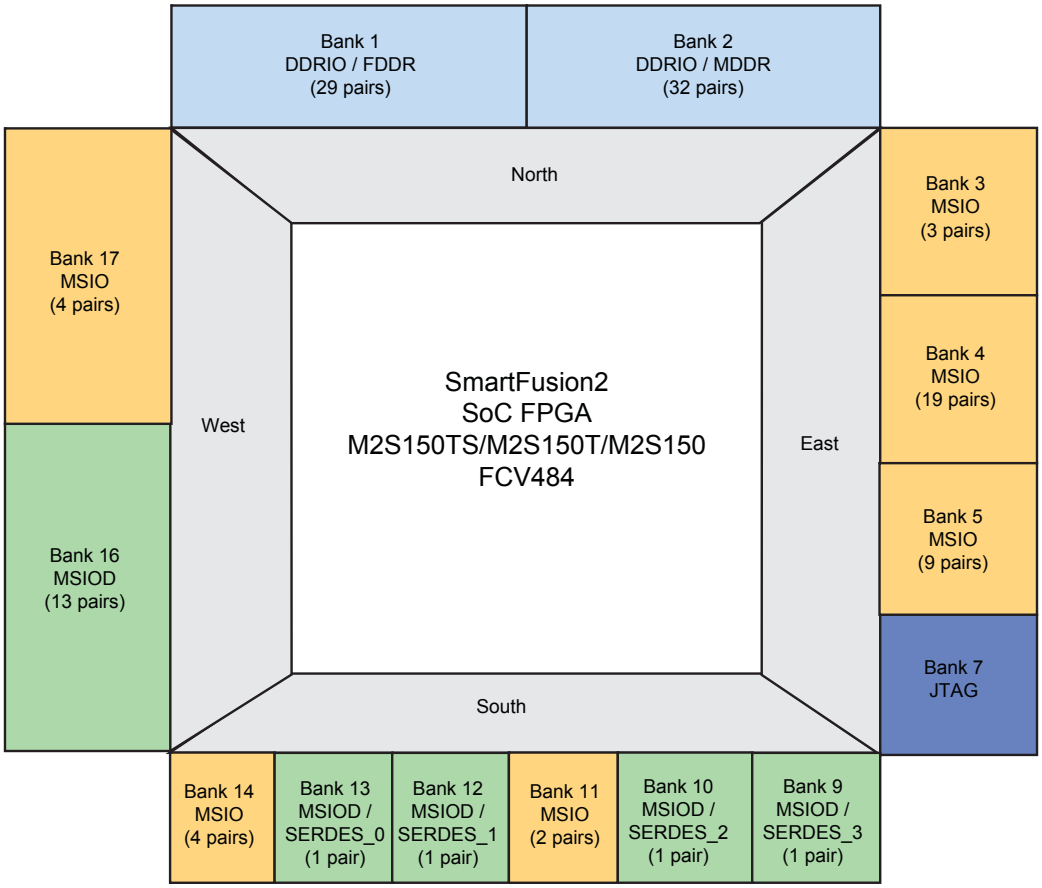
1. *In bank 1, there are 15 single-ended user I/Os. Pin D21, MSI26NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI32NB1 is an input only pin.*
2. *For M2S010-FG484 device, SERDES block is not available in bank 5.*

***Figure 10* • SmartFusion2 M2S010TS/M2S010T/M2S010-FG484 I/O Bank Locations**



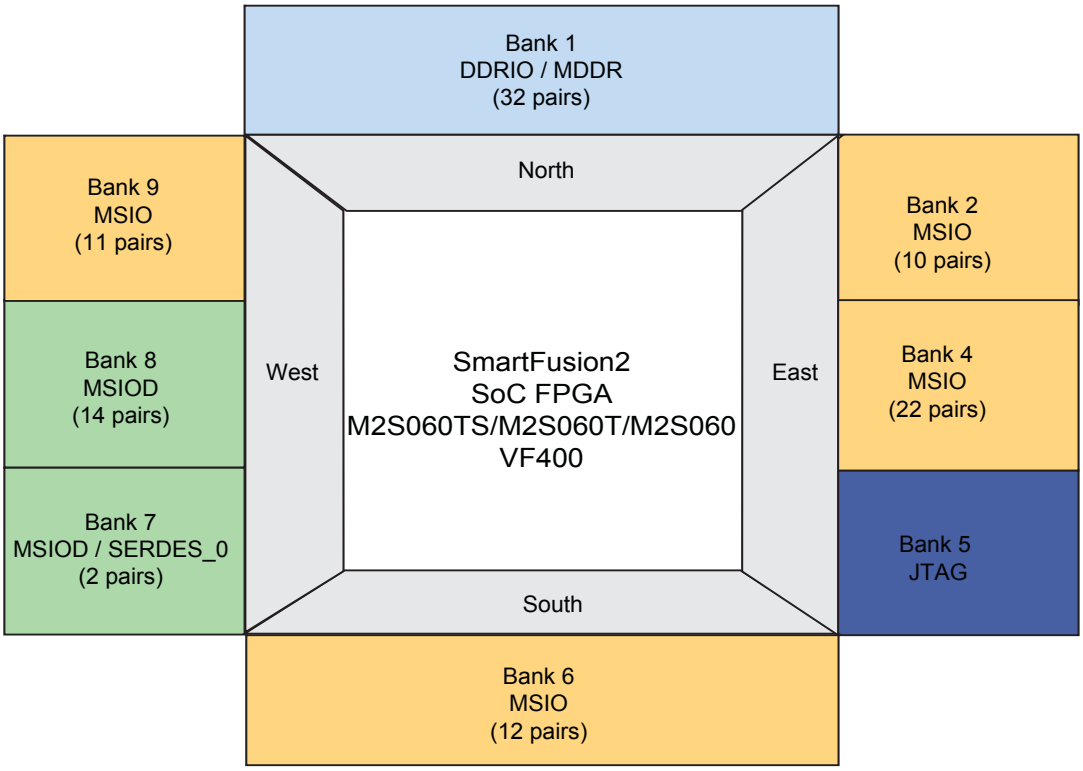
Note: In bank 1 there are 9 single-ended user I/Os. Pin D21, MSI16NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI16NB1 is an input only pin.

***Figure 11* • SmartFusion2 M2S005S/M2S005-FG484 I/O Bank Locations**



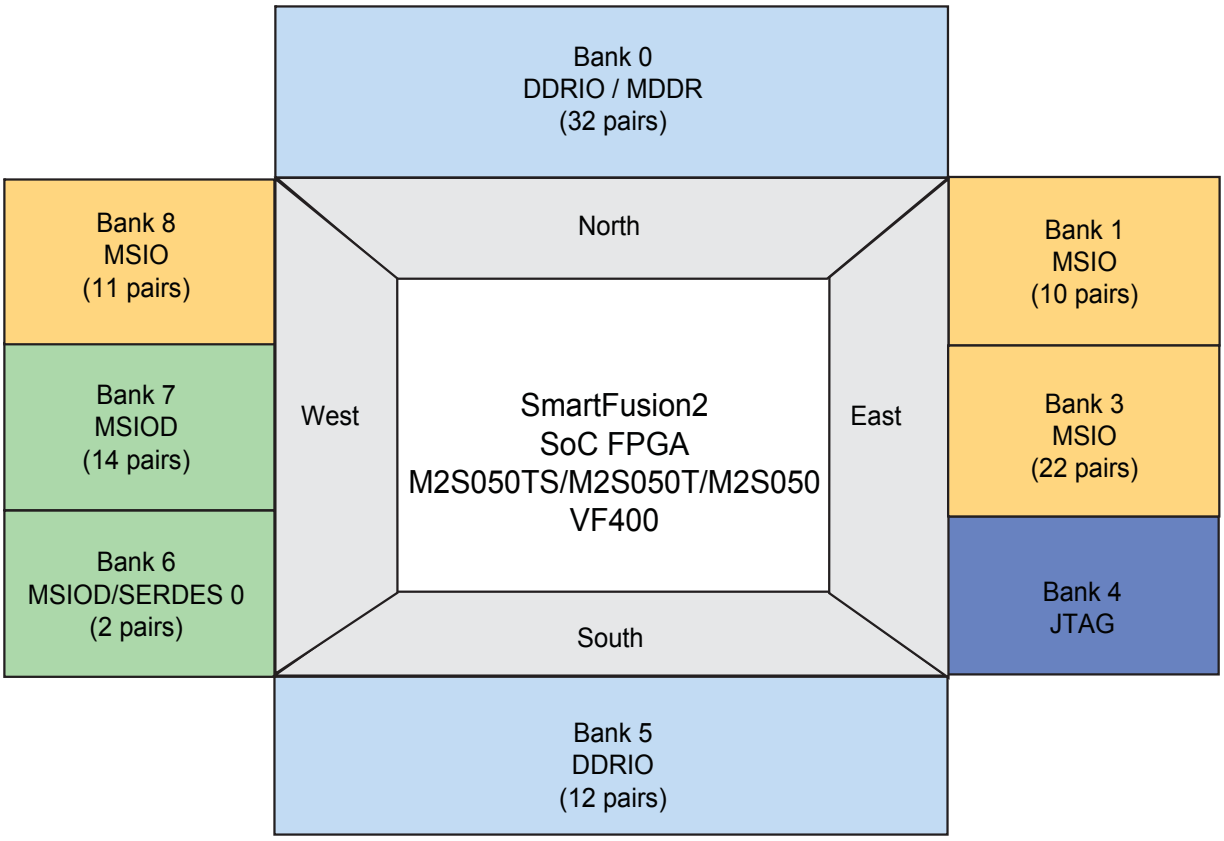
Note: For the M2S150-FCV484 device, SERDES block is not available in banks 9, 10, 12, and 13.

***Figure 12* • SmartFusion2 M2S150TS/M2S150T/M2S150-FCV484 I/O Bank Locations**



Note: *For the M2S060-VF400 device, SERDES block is not available in bank 7.*

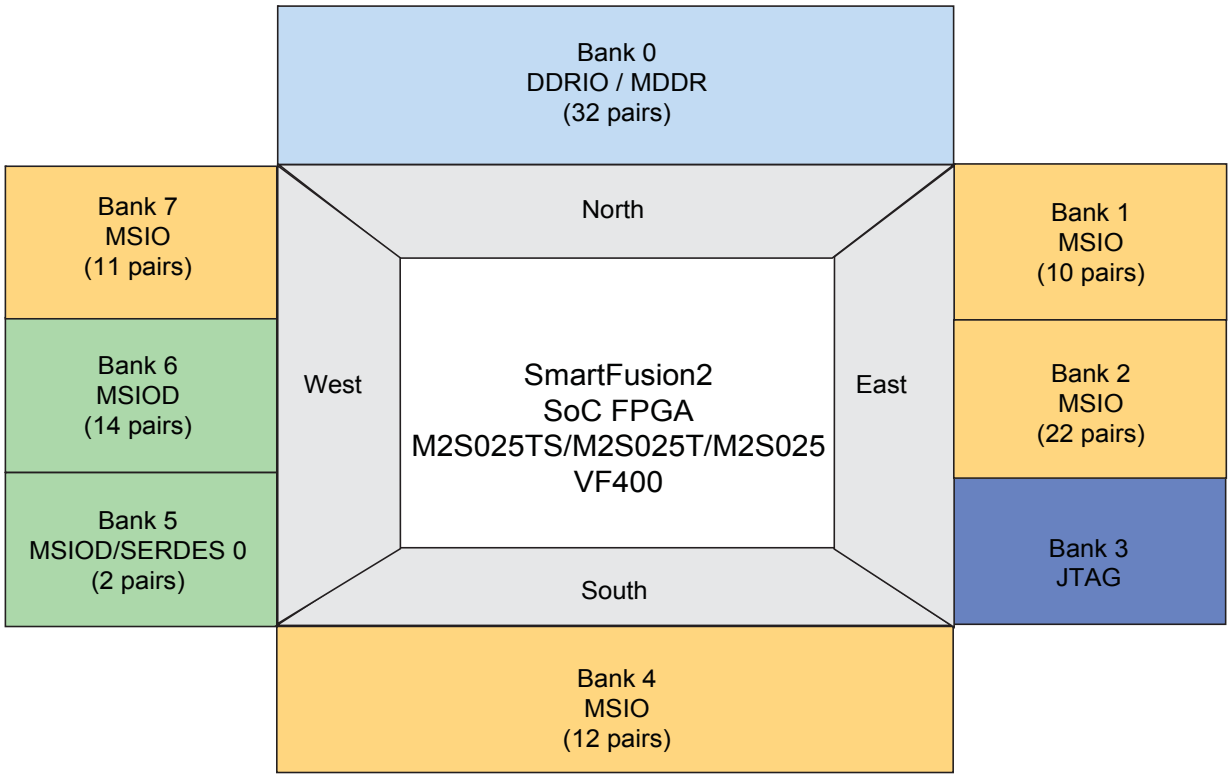
***Figure 13* • SmartFusion2 M2S060TS/M2S060T/M2S060-VF400 I/O Bank Locations**



Notes:

1. *In bank 1, there are 21 single-ended user I/Os. Pin D18, MSI46NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI46NB1 is an input only pin.*
2. *For M2S050-VF400 device, SERDES block is not available in bank 6.*

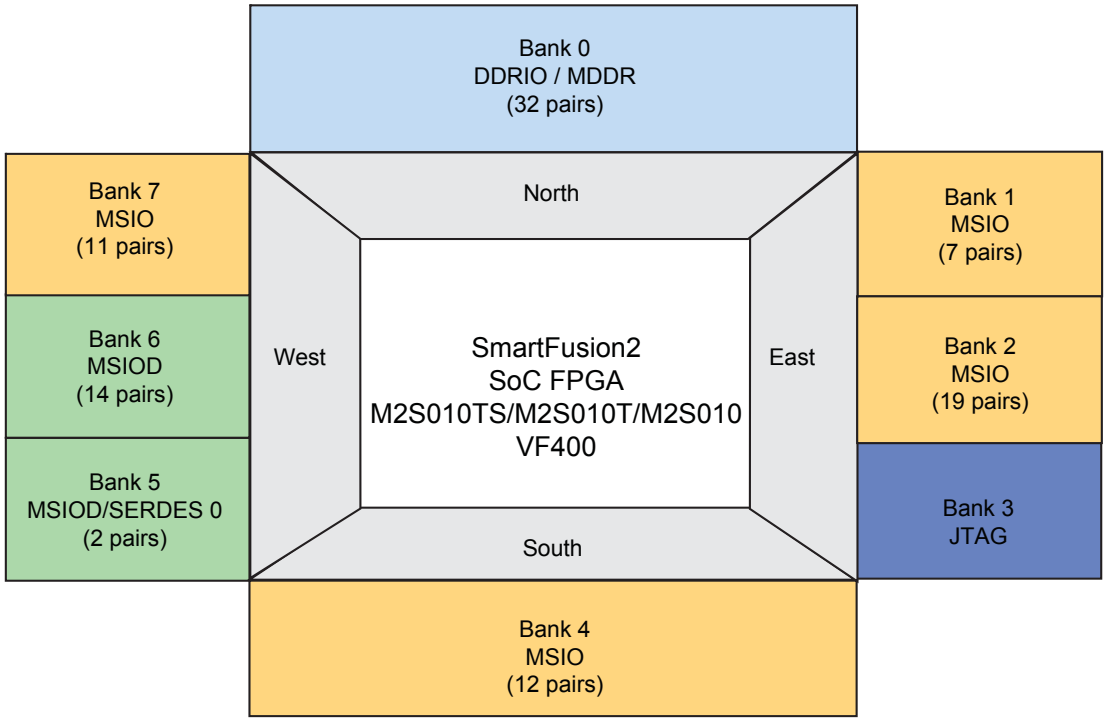
***Figure 14* • SmartFusion2 M2S050TS/M2S050T/M2S050-VF400 I/O Bank Locations**



Notes:

1. *In bank 1, there are 21 single-ended user I/Os. Pin D18, MSI32NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI32NB1 is an input only pin.*
2. *For M2S025-VF400 device, SERDES block is not available in bank 5.*

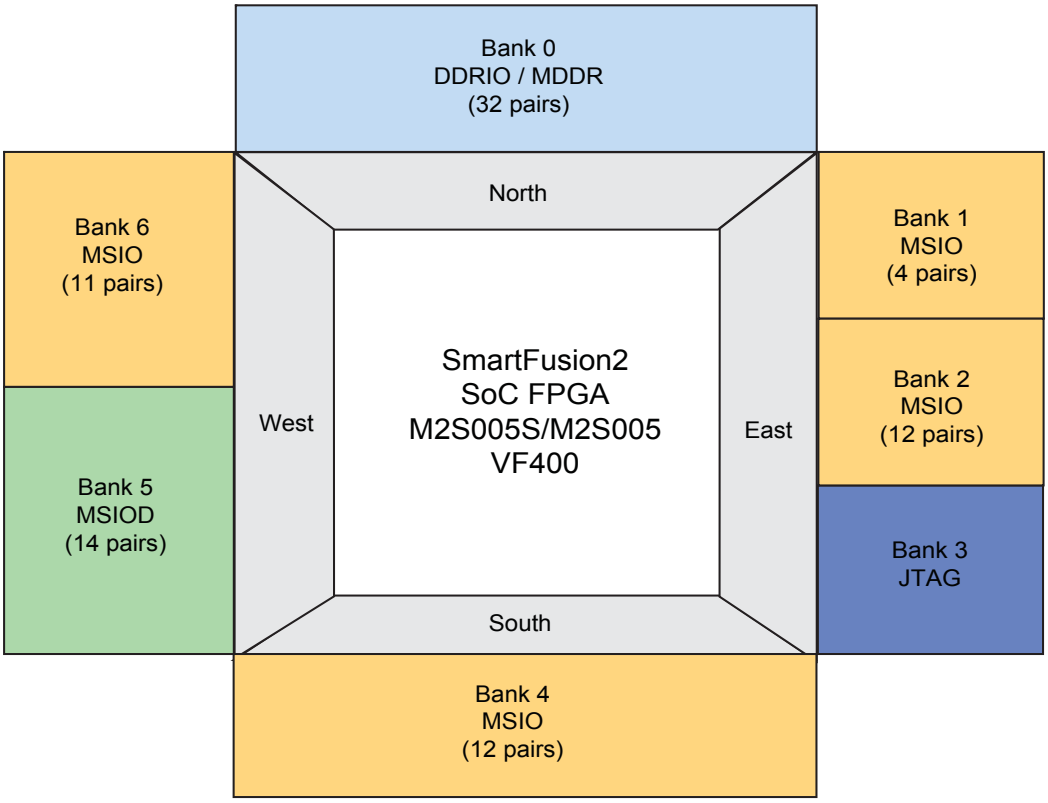
***Figure 15* • SmartFusion2 M2S025TS/M2S025T/M2S025-VF400 I/O Bank Locations**



Notes:

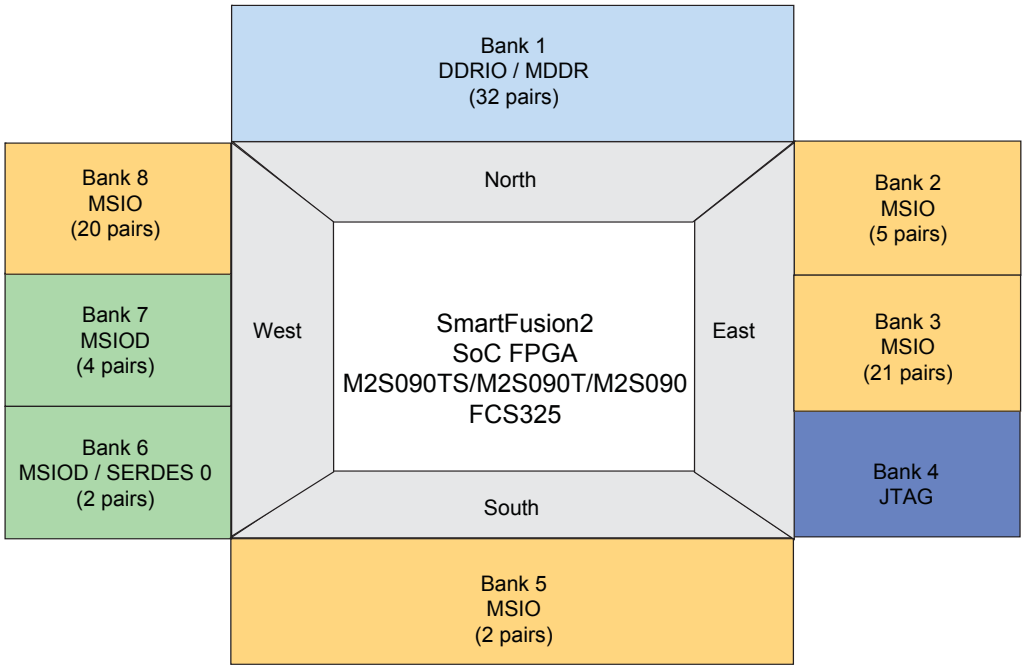
1. *In bank 1 there are 15 single-ended user I/Os. Pin D18, MSI26NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI26NB1 is an input only pin.*
2. *For M2S010-VF400 device, SERDES block is not available in bank 5.*

***Figure 16* • SmartFusion2 M2S010TS/M2S010T/M2S010-VF400 I/O Bank Locations**



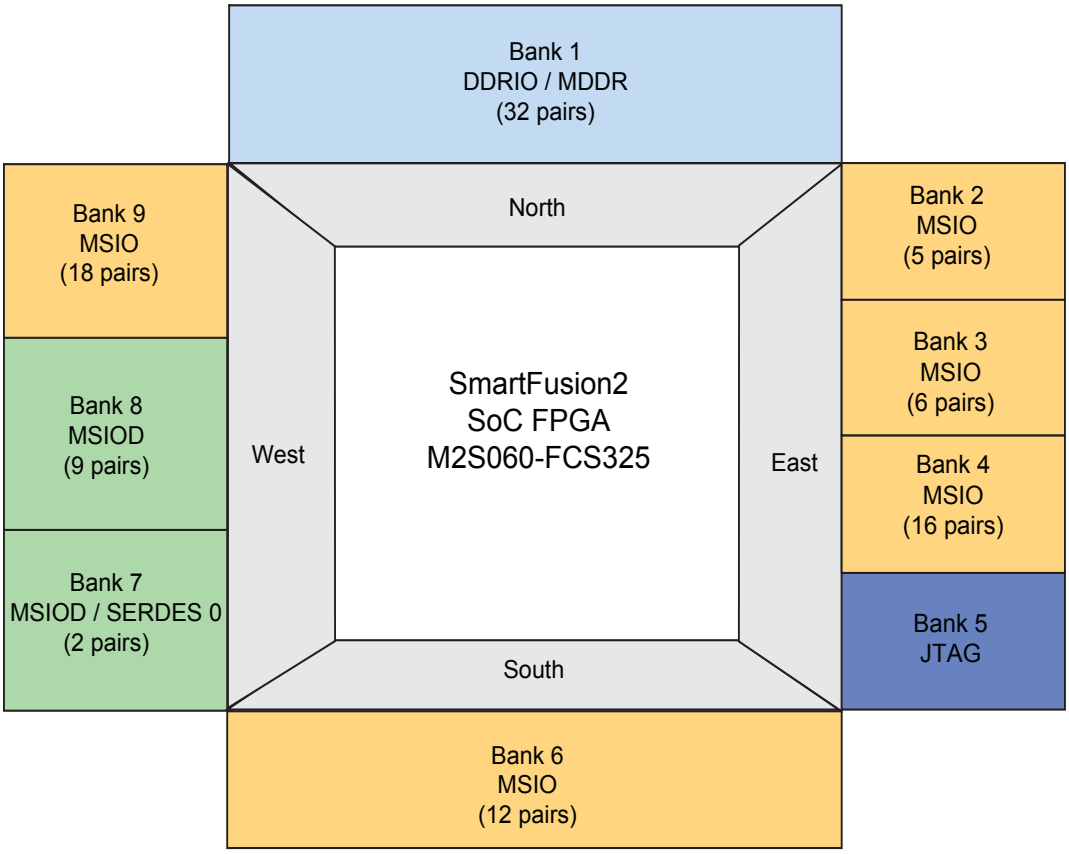
Note: In bank 1 there are 9 single-ended user I/Os. Pin D18, MSI16NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI16NB1 is an input only pin.

***Figure 17* • SmartFusion2 M2S005S/M2S005-VF400 I/O Bank Locations**



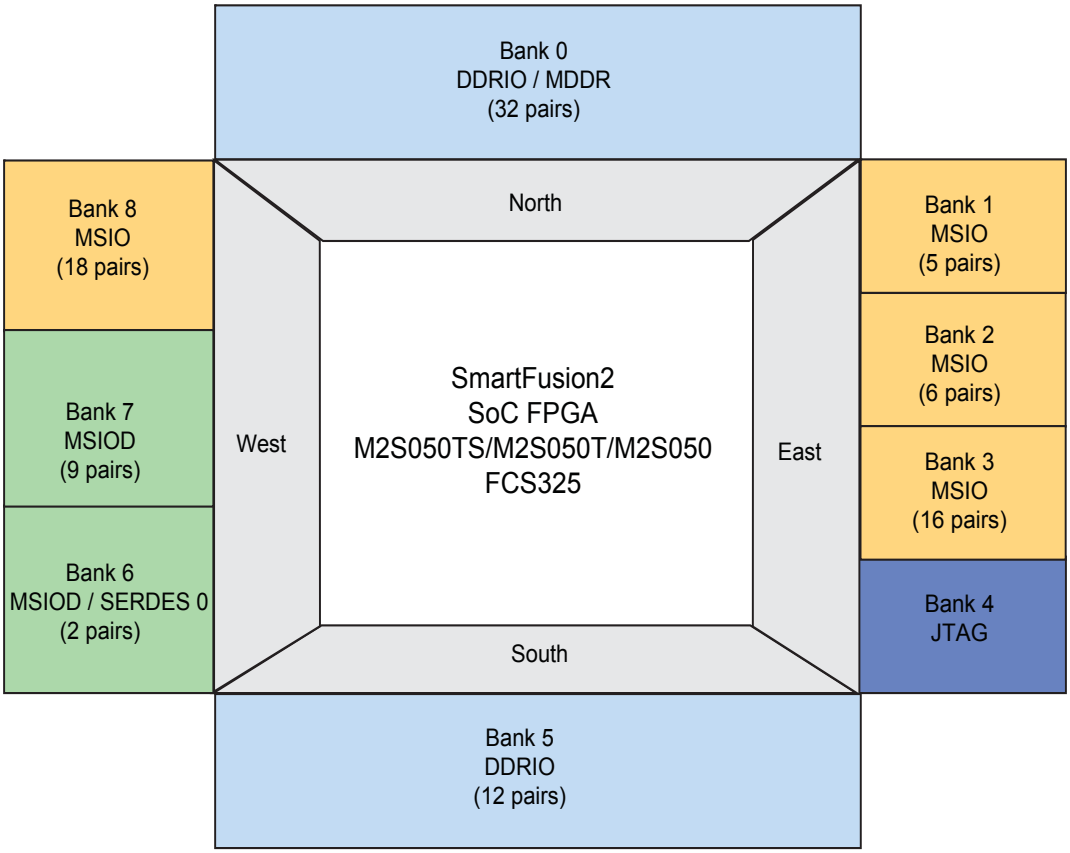
Note: For M2S090-FCS325 device, SERDES block is not available in bank 6.

***Figure 18* • SmartFusion2 M2S090TS/M2S090T/M2S090-FCS325 I/O Bank Locations**



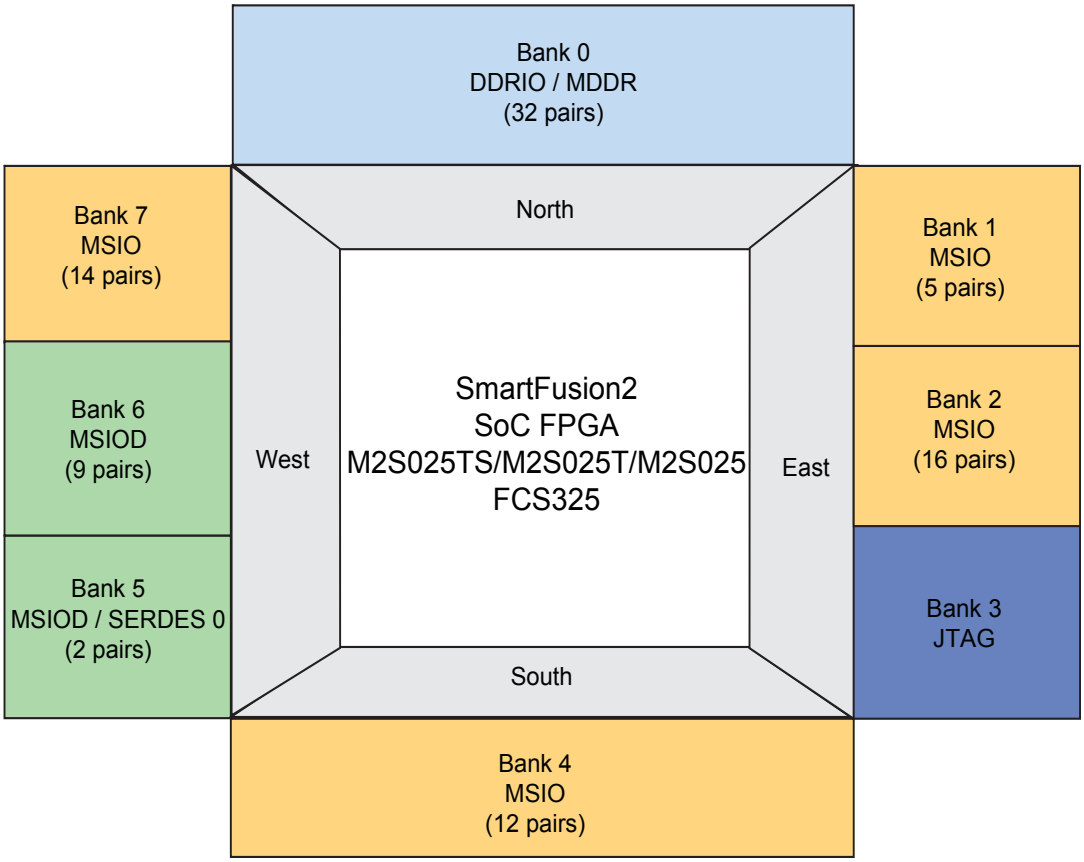
Note: For M2S060-FCS325 device, SERDES block is not available in bank 7.

***Figure 19* • SmartFusion2 M2S060-FCS325 I/O Bank Locations**



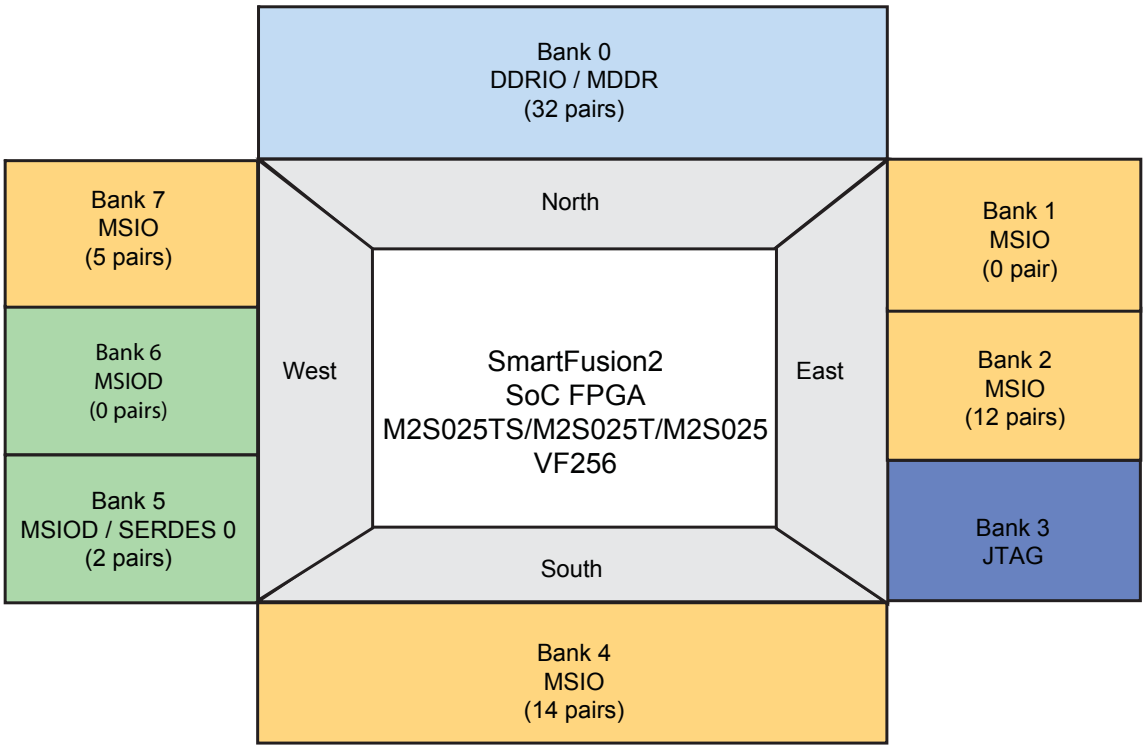
Note: For M2S050-FCS325 device, SERDES block is not available in bank 6.

***Figure 20* • SmartFusion2 M2S050TS/M2S050T/M2S050-FCS325 I/O Bank Locations**



Note: For M2S025-FCS325 device, SERDES block is not available in bank 5.

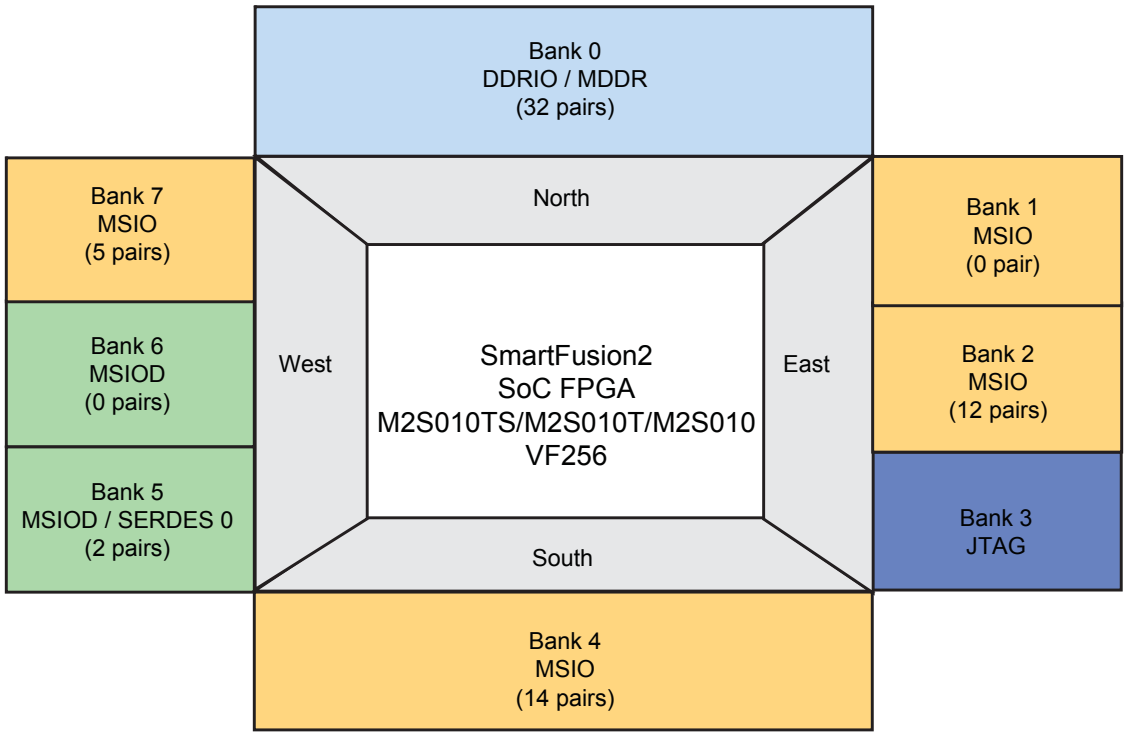
***Figure 21* • SmartFusion2 M2S025TS/M2S025T/M2S025-FCS325 I/O Bank Locations**



Notes:

1. *In bank 1, there are 4 single-ended user I/Os. Pin G12, MSIO32NB1/MMUART_0_TXD/GPIO_27_B, cannot be configured as differential. The function MSI32NB1 is an input only pin.*
2. *For M2S025-VF256 device, SERDES block is not available in bank 5.*

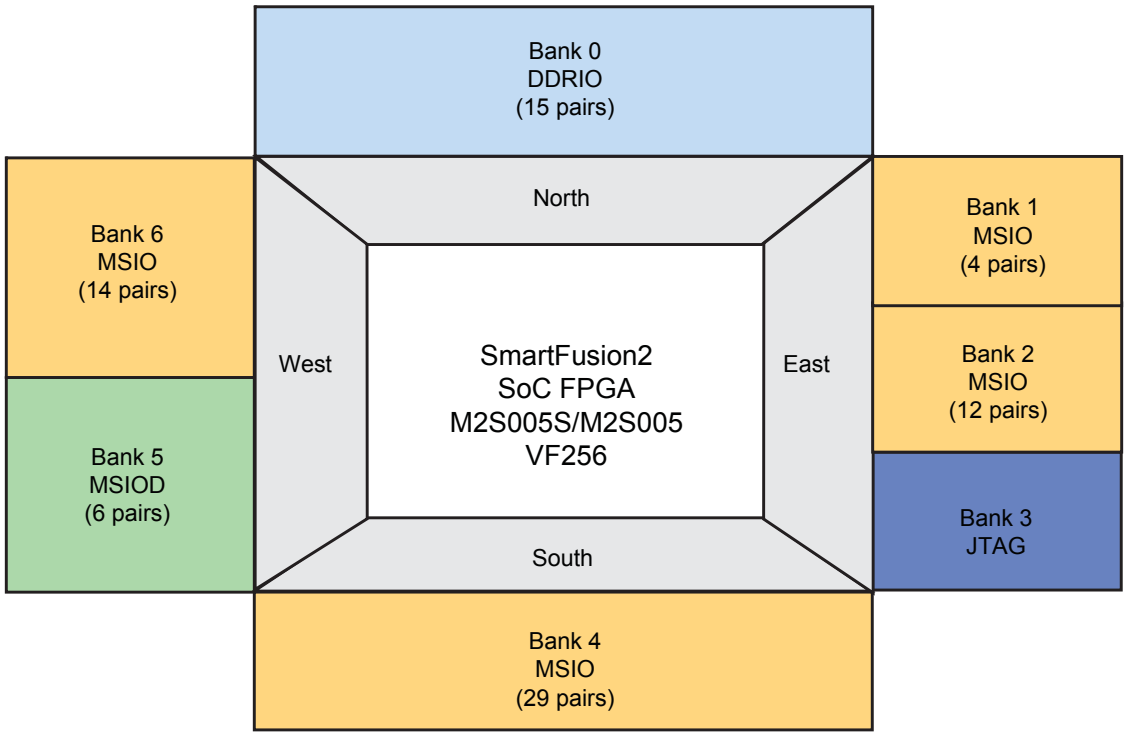
***Figure 22* • SmartFusion2 M2S025TS/M2S025T/M2S025-VF256 I/O Bank Locations**



Notes:

1. *In bank 1, there are 4 single-ended user I/Os. Pin G12, MSI26NB1/MMUART_0_TXD/GPIO_27_B, cannot be configured as differential. The function MSI26NB1 is an input only pin.*
2. *For M2S010-VF256 device, SERDES block is not available in bank 5.*

***Figure 23* • SmartFusion2 M2S010TS/M2S010T/M2S010-VF256 I/O Bank Locations**



Note: In bank 1 there are 9 single-ended user I/Os. Pin D12, MSI16NB1/MMUART_0_TXD/GPIO_27_B, cannot be configured as differential. The function MSI16NB1 is an input only pin.

***Figure 24* • SmartFusion2 M2S005S/M2S005-VF256 I/O Bank Locations**

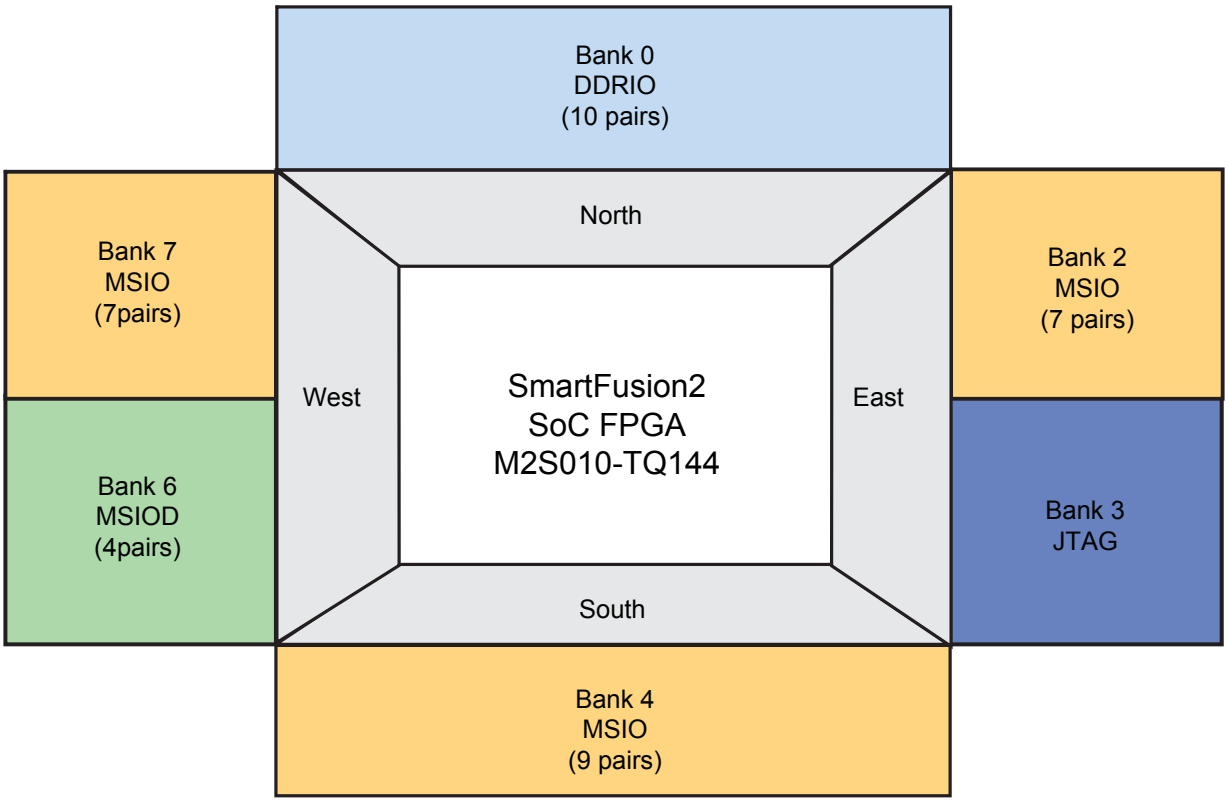


***Figure 25* • SmartFusion2 M2S010-TQ144 I/O Bank Locations**

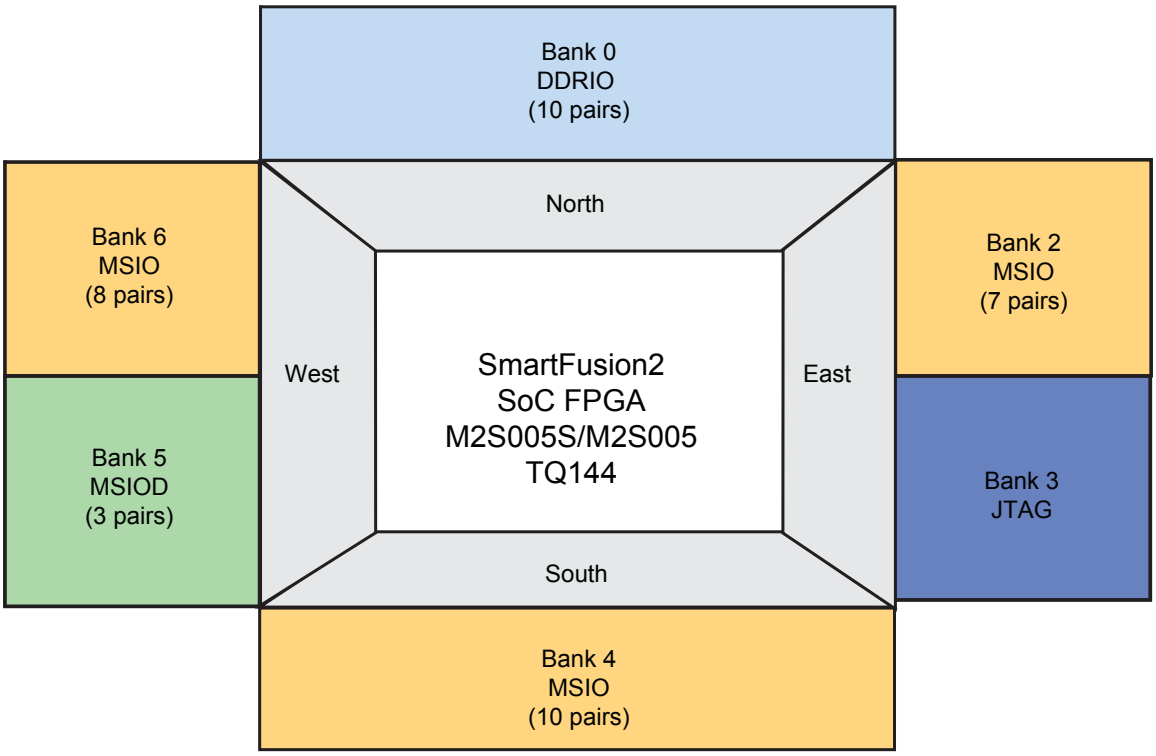


***Figure 26* • SmartFusion2 M2S005S/M2S005-TQ144 I/O Bank Locations**

Table 1 • **Organization of I/O Banks in SmartFusion2 Devices - FC1152, FCS536, FCV484, FG896, FG676, and FG484**

	FC1152	FCS536	FCV484	FG896	FG676		FG484					
Bank No.	**M2S150TS M2S150T M2S150**	**M2S150TS M2S150T M2S150**	**M2S150TS M2S150T M2S150**	**M2S050TS M2S050T M2S050**	**M2S090TS M2S090T M2S090**	**M2S060TS M2S060T M2S060**	**M2S090TS M2S090T M2S090**	**M2S060TS M2S060T M2S060**	**M2S050TS M2S050T M2S050**	**M2S025TS M2S025T M2S025**	**M2S010TS M2S010T M2S010**	**M2S005S**
Bank 0	MSIO: fabric	MSIO: fabric	–	DDRIO: MDDR or fabric	MSIO: fabric	MSIO: fabric	–	–	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric
Bank 1	DDRIO: FDDR or fabric	DDRIO: FDDR or fabric	DDRIO: FDDR or fabric	MSIO: MSS or fabric	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric
Bank 2	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: fabric	MSIO: MSS or fabric	MSIO: fabric		MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric
Bank 3	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: fabric	MSIO: MSS or fabric		MSIO: MSS or fabric	JTAG/ SWD	JTAG/ SWD	JTAG/ SWD
Bank 4	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric	JTAG/ SWD	JTAG/ SWD	MSIO: fabric	JTAG/ SWD	MSIO: fabric	JTAG/ SWD	MSIO: fabric	MSIO: fabric	MSIO: fabric
Bank 5	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric	DDRIO: FDDR or fabric	MSIO: fabric	JTAG/ SWD	MSIO: fabric	JTAG/ SWD	DDRIO: FDDR or fabric	MSIOD: SERDES 0 or fabric	MSIOD: SERDES 0 or fabric	MSIOD: fabric
Bank 6	MSIO: fabric		MSIO: fabric	MSIOD: SERDES 0 or fabric	MSIOD: SERDES 0 or fabric	MSIO: fabric	MSIOD: SERDES 0 or fabric	MSIO: fabric	MSIOD: SERDES 0 or fabric	MSIOD: fabric	MSIOD: fabric	MSIO: fabric
Bank 7	JTAG/ SWD	JTAG/ SWD	JTAG/ SWD	MSIOD: fabric	MSIOD: fabric	MSIOD: SERDES 0 or fabric	MSIOD: fabric	MSIOD: SERDES 0 or fabric	MSIOD: fabric	MSIO: fabric	MSIO: fabric	–
Bank 8	MSIO: fabric	MSIO: fabric	–	MSIO: fabric	MSIO: fabric	MSIOD: SERDES 0 or fabric	MSIO: fabric	MSIOD: fabric	MSIO: fabric	–	–	–

Note: Banks that are shaded should always be powered with the appropriate VDDI bank supplies.

Table 1 • **Organization of I/O Banks in SmartFusion2 Devices - FC1152, FCS536, FCV484, FG896, FG676, and FG484 (continued)**

	FC1152	FCS536	FCV484	FG896	FG676		FG484					
Bank No.	**M2S150TS M2S150T M2S150**	**M2S150TS M2S150T M2S150**	**M2S150TS M2S150T M2S150**	**M2S050TS M2S050T M2S050**	**M2S090TS M2S090T M2S090**	**M2S060TS M2S060T M2S060**	**M2S090TS M2S090T M2S090**	**M2S060TS M2S060T M2S060**	**M2S050TS M2S050T M2S050**	**M2S025TS M2S025T M2S025**	**M2S010TS M2S010T M2S010**	**M2S005S**
Bank 9	MSIOD: SERDES 3 or fabric	MSIOD: SERDES 3 or fabric	MSIOD: SERDES 3 or fabric	MSIOD: SERDES 1 or fabric	–	MSIO: fabric	–	MSIO: fabric	–	–	–	–
Bank 10	MSIOD: SERDES 2 or fabric	MSIOD: SERDES 2 or fabric	MSIOD: SERDES 2 or fabric	–	–	–	–	–	–	–	–	–
Bank 11	MSIO: fabric	MSIO: fabric	MSIO: fabric	–	–	–	–	–	–	–	–	–
Bank 12	MSIOD: SERDES 1 or fabric	MSIOD: SERDES 1 or fabric	MSIOD: SERDES 1 or fabric	–	–	–	–	–	–	–	–	–
Bank 13	MSIOD: SERDES 0 or fabric	MSIOD: SERDES 0 or fabric	MSIOD: SERDES 0 or fabric	–	–	–	–	–	–	–	–	–
Bank 14	MSIO: fabric	MSIO: fabric	MSIO: fabric	–	–	–	–	–	–	–	–	–
Bank 15	MSIOD: fabric	MSIOD: fabric	–	–	–	–	–	–	–	–	–	–
Bank 16	MSIOD: fabric	MSIOD: fabric	MSIOD: fabric	–	–	–	–	–	–	–	–	–
Bank 17	MSIO: fabric	MSIO: fabric	MSIO: fabric	–	–	–	–	–	–	–	–	–
Bank 18	MSIO: fabric	MSIO: fabric	–	–	–	–	–	–	–	–	–	–

Note: Banks that are shaded should always be powered with the appropriate VDDI bank supplies.

Table 2 • **Organization of I/O Banks in SmartFusion2 Devices - VF400, FCS325, VF256, and TQ144**

	VF400					FCS325				VF256			TQ144	
Bank No	**M2S060TS M2S060T M2S060**	**M2S050TS M2S050T M2S050**	**M2S025TS M2S025T M2S025**	**M2S010TS M2S010T M2S010**	**M2S005S**	**M2S090TS M2S090T M2S090**	**M2S060TS M2S060T M2S060**	**M2S050TS M2S050T M2S050**	**M2S025TS M2S025T M2S025**	**M2S025TS M2S025T M2S025**	**M2S010TS M2S010T M2S010**	**M2S005S**	**M2S010**	**M2S005S**
Bank 0	–	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	–	–	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	DDRIO: fabric	DDRIO: fabric	DDRIO: fabric
Bank 1	DDRIO: MDDR or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric		
Bank 2	MSIO: fabric	–	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: fabric	MSIO: fabric	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric
Bank 3	–	MSIO: MSS or fabric	JTAG/ SWD	JTAG/ SWD	JTAG/ SWD	MSIO: fabric	MSIO: fabric	MSIO: MSS or fabric	JTAG/ SWD	JTAG/ SWD	JTAG/ SWD	JTAG/ SWD	JTAG/ SWD	JTAG/ SWD
Bank 4	MSIO: fabric	JTAG/ SWD	MSIO: fabric	MSIO: fabric	MSIO: fabric	JTAG/ SWD	MSIO: fabric	JTAG/ SWD	MSIO: fabric	MSIO: fabric	MSIO: fabric	MSIO: fabric	MSIO: fabric	MSIO: fabric
Bank 5	JTAG/ SWD	DDRIO: FDDR or fabric	MSIOD: SERDES 0 or fabric	MSIOD: SERDES 0 or fabric	MSIOD: fabric	MSIO: fabric	JTAG/ SWD	DDRIO: FDDR or fabric	MSIOD: SERDES 0 or fabric	MSIOD: SERDES 0 or fabric	MSIOD: SERDES 0 or fabric	MSIOD: fabric	–	MSIOD: fabric
Bank 6	MSIO: fabric	MSIOD: SERDES 0 or fabric	MSIOD: fabric	MSIOD: fabric	MSIO: fabric	MSIOD: SERDES 0 or fabric	MSIO: fabric	MSIOD: SERDES 0 or fabric	MSIO: fabric	MSIOD: fabric	MSIOD: fabric	MSIO: fabric	MSIOD: fabric	MSIO: fabric
Bank 7	MSIOD: SERDES 0 or fabric	MSIOD: fabric	MSIO: fabric	MSIO: fabric	–	MSIOD: fabric	MSIOD: SERDES 0 or fabric	MSIOD: fabric	MSIO: fabric	MSIO: fabric	MSIO: fabric	–	MSIO: fabric	–
Bank 8	MSIOD: fabric	MSIO: fabric	–	–	–	MSIO: fabric	MSIOD: fabric	MSIO: fabric	–	–	–	–	–	–
Bank 9	MSIO: fabric	–	–	–	–	–	MSIO: fabric	–	–	–	–	–	–	–

Note: Banks that are shaded should always be powered with the appropriate VDDI bank supplies.

Table 3 • **User I/O Types**

Name	Type	Description
MSIOxyBz	In/out	MSIOs provide programmable drive strength, weak pull-up, and weak-pull-down. In single ended mode, the I/O pair operates as two separate I/Os named P and N. Some of these pins are also multiplexed with integrated peripherals in the MSS (I^2C, USB, SPI, UART, CAN, and fabric I/Os).This allows MSIO pins to be multiplexed as I/Os for the FPGA fabric, the ARM® Cortex®-M3 processor, or for given integrated MSS peripherals. MSIOs can be routed to dedicated I/O buffers (MSSIOBUF) or in some cases to the FPGA fabric interface through an IOMUX. SmartFusion2 I/O ports also support ESD protection. MSIO I/O cells operate at up to 3.3 V and are capable of high-speed LVDS2V5 and LVDS3V3 operation.
MSIODxyBz	In/out	MSIOD is very similar to MSIO, but drops 3.3 V and hot-plug support and adds pre-emphasis, in order to achieve higher speeds. MSIODs provide programmable drive strength, weak pull-up, and weak pull-down. MSIOD I/O cells operate at up to 2.5 V and are capable of high-speed LVDS2V5 operation. Some of these pins are also multiplexed with the SERDES interface. SmartFusion2 I/O ports support ESD protection.
DDRIOxyBz	In/out	The double data input output (DDRIO) is a multi-standard I/O optimized for LPDDR/DDR2/DDR3 performance. In SmartFusion2 devices there are two DDR subsystems: the fabric DDR and MSS DDR controllers. All DDRIOs can be configured as differential I/Os or two single-ended I/Os. If you select MDDR/FDDR, Libero SoC automatically connects MDDR/FDDR signals to the DDRIOs. DDRIOs can be connected to the respective DDR subsystem PHYs or can be used as user I/Os. Depending on the memory configuration, only the required DDRIOs are used by Libero SoC. The unused DDRIOs are available to connect to the fabric.
Note: For more information on I/O status of MSIO, MSIOD and DDRIO pins during power up/down and default conditions, refer to *AC396: SmartFusion2 and IGLOO2 in Hot Swapping and Cold Sparing Application Note.*		

All user I/Os have internal clamp diode control circuitry. A pull-up clamp diode must not be present in the I/O circuitry if the hot-swap feature is used. The 3.3 V PCI standard requires a pull-up clamp diode on the I/O, so it cannot be selected if hot-swap capability is required.

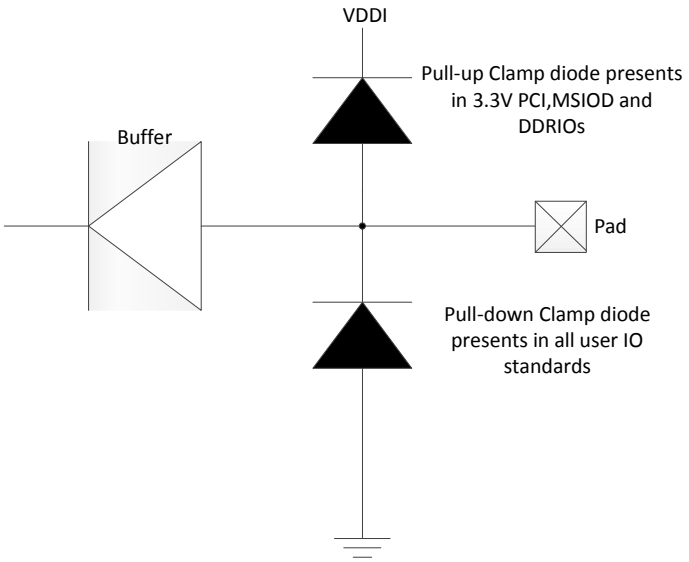


Figure 27 • **Internal Clamp Diode Control Circuitry**

Naming Conventions

User I/O Naming Conventions

The naming convention used for each FPGA user I/O is **IOxyBz**, where:

IO is the type of I/O—MSIO, MSIOD, or DDRIO.

x refers the I/O pair number in bank z.

y is P (positive) or N (negative). In single-ended mode, the I/O pair operates as two separate I/Os named P and N. Differential mode is implemented with a fixed I/O pair and cannot be split with an adjacent I/O.

B is bank.

z refers to bank number (0–9 for M2S050-FG896).

Differential standards are implemented as true differential outputs and complementary single-ended outputs for SSTL/HSTL. In the single-ended mode, the I/O pair operates as two separate I/Os named P and N. All the configuration and data inputs/outputs are then separate and use names ending in P and N to differentiate between the two I/Os.

For more information, refer to the "I/Os" chapter of the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide*.

Dedicated Global I/O Naming Conventions

Dedicated global I/Os are dual-use I/Os which can drive the global blocks either directly or through clock conditioning circuits (CCC) or virtual clock conditioning circuits (VCCC). They can also be used as regular user I/Os. These global I/Os are the primary source for bringing in the external clock inputs into the SmartFusion2 device.

In the M2S050T-FG896 device, there are 16 global blocks located in the center of the fabric and 32 global I/Os located 8 each on the north, east, south, and west sides of the fabric. There are 6 CCC blocks, located 2 each on northwest, northeast, and southwest side of the fabric and 2 VCCC blocks on the southeast side of the fabric.

Dedicated global I/Os that drive the global blocks (GB) directly are named as **GBn,** where

n is 0 to 15.

Dedicated global I/Os that drive GBs through CCCs are named as **CCC_xyz_CLKIw**, where:

xy is the location—NE, SW, or NW.

z is 0 or 1.

I represents input clock

w refers to one of the four possible output clocks of the associated CCC_xyz—GL0, GL1, GL2, or GL3.

Dedicated global I/Os that drive GBs through VCCCs are named as **VCCC_SEz**, where:

SE is southeast.

z is 0 or 1.

Unused dedicated global I/Os behave similarly to unused regular User I/Os (MSIO, MSIOD, DDRIO). Libero configures unused User I/Os as input buffer disabled, output buffer tristated with weak pull-up.

For further details, refer to the "Fabric Global Routing Resources" chapter of the *UG0449: SmartFusion2 SoC FPGA and IGLOO2 FPGA Clocking Resources User Guide*.

Multi-Function I/Os

Certain I/Os can have more than one function. Users select the functionality through Libero configuration tools.

The name of a pin shows the functionalities for which that pin can be configured and used.

Example pin name: **MSIO48NB1/I2C_0_SCL/GPIO_31_B/USB_DATA1_C**

This I/O port is multi-purpose and can be configured as MSIO, I2C0 clock, fabric I/O, or USB_DATA1_C.

MDDR/FDDR Interface

SmartFusion2 devices have MDDR/ FDDR blocks. The DDR subsystems are hardened ASIC blocks for interfacing the LPDDR, DDR2, and DDR3 memories. It supports 8-/16-/32-bit data bus width modes. The DDRIO uses fixed impedance calibration for different drive strengths. These values can be programmed using Libero SoC software for the selected I/O standard. The values are fed to the pull-up/pull-down reference network to match the impedance with an external resistor. For more information about reference resistor values (for different drive modes), refer to the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide*.

DDR Controller Pins

Table 4 shows the DDR Controller pins.

Table 4 • **DDR Controller Pins**

Pin Name	Type	Reference Resistor (Ω)
xDDR_CAS_N	Out	DRAM CASN.
xDDR_CKE	Out	DRAM Clock enable.
xDDR_CLK	Out	DRAM single-ended clock for differential pads.
xDDR_CLK_N	Out	DRAM single-ended clock for differential pads.
xDDR_CS_N	Out	DRAM Chip select.
xDDR_ODT	Out	DRAM on-die termination (ODT). 0: Termination Off 1: Termination On
xDDR_RAS_N	Out	DRAM RASN.
xDDR_RESET_N	Out	DRAM reset for DDR3.
xDDR_WE_N	Out	DRAM Write enable
xDDR_ADDR[15:0]	Out	DRAM address bits.
xDDR_BA[2:0]	Out	DRAM bank address.
xDDR_DM_RDQS[3:0]	In/out	DRAM data mask from bidirectional pads.
xDDR_DQS[3:0]	In/out	DRAM single-ended data strobe output for bidirectional pads.
xDDR_DQS[3:0]_N	In/out	DRAM single-ended data strobe output for bidirectional pads.
xDDR_DQ[31:0]	In/out	DRAM data input or output for bidirectional pads.
xDDR_DQ_ECC[3:0]	In/out	DRAM data input or output for SECDED.
xDDR_DM_RDQS_ECC	In/out	DRAM single-ended data strobe output for bidirectional pads.
xDDR_DQS_ECC	In/out	DRAM single-ended data strobe output for bidirectional pads.
xDDR_DQS_ECC_N	In/out	DRAM data input or output for bidirectional pads.

Notes:

1. *Though calibration is not required, it is recommended to use corresponding resistor placeholder to connect the xDDR_IMP_CALIB to the ground with or without a resistor.*
2. *x represents Fabric or MSS DDR.*

Table 4 • **DDR Controller Pins (continued)**

xDDR_TMATCH_[0/1]_IN	In	DQS enable input for timing match between DQS and system clock. For simulations, tie to xDDR_TMATCH_[0/1]_OUT.
xDDR_TMATCH_[0/1]_OUT	Out	DQS enable output for timing match between DQS and system clock. For simulations, tie to xDDR_TMATCH_[0/1]_IN.
xDDR_TMATCH_ECC_IN	In	DQS enable input for timing match between DQS and system clock. For simulations, tie to xDDR_TMATCH_ECC_OUT.
xDDR_TMATCH_ECC_OUT	Out	DQS enable output for timing match between DQS and system clock. For simulations, tie to xDDR_TMATCH_ECC_IN.
xDDR_IMP_CALIB	Ref	Pull-down with resistor depending on voltage/standard: • DDR2 - 150 Ω • DDR3 (1.5 V) - 240 Ω • LPDDR - 150 Ω

Notes:

1. *Though calibration is not required, it is recommended to use corresponding resistor placeholder to connect the xDDR_IMP_CALIB to the ground with or without a resistor.*
2. *x represents Fabric or MSS DDR.*

For more information about DDR memory calibration, refer to the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide*.

For DDR termination details refer *AC393: SmartFusion2 and IGLOO2 Board Design Guidelines Application Note*.

I/O Standards

Table 5 shows the supported I/O standards for different DDR memories.

Table 5 • **Supported I/O Standards for Different DDR Memories**

Memory Type	I/O Standard
DDR3	SSTL15I, SSTL15II
DDR2	SSTL18I, SSTL18II
LPDDR	LVCMOS18

Supply Pins

SmartFusion2 devices support multi-standard I/Os (MSIOs), MSIODs, double data rate I/Os (DDRIOs), microcontroller serial interfaces, high speed serial interfaces, and a debugging JTAG interface. SmartFusion2 devices require the power supplies listed in Table 6.

Table 6 • **Supply Pins**

Name	Type	Description
VDD	Supply	DC core supply voltage. Must always power this pin.
VPP	Supply[1]	Power supply for charge pumps (for normal operation and programming). Must always power this pin.
VPPNVM	Supply[1]	Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to VPP.
VDDIx	Bank power supplies[2]	VDDIx, Bank x power
VREFx	Supply[3]	Reference voltage for MDDR/FDDR signals which is powered through the corresponding Bank Supply (VDDIx). When **unused**, VREFx can be DNC or grounded (VSS).
CCC_NE0_PLL_VDDA	PLL power supplies[4]	Analog power pad for PLL0
CCC_NE1_PLL_VDDA		Analog power pad for PLL1
CCC_NW0_PLL_VDDA		Analog power pad for PLL2
CCC_NW1_PLL_VDDA		Analog power pad for PLL3
CCC_SW0_PLL_VDDA		Analog power pad for PLL4
CCC_SW1_PLL_VDDA		Analog power pad for PLL5
MSS_MDDR_PLL_VDDA		Analog power pad for PLL of MDDR and MSS
FDDR_PLL_VDDA		Analog power pad for PLL of FDDR

Notes:

1. *For details on VPP and VPPNVM power supplies, refer to Table 2 - Recommended Operating Conditions of the DS0128: IGLOO2 FPGA and SmartFusion2 SoC FPGA Datasheet.*
2. *For details on bank power supplies, refer to the "Recommendation for Unused Bank Supplies" table in the AC393: SmartFusion2 and IGLOO2 Board Design Guidelines Application Note. For more details on user I/O pins (MSIO, MSIOD, DDRIO) and supported voltage standards, refer to the Supported Voltage Standards table in the UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide.*
3. *Reference voltages should be powered with the appropriate bank supplies through voltage divider circuitry. If I/O banks are being used as single-ended I/Os (and MDDR or FDDR functionalities are not being used), then VREFx can be left floating (DNC) even though the VDDIx powered to the corresponding supplies.*
4. *If used as PLL, the supply must be connected over resistor and capacitors (filter circuitry) to a common PLL supply (2.5 V or 3.3 V) to the corresponding on-board PLL return path. If PLL is unused or used as divider, the supply must connect directly to either 2.5 V or 3.3 V (without filter circuitry).*
5. *If used, all SERDES PLL pins must be powered through resistor and capacitors (filter circuitry) to the correct appropriate supply to the corresponding on-board return path. If **unused** must connect directly to the appropriate supplies (without filter circuitry).*
6. *If used, all CCC PLL pins must be powered through resistor and capacitors (filter circuitry) to the appropriate supply to the corresponding on-board return path on-board. If unused must connect directly to the Ground (without filter circuitry).*

Table 6 • **Supply Pins (continued)**

Name	Type	Description
SERDES_x_VDD	SERDESx power supplies[5]	PCIe/PCS supply. It is a +1.2 V supply and internally shorted to VDD.
SERDES_x_L01_VDDAIO		Tx/Rx analog I/O voltage. Low voltage power for Lane0 and Lane1 of SERDESIFx, located on the left side. It is a +1.2 V SERDES PMA supply.
SERDES_x_L23_VDDAIO		Tx/Rx analog I/O voltage. Low voltage power for Lane2 and Lane3 of SERDESIFx, located on the right side. It is a +1.2 V SERDES PMA supply.
SERDES_x_L01_VDDAPLL		Analog power for SERDESx PLL of Lane0 and Lane1. In used condition, it must be connected to +2.5 V. In unused condition, it can be connected to either +2.5 V or VDD (1.2 V).
SERDES_x_L23_VDDAPLL		Analog power for SERDESx PLL of Lane2 and Lane3. In used condition, it must be connected to +2.5 V. In unused condition, it can be connected to either +2.5 V or VDD (1.2 V).
SERDES_x_L01_REFRET		Local on-chip ground return path for SERDES_x_L01_VDDAPLL for Lane0 and Lane1 of SERDESIF0, located on the left side. If unused, it must be grounded (VSS).
SERDES_x_L23_REFRET		Local on-chip ground return path for SERDES_x_L23_VDDAPLL for Lane2 and Lane3 of SERDESIF0, located on the right side. If unused, it must be grounded (VSS).
SERDES_x_PLL_VDDA		High supply voltage for PLL SERDESx. It can be +2.5 V or +3.3 V.
SERDES_x_PLL_VSSA		VDDA to on-die VSSA high pass filter connection for PLL SERDESx. If unused, it must be grounded (VSS).
CCC_NE0_PLL_VSSA	PLL return paths[6]	Return path for corresponding analog PLL VDDA supply. High frequency noise should be eliminated by placing the R-C filter circuitry in between VDDA and VSSA pins.
CCC_NE_PLL_VSSA		
CCC_NW0_PLL_VSSA		
CCC_NW1_PLL_VSSA		
CCC_SW0_PLL_VSSA		
CCC_SW1_PLL_VSSA		
MSS_MDDR_PLL_VSSA		Analog ground pad for PLL of MDDR and MSS
FDDR_PLL_VSSA		Analog ground pad for PLL of FDDR

Notes:

1. *For details on VPP and VPPNVM power supplies, refer to Table 2 - Recommended Operating Conditions of the DS0128: IGLOO2 FPGA and SmartFusion2 SoC FPGA Datasheet.*
2. *For details on bank power supplies, refer to the "Recommendation for Unused Bank Supplies" table in the AC393: SmartFusion2 and IGLOO2 Board Design Guidelines Application Note. For more details on user I/O pins (MSIO, MSIOD, DDRIO) and supported voltage standards, refer to the Supported Voltage Standards table in the UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide.*
3. *Reference voltages should be powered with the appropriate bank supplies through voltage divider circuitry. If I/O banks are being used as single-ended I/Os (and MDDR or FDDR functionalities are not being used), then VREFx can be left floating (DNC) even though the VDDIx powered to the corresponding supplies.*
4. *If used as PLL, the supply must be connected over resistor and capacitors (filter circuitry) to a common PLL supply (2.5 V or 3.3 V) to the corresponding on-board PLL return path. If PLL is unused or used as divider, the supply must connect directly to either 2.5 V or 3.3 V (without filter circuitry).*
5. *If used, all SERDES PLL pins must be powered through resistor and capacitors (filter circuitry) to the correct appropriate supply to the corresponding on-board return path. If **unused** must connect directly to the appropriate supplies (without filter circuitry).*
6. *If used, all CCC PLL pins must be powered through resistor and capacitors (filter circuitry) to the appropriate supply to the corresponding on-board return path on-board. If unused must connect directly to the Ground (without filter circuitry).*

Table 6 • **Supply Pins (continued)**

Name	Type	Description
VSS	Ground	Ground pad for core and I/Os. Must always connect to ground.
VSSNVM		Analog sense circuit ground of eNVM. Must always connect to ground.

Notes:

1. *For details on VPP and VPPNVM power supplies, refer to Table 2 - Recommended Operating Conditions of the DS0128: IGLOO2 FPGA and SmartFusion2 SoC FPGA Datasheet.*
2. *For details on bank power supplies, refer to the "Recommendation for Unused Bank Supplies" table in the AC393: SmartFusion2 and IGLOO2 Board Design Guidelines Application Note. For more details on user I/O pins (MSIO, MSIOD, DDRIO) and supported voltage standards, refer to the Supported Voltage Standards table in the UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide.*
3. *Reference voltages should be powered with the appropriate bank supplies through voltage divider circuitry. If I/O banks are being used as single-ended I/Os (and MDDR or FDDR functionalities are not being used), then VREFx can be left floating (DNC) even though the VDDIx powered to the corresponding supplies.*
4. *If used as PLL, the supply must be connected over resistor and capacitors (filter circuitry) to a common PLL supply (2.5 V or 3.3 V) to the corresponding on-board PLL return path. If PLL is unused or used as divider, the supply must connect directly to either 2.5 V or 3.3 V (without filter circuitry).*
5. *If used, all SERDES PLL pins must be powered through resistor and capacitors (filter circuitry) to the correct appropriate supply to the corresponding on-board return path. If **unused** must connect directly to the appropriate supplies (without filter circuitry).*
6. *If used, all CCC PLL pins must be powered through resistor and capacitors (filter circuitry) to the appropriate supply to the corresponding on-board return path on-board. If unused must connect directly to the Ground (without filter circuitry).*

Additional Notes on Supply Pins

- As an alternative to leaving unused positive and ground level supplies floating (not connected, open), they can be shorted to VSS on-board. This could be considered a better practice in avionics, so that floating supplies do not pick up charge from radiation.
- For on-board connectivity solutions, refer to the *AC393: SmartFusion2 SoC FPGA and IGLOO2 FPGA Board Design Guidelines Application Note*.

JTAG Pins

JTAG pins can operate at any voltage—1.2 V / 1.5 V / 1.8 V / 2.5 V / 3.3 V (nominal). The debug port is implemented using a serial wire JTAG debug port (SWJ-DP) rather than a serial wire debug port (SW-DP). This enables either the M3 JTAG or the SW protocol to be used for debugging.

Table 7 • **JTAG Pin Names and Descriptions**

Name	Type	Bus Size	Description
JTAGSEL	In	1	JTAG controller selection. If JTAGSEL is pulled High, an external TAP controller connects to the JTAG interface—system controller TAP. If JTAGSEL is pulled Low, an external TAP controller connects to either the Cortex-M3 JTAG TAP (if debug is enabled) or an auxiliary TAP (if debug is disabled).
JTAG_TCK/ M3_TCK	In	1	Test clock. Serial input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/pull-down resistor. If JTAG is not used, Microsemi recommends tying it off. Connect TCK to GND or +3.3 V through a resistor placed close to the FPGA pin. This prevents totem-pole current on the input buffer and operation in case TMS enters an undesired state. Note that to operate at all +3.3 V voltages, 500 Ω to 1 kΩ will satisfy the requirements.
JTAG_TDI/ M3_TDI	In	1	Test data. Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.
JTAG_TDO/ M3_TDO/ M3_SWO	Out	1	Test data. Serial output for JTAG boundary scan, ISP, and UJTAG usage. The TDO pin does not have an internal pull-up/-down resistor. M3_SWO: Serial Wire Viewer output
JTAG_TMS/ M3_TMS/ M3_SWDIO		1	Test mode select. The TMS pin controls the use of the IEEE1532 boundary scan pins (TCK, TDI, TDO, and TRST). There is an internal weak pull-up resistor on the TMS pin. M3_SWDIO: Serial Wire Debug data input/output
JTAG_TRSTB / M3_TRSTB		1	Boundary scan reset pin. The TRST pin functions as an active low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor (1 k) could be included to ensure the TAP is held in Reset mode. In critical applications, an upset in the JTAG circuit could allow entering an undesired JTAG state. In such cases, Microsemi recommends that you tie off TRST to GND through a resistor (1 k) placed close to the FPGA pin. The TRSTB pin also resets the serial wire JTAG debug port (SWJ-DP) circuitry within the Cortex-M3 processor.

Programming SPI

The system controller contains a dedicated SPI block for programming. The SPI is operated in either Master or Slave mode. In Master mode, the SmartFusion2 device is interfaced with an external SPI flash device and the programming data is downloaded from it to the FPGA. In Slave mode, it is communicated with a remote device that initiates download of the programming data to the FPGA.

Table 8 • **Programming SPI Interface**

Name	Type	Description
SC_SPI_SS	Out	SPI slave select
SC_SPI_SDO	Out	SPI data output
SC_SPI_SDI	In	SPI data input
SC_SPI_CLK	Out	SPI clock
FLASH_GOLDEN_N	In	If pulled Low, this indicates that the device is to be re-programmed from an image in the external SPI flash attached to the SPI interface. If pulled High, the SPI is put into slave mode. Add an external pull-up resistor value of 10 kΩ to VDDI (Bank).

Notes:

1. *If unused, SPI programming pins must be left floating.*
2. *For more details related to reset, clock, and programming, refer to the AC393: SmartFusion2 SoC FPGA and IGLOO2 FPGA Board Design Guidelines Application Note.*
3. *For more information on remaining programming modes, refer to the UG0451: SmartFusion2 SoC FPGA and IGLOO2FPGA Programming User Guide.*

Dedicated I/Os

Dedicated I/Os (Table 9 and Table 10 on page 38) can be used for a single purpose such as SERDES, device reset, or clock functions. SmartFusion2 dedicated I/Os:

- Device reset pins
- Crystal oscillator pins
- SERDES I/Os
- Programming SPI pins

Table 9 • **Device Reset and Crystal Oscillator Pin Types and Descriptions**

Pin	Type	Description
Device Reset I/Os		
DEVRST_N	Input	Device reset; active Low and powered by VPP. It is an asynchronous signal and Schmitt trigger input with the maximum slew rate must not exceed 1 µs. When DEVRST_N is asserted, all user IOs are fully tri-stated. In unused condition, pull up to VPP through 10 kΩ resistor.
Crystal Oscillator I/Os[1, 2]		
XTLOSC_[MAIN/AUX]_EXTAL	Input	Crystal connection or external RC network.
XTLOSC_[MAIN/AUX]_XTAL	Input	Input clock from the main/auxiliary crystal oscillator

Notes:

1. *The M2S050 device has only a main crystal oscillator.*
2. *Crystal oscillator pins have a nominal 50 kΩ internal weak pull-ups to VPP. If unused, those pins can be left floating (DNC). The pins should not be grounded (VSS).*

SERDES I/Os

The SERDES I/Os available in SmartFusion2 devices are dedicated for high speed serial communication protocols. The SERDES I/Os support protocols such as PCI Express 2.0, XAUI, serial gigabit media independent interface (SGMII), serial rapid IO (SRIO), and any user-defined high speed serial protocol implementation in fabric. Refer to the *AC393: SmartFusion2 SoC FPGA and IGLOO2 FPGA Board Design Guidelines Application Note* for further information.

***Table 10* • SERDES I/O Port Names and Descriptions**

Port Name	Type	Description
Data / Reference Pads		
SERDES_x_RXD0_P	Input[1]	Receive data. SERDES differential positive input for each lane. Each SERDESIF consists of 4 RX signals. Here x = 0 for SERDESIF_0 and x = 1 for SERDESIF_1.
SERDES_x_RXD1_P		
SERDES_x_RXD2_P		
SERDES_x_RXD3_P		
SERDES_x_RXD0_N	Input[1]	Receive data. SERDES differential negative input for each lane. Each SERDESIF consists of 4 RX signals. Here x = 0 for SERDESIF_0 and x = 1 for SERDESIF_1.
SERDES_x_RXD1_N		
SERDES_x_RXD2_N		
SERDES_x_RXD3_N		
SERDES_x_TXD0_P	Output[2]	Transmit data. SERDES differential positive output for each lane. Each SERDESIF consists of 4 TX signals. Here x = 0 for SERDESIF_0 and x = 1 for SERDESIF_1.
SERDES_x_TXD1_P		
SERDES_x_TXD2_P		
SERDES_x_TXD3_P		
SERDES_x_TXD0_N	Output[2]	Transmit data. SERDES differential negative output for each lane. Each SERDESIF consists of 4 TX signals. Here x = 0 for SERDESIF_0 and x = 1 for SERDESIF_1.
SERDES_x_TXD1_N		
SERDES_x_TXD2_N		
SERDES_x_TXD3_N		
Common I/O Pads per SERDES Interface		
SERDES_x_L01_REXT	Reference[2]	External reference resistor connection to calibrate TX/RX termination value. Each SERDESIF consists of 2 REXT signals—one for Lane0 and Lane1, and another for Lane2 and Lane3. Here x = 0 for SERDESIF_0 and x = 1 for SERDESIF_1.
SERDES_x_L23_REXT		
SERDES_x_REFCLK0_P	Clock[3]	Reference clock differential positive. Each SERDESIF consists of two signals (REFCLK0_P, REFCLK1_P). Here x = 0 for SERDESIF_0 and x = 1 for SERDESIF_1.
SERDES_x_REFCLK1_P		
SERDES_x_REFCLK0_N	Clock[3]	Reference clock differential negative. Each SERDESIF consists of two signals (REFCLK0_P, REFCLK1_P). Here x = 0 for SERDESIF_0 and x = 1 for SERDESIF_1.
SERDES_x_REFCLK1_N		

Notes:

1. *If unused, must always connect to VSS (ground).*
2. *If the SERDES unit is not being used, these pins must remain floating (DNC).*
3. *These pins are MUXed with MSIOD functionality. If SERDES functionality and MSIOD functionality are not used, the pins must be left floating. Libero SoC will disable unused I/Os and weakly pull them up.*

Special Pins

The two live probe I/O cells are dual-purpose. If live probe functionality will never be used on these I/Os, the user can configure the I/O as an input, output, or bidirectional. However, if the intent is to perform live switching between the user I/O and probe functionality, then use the I/O only as an output. If it were configured as an input during general use, then as soon as it is switched over to live probe operation, the probe circuitry would drive out onto this I/O, potentially causing device damage.

Table 11 • **Special Pins**

Name	Type	Description
PROBE_A	In/out	The two live probe I/O cells are dual-purpose: 1. Live probe functionality 2. User I/O
PROBE_B	In/out	
CCC_xyz_CLKI0	Input	Input clock from dedicated input pad 0. The xy portion refers to the CCC location (NE, SW, SE, or NW) and z represents the CCC number (0 or 1).
CCC_xyz_CLKI1	Input	Input clock from dedicated input pad 1. The xy portion refers to the CCC location (NE, SW, SE, or NW) and z represents the CCC number (0 or 1).
CCC_xyz_CLKI2	Input	Input clock from dedicated input pad 2. The xy portion refers to the CCC location (NE, SW, SE, or NW) and z represents the CCC number (0 or 1).
CCC_xyz_CLKI3	Input	Input clock from dedicated input pad 3. The xy portion refers to the CCC location (NE, SW, SE, or NW) and z represents the CCC number (0 or 1).
GBx	Input	GB is a multiplexer that generates an independent global signal. The GBs can be driven from multiple sources such as dedicated global I/Os, fabric CCCs, VCCCs, and fabric routing
xDDR_TMATCH_[0/1]_IN	Input	DQS enable input for timing match between DQS and system clock. TMATCH_IN and TMATCH_OUT pins need to be looped back with the trace length as short as possible.
xDDR_TMATCH_[0/1]_OUT	Output	DQS enable output for timing match between DQS and system clock.
DNC	–	Do not connect. This pin should not be connected to any signals on the PCB; leave this pin unconnected.
NC	–	No connect This pin is not connected to circuitry within the device. This pin can be driven to any voltage or can be left floating with no effect on the operation of the device.

Input Only Pins

These pins are differentially paired with Flash_golden_n (input only pin) and are input only when used to connect to the FPGA fabric. These pins can be used as output for the listed MSS peripherals.

Table 12 • **Input Only Pins**

Device	Pin	Description
M2S050T-FG896	H27	MSI46NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI46NB1 is an input only pin.
M2S090T-FG676	D23	MSI59NB2/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI59NB2 is an input only pin.
M2S090T-FG484	D21	MSI59NB2/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI59NB2 is an input only pin.
M2S060T-FG484	D21	MSI47NB2/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI47NB2 is an input only pin.
M2S050T-FG484	D21	MSI46NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI46NB1 is an input only pin.
M2S025T-FG484	D21	MSI32NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI32NB1 is an input only pin.
M2S010T-FG484	D21	MSI26NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI32NB1 is an input only pin.
M2S005-FG484	D21	MSI16NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI16NB1 is an input only pin.
M2S050T-VF400	D18	MSI46NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI46NB1 is an input only pin.
M2S025T-VF400	D18	MSI32NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI32NB1 is an input only pin.
M2S010T-VF400	D18	MSI26NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI26NB1 is an input only pin.
M2S005-VF400	D18	MSI16NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI16NB1 is an input only pin.
M2S025T-VF256	G12	MSI26NB1/MMUART_0_TXD/GPIO_27_B, cannot be configured as differential. The function MSI26NB1 is an input only pin.

***Table 12* • Input Only Pins (continued)**

Device	Pin	Description
M2S010T-VF256	G12	MSI26NB1/MMUART_0_TXD/GPIO_27_B, cannot be configured as differential. The function MSI26NB1 is an input only pin.
M2S005-VF256	D12	MSI16NB1/MMUART_0_TXD/GPIO_27_B, cannot be configured as differential. The function MSI16NB1 is an input only pin.

Microcontroller Subsystem (MSS)

***Table 13* • MSS Pin Names and Descriptions**

Name	Type	Description
Inter-Integrated Circuit (I^2C) Peripherals		
I2C_0_SCL	In/out	I^2C bus serial clock output.
I2C_0_SDA	In/out	I^2C bus serial data input/output.
I2C_1_SCL	In/out	I^2C bus serial clock output.
I2C_1_SDA	In/out	I^2C bus serial data input/output.
Universal Asynchronous Receiver/Transmitter (UART) Peripherals		
MMUART_0_CLK	Out	UART clock.
MMUART_0_TXD	Out	UART transmit data.
MMUART_0_RXD	In	UART receive data.
MMUART_0_CTS	In	UART clear to send.
MMUART_0_RTS	Out	UART request to send.
MMUART_0_DTR	Out	Modem data terminal ready.
MMUART_0_DCD	In	Modem data carrier detects.
MMUART_0_DSR	In	Modem data set ready.
MMUART_0_RI	In	Modem ring indicator.
MMUART_1_CLK	Out	UART Clock.
MMUART_1_TXD	Out	UART transmit data.
MMUART_1_RXD	In	UART receive data.
MMUART_1_CTS	In	UART clear to send.
MMUART_1_RTS	Out	UART request to send.
MMUART_1_DTR	Out	Modem data terminal ready.
MMUART_1_DCD	In	Modem data carrier detects.
MMUART_1_DSR	In	Modem data set ready.
MMUART_1_RI	In	Modem ring indicator.
Serial Peripheral Interface (SPI) Controllers		
SPI_0_SS0	Out	SPI slave select0.
SPI_0_SS1	Out	SPI slave select1.
SPI_0_SS2	Out	SPI slave select2.
SPI_0_SS3	Out	SPI slave select3.
SPI_0_SS4	Out	SPI slave select4.
SPI_0_SS5	Out	SPI slave select5.
SPI_0_SS6	Out	SPI slave select6.
SPI_0_SS7	Out	SPI slave select7.
SPI_0_CLK	Out	SPI clock.

Table 13 • **MSS Pin Names and Descriptions (continued)**

Name	Type	Description
SPI_0_SDO	Out	SPI data output.
SPI_0_SDI	In	SPI data input.
SPI_1_SS0	Out	SPI slave select0.
SPI_1_SS1	Out	SPI slave select1.
SPI_1_SS2	Out	SPI slave select2.
SPI_1_SS3	Out	SPI slave select3.
SPI_1_SS4	Out	SPI slave select4.
SPI_1_SS5	Out	SPI slave select5.
SPI_1_SS6	Out	SPI slave select6.
SPI_1_SS7	Out	SPI slave select7.
SPI_1_CLK	Out	SPI clock.
SPI_1_SDO	Out	SPI data output.
SPI_1_SDI	In	SPI data input.

Note: All the pins can also be used as Fabric I/Os as all MSS pins are muxed with Fabric I/Os.

I/O Programmable Features

SmartFusion2 devices support different I/O programmable features for MSIO, MSIOD, and DDRIO. Each I/O pair (P, N) supports the following programmable features:

- Programmable drive strength
- Programmable weak pull-up and pull-down
- Configurable ODT and driver impedance
- Programmable input delay
- Programmable Schmitt input and receiver

For more information on SmartFusion2 I/O programmable features, refer to the "SmartFusion2 I/O Features" table of the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide*.

Packaging Information

FC1152

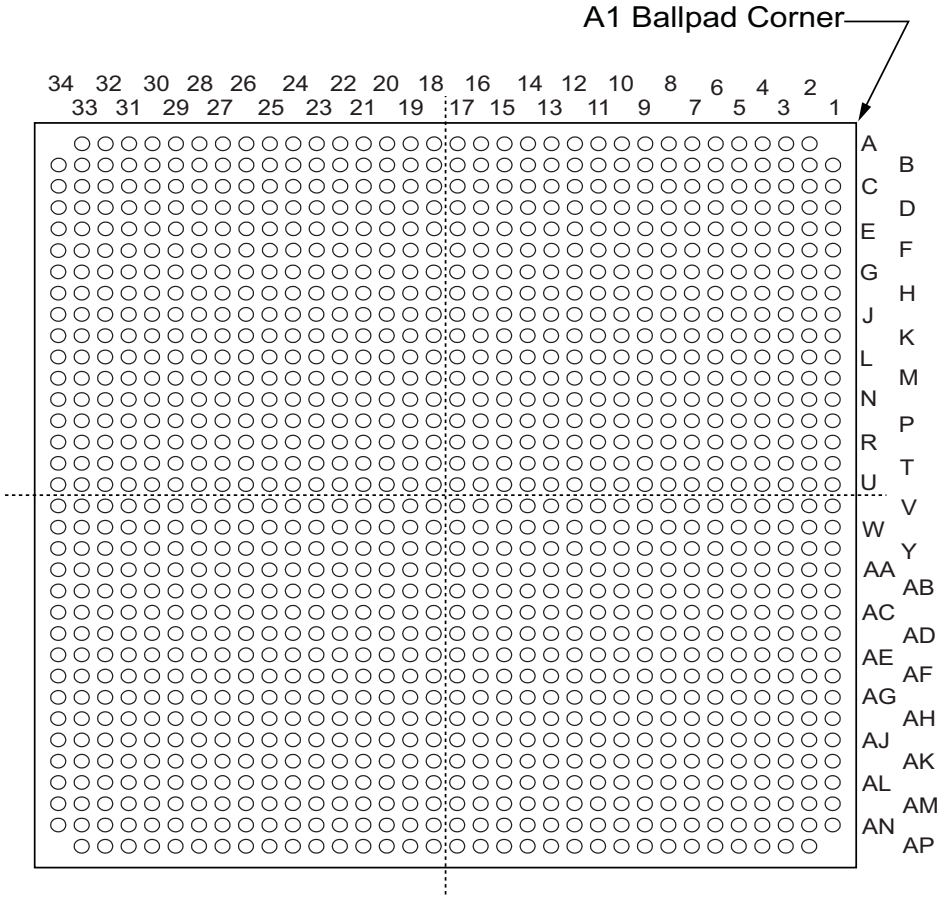


***Figure 28* • FC1152 Package Drawing**

Note

For Package Manufacturing and Environmental information, visit the Resource Center at *Packaging Resource Center*.

Pin Tables

Pin tables for the FC1152 package depicted in Figure 28 are found in the Excel® spreadsheet located here: *http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=132128*

The following devices are available in the FC1152:

M2S150(T), (TS)

FG896

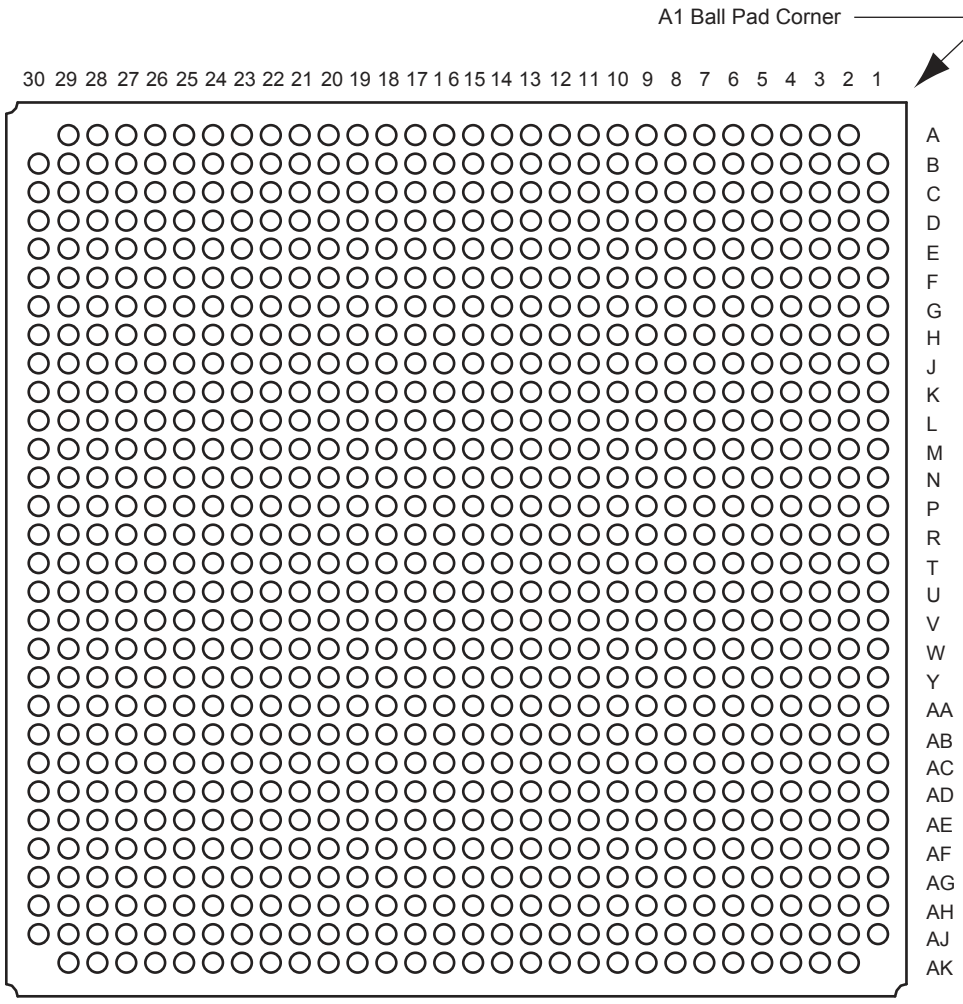


Figure 29 • **FG896 Package Drawing**

Note

For Package Manufacturing and Environmental information, visit the Resource Center at *Packaging Resource Center*.

Pin Tables

Pin tables for the FG896 package depicted in Figure 29 are found in the Excel spreadsheet located here:

http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=131803

The following devices are available in the FG896:

M2S050(T), (TS)

FG676

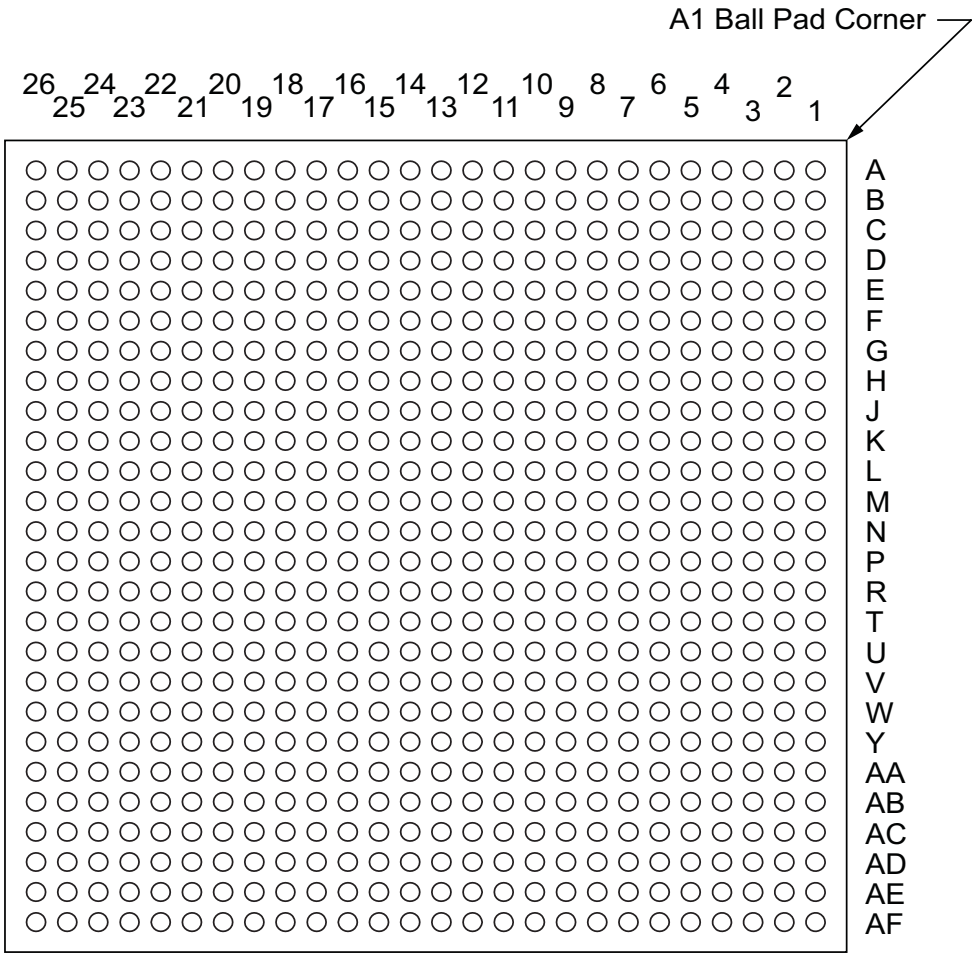


***Figure 30* • FG676 Package Drawing**

Note

For Package Manufacturing and Environmental information, visit the Resource Center at *Packaging Resource Center*.

Pin Tables

Pin tables for the FG676 package depicted in Figure 30 are found in the Excel® spreadsheet located here: *http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=132535*

The following devices are available in the FG676:

M2S090(T), (TS)

FG484

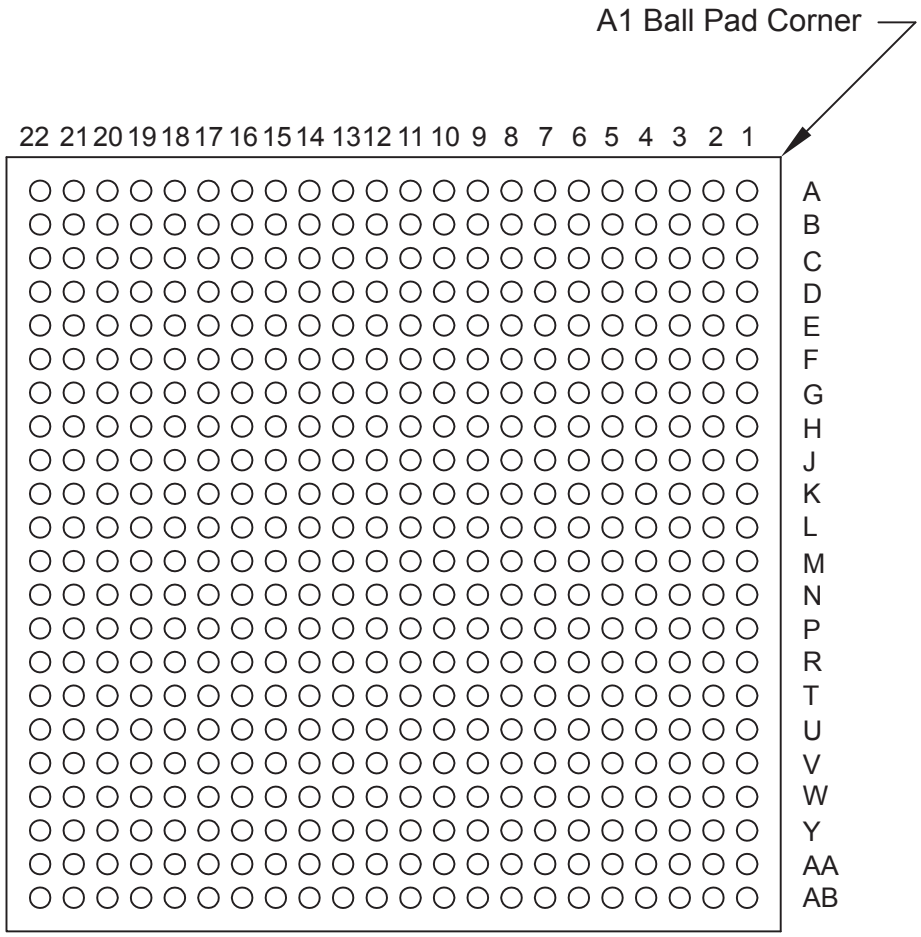


***Figure 31* • FG484 Package Drawing**

Note

For Package Manufacturing and Environmental information, visit the Resource Center at *Packaging Resource Center*.

Pin Tables

Pin tables for the FG484 package depicted in Figure 31 are found in the Excel® spreadsheet located here: *http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=131802*

The following devices are available in the FG484:

M2S005(S)

M2S010(T), (TS)

M2S025(T), (TS)

M2S050(T), (TS)

M2S060(T), (TS)

M2S090(T), (TS)

VF400

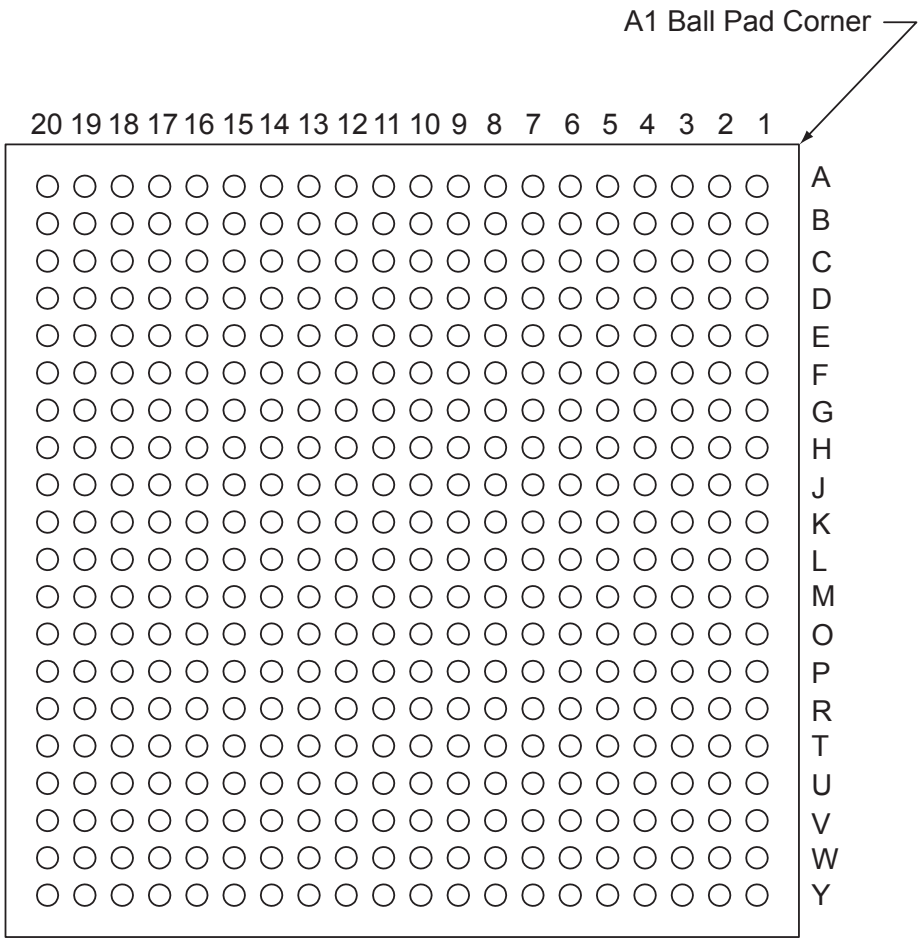


***Figure 32* • VF400 Package Drawing**

Note

For Package Manufacturing and Environmental information, visit the Resource Center at *Packaging Resource Center*.

Pin Tables

Pin tables for the VF400 package depicted in Figure 32 are found in the Excel spreadsheet located here:

http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=131805

The following devices are available in the VF400:

M2S005(S)

M2S010(T), (TS)

M2S025(T), (TS)

M2S050(T), (TS)

FCS325

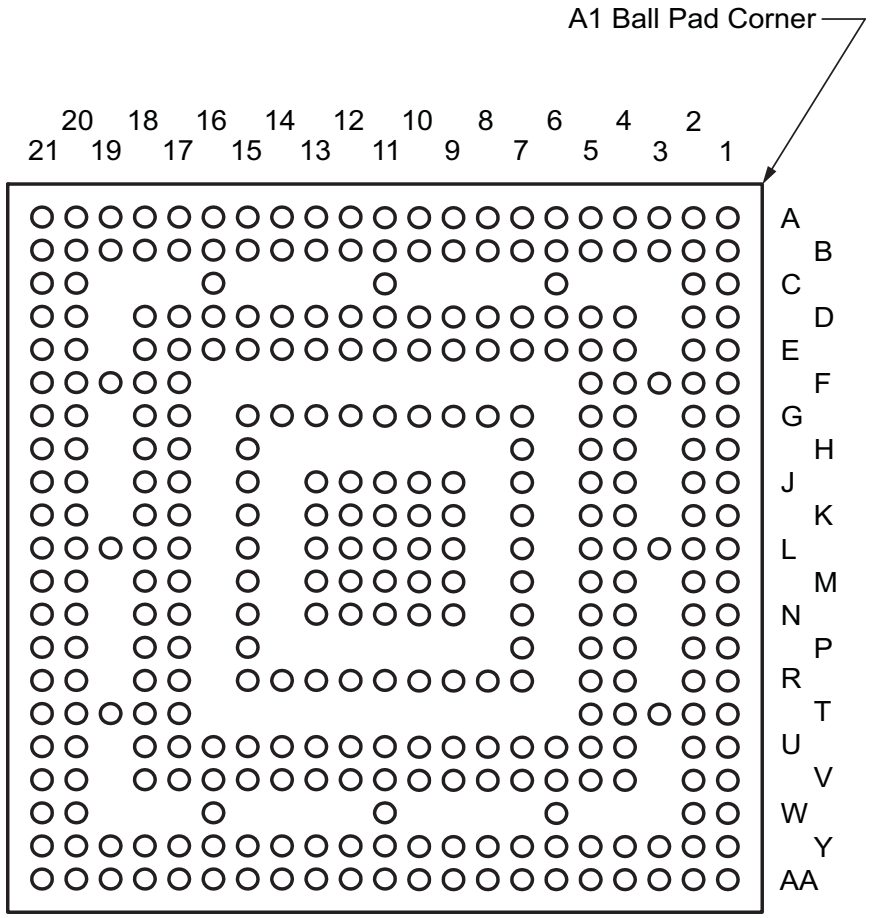


Figure 33 • **FCS325 Package Drawing**

Note

For Package Manufacturing and Environmental information, visit the Resource Center at *Packaging Resource Center*.

Pin Tables

Pin tables for the FCS325 package depicted in Figure 33 are found in the Excel® spreadsheet located here: *http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=132603*

The following devices are available in the FCS325:

M2S050(T), (TS)

VF256

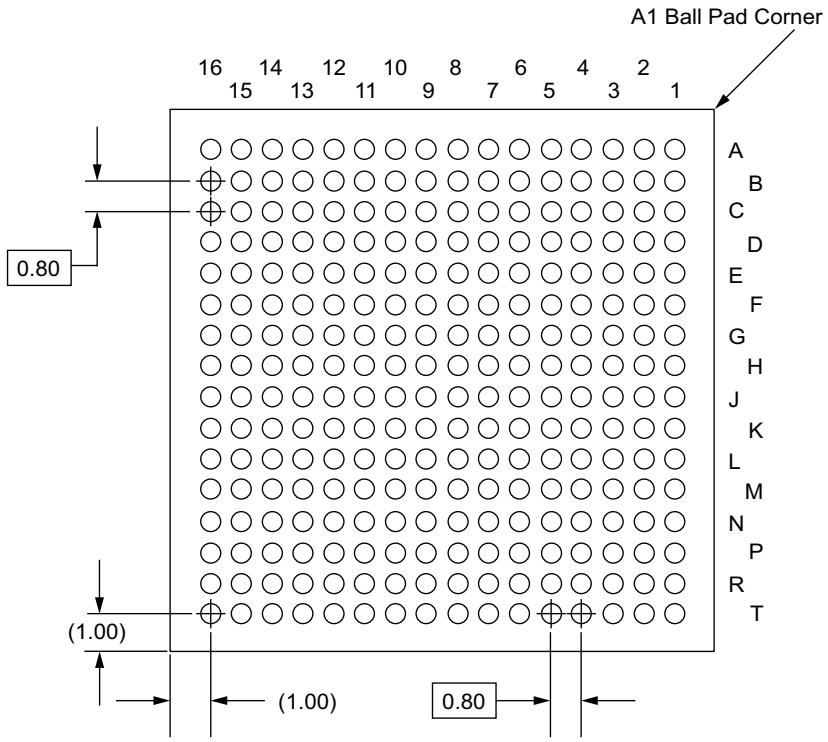


Figure 34 • **VF256 Package Drawing**

Note

For Package Manufacturing and Environmental information, visit the Resource Center at *Packaging Resource Center*.

Pin Tables

Pin tables for the VF256 package depicted in Figure 34 are found in the Excel® spreadsheet located here: *http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=133773*

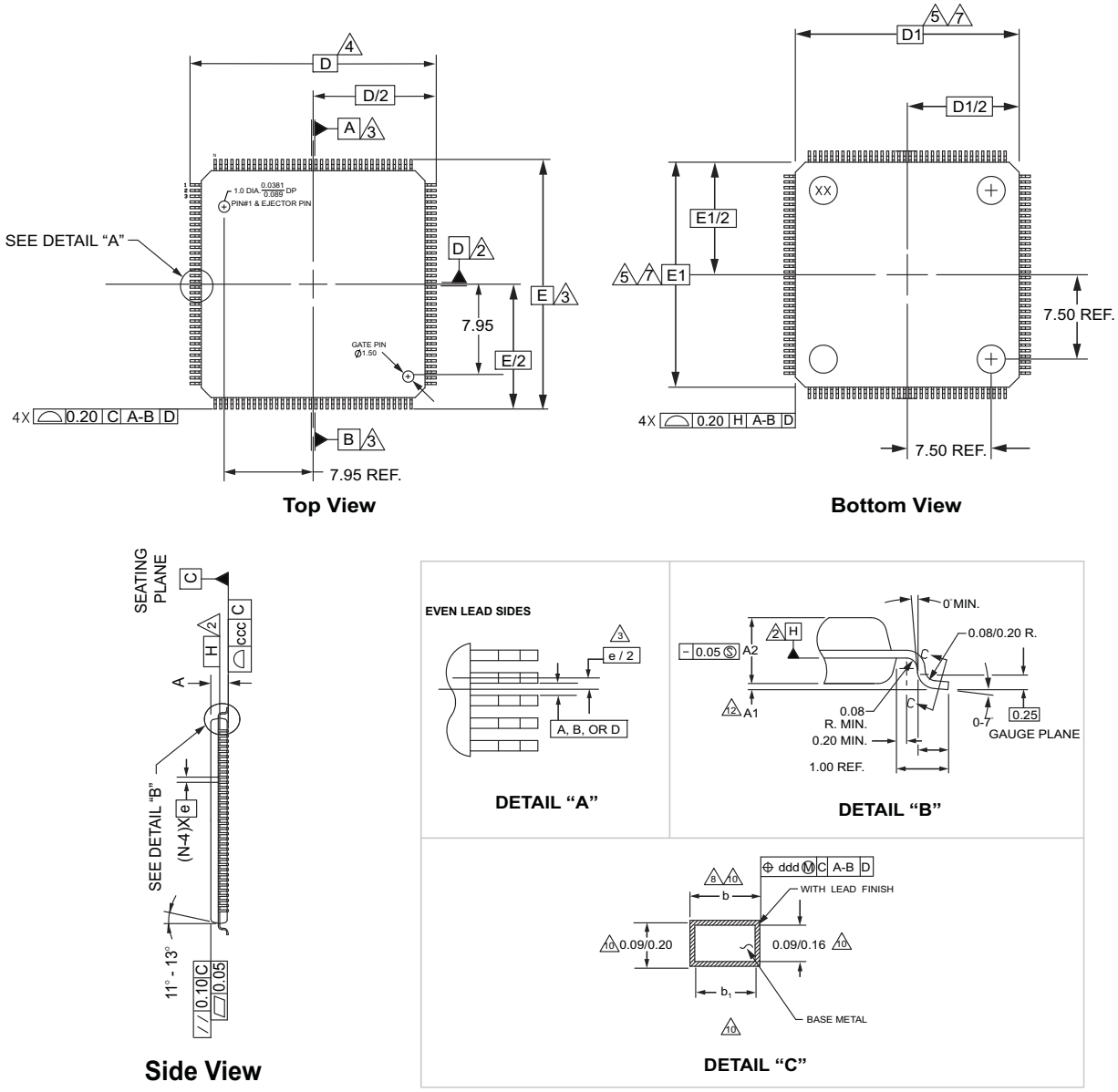
The following devices are available in the VF256:

M2S005(S)

M2S010(T), (TS)

M2S025(T), (TS)

TQ144



NOTES: UNLESS OTHERWISE SPECIFIED

1. *All dimensioning and tolerances confirm to ASME Y14.5-1994.*
2. *Datum plane **H** located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.*
3. *Datums **A-B** and **D** to be determined at centerline between leads where leads exit plastic body at datum plane **H**.*
4. *To be determined at seating plane **C**.*
5. *Dimensions **D1** and **E1** do not include mold protrusion. Allowable mold protrusion is 0.254 mm per side. Dimension **D1** and **E1** include mold mismatch and are determined at datum plane **H**.*
6. *N is number of terminals.*
7. *Package top dimensions are smaller than bottom dimensions by 0.10 millimeters and top of package will not overhang bottom of package.*
8. *Dimension **b** does not include damber protrusion. Allowable damber protrusion shall be not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Damber can not be located on the lower radius or the foot.*
9. *All dimensions are in millimeters.*
10. *These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.*
11. *This drawing conforms to JEDEC registered outline m2s-026-c, variation BFB.*
12. *A1 is defined as the distance from the seating plane to the lowest point of the package body.*

***Figure 35* • TQ144 Package Drawing**

Note: For Package Manufacturing and Environmental information, visit the Resource Center at *Packaging Resource Center*.

Pin Tables

Pin tables for the TQ144 package depicted in Figure 35 on page 51 are found in the Excel® spreadsheet located here: *http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=133134*

The following devices are available in the TQ144:

M2S010
M2S005 (S)

List of Changes

The following table shows important changes made in this document for each revision.

Revision	Changes	Page
Revision 10 (December 2015)	Added Figure 19 • SmartFusion2 M2S060-FCS325 I/O Bank Locations. (SAR 74266)	18
	Added "MDDR/FDDR Interface" section (SAR 69579)	31
Revision 9 (July 2015)	Added Figure 7 • SmartFusion2 M2S060TS/M2S060T/M2S060-FG484 I/O Bank Locations (SAR 67177).	7
	Updated Table 1 • Organization of I/O Banks in SmartFusion2 Devices - FC1152, FCS536, FCV484, FG896, FG676, and FG484.	26
	Added Figure 27 • Internal Clamp Diode Control Circuitry.	29
	Updated Table 4 • Reference Resistors (SAR 67026).	30
	Updated "Programming SPI" section (SAR 66178).	37
	Updated "Supply Pins" section (SAR 66040).	33
	Updated Table 12 • Input Only Pins.	40
Revision 8 (January 2015)	Added Figure 4 • SmartFusion2 M2S060TS/ M2S060T/M2S060-FG676 I/O Bank Locations.	4
	Added Figure 5 • SmartFusion2 M2S150TS/M2S150T/M2S150-FCS536 I/O Bank Locations.	5
	Added Figure 11 • SmartFusion2 M2S150TS/M2S150T/M2S150-FCV484 I/O Bank Locations.	12
	Added Figure 12 • SmartFusion2 M2S060TS/M2S060T/M2S060-VF400 I/O Bank Locations.	13
	Removed all instances of and references to M2S100 device from Table 1 • Organization of I/O Banks in SmartFusion2 Devices - FC1152, FCS536, FCV484, FG896, FG676, and FG484 (SAR 62858).	26
	Replaced VQ144 with TQ 144 from Table 2 • Organization of I/O Banks in SmartFusion2 Devices - VF400, FCS325, VF256, and TQ144.	28
	Removed GPIO or USB_DIR_C from Table 13.	42

Revision	Changes	Page
Revision 7 (June 2014)	Updated Notes for Bank Location figures (SAR 56735).	NA
	Added new Figure 28 • SmartFusion2 M2S010TS/M2S010T/M2S010-VF256 I/O Bank Locations, Figure 29 • SmartFusion2 M2S005S/M2S005-VF256 I/O Bank Locations, Figure 30 • SmartFusion2 M2S010-TQ144 I/O Bank Locations, and Figure 31 • SmartFusion2 M2S005S/M2S005-TQ144 I/O Bank Locations (SAR 58291).	27, 28, 29, and 30
	Modified Table 1 • Organization of I/O Banks in SmartFusion2 Devices - FC1152, FCS536, FCV484, FG896, FG676, and FG484 by moving VF400 and FCS 325 devices to Table 2 • Organization of I/O Banks in SmartFusion2 Devices - VF400, FCS325, VF256, and TQ144 (SAR 58291).	26
	Added VF256 and VQ144 devices to Table 2 • Organization of I/O Banks in SmartFusion2 Devices - VF400, FCS325, VF256, and TQ144 (SAR 58291).	28
	Modified notes in Table 4 • Reference Resistors (SAR 58085).	30
	Modified notes in Table 6 • Supply Pins (SAR 56681).	33
	Modified Table 6 • Supply Pins by adding 'x' to supply pin names and deleting the individual pin names (SAR 58291).	33
	Added Table 12 • Input Only Pins (SAR 56733).	40
	Added Figure 34 • VF256 Package Drawing and Figure 35 • TQ144 Package Drawing (SAR 58291).	50 and 51
Revision 6 (March 2014)	Modified Notes for the following figures: Figure 1 • SmartFusion2 M2S150TS/M2S150T/M2S150-FC1152 I/O Bank Locations, Figure 2 • SmartFusion2 M2S050TS/M2S050T/M2S050-FG896 I/O Bank Locations, and Figure 6 • SmartFusion2 M2S090TS/M2S090T/M2S090-FG484 I/O Bank Locations (SAR 55001).	1, 2, and 4
	Figure 18 • SmartFusion2 M2S090TS/M2S090T/M2S090-FCS325 I/O Bank Locations, Figure 27 • SmartFusion2 M2S025TS/M2S025T/M2S025-VF256 I/O Bank Locations, and Figure 31 • SmartFusion2 M2S005S/M2S005-TQ144 I/O Bank Locations are new (SAR 55995).	17, 26, and 30
	Updated Table 1 • Organization of I/O Banks in SmartFusion2 Devices - FC1152, FCS536, FCV484, FG896, FG676, and FG484 for I/O types (SARs 55743 and 47532).	26
	Note added for VPP and VPPNVM for 090, 100, and 150 devices in Table 6 • Supply Pins for I/O types (SAR 55658).	33
	Added descriptions for TMATCH pins to Table 11 • Special Pins (SAR 54080).	39

Revision	Changes	Page
Revision 5 (January 2014)	Table 3 • User I/O Types was corrected to change LVDS to LVDS2V5 (SAR 47753).	29
	Updated description column in Table 3 • User I/O Types (SAR 48665). Also added a Note for default state of I/Os (SAR 53163)	29
	Updated description column for VREF0 and VREF5 in Table 6 • Supply Pins (SAR 47164). Also modified pin name from MDDR_PLL_VDDA to MSS_MDDR_PLL_VDDA (SAR 52457).	33
	Updated description column in Table 9 • Device Reset and Crystal Oscillator Pin Types and Descriptions for DEVRST_N (SARs 48158, 50803, and 50159).	37
	Updated the links (SAR 52241).	N/A
	Figure 1 • SmartFusion2 M2S150TS/M2S150T/M2S150-FC1152 I/O Bank Locations Figure 2 • SmartFusion2 M2S100TS/M2S100T-FC1152 I/O Bank Locations Figure 4 • SmartFusion2 M2S090TS/M2S090T-FG676 I/O Bank Locations Figure 10 • SmartFusion2 M2S005S/M2S005-FG484 I/O Bank Locations Figure 16 • SmartFusion2 M2S005S/M2S005-VF400 I/O Bank Locations Figure 18 • SmartFusion2 M2S050TS/M2S050T/M2S050-FCS325 I/O Bank Locations are new I/O Bank Location Figures for the FC1152, FG676, FG484, VF400, and FCS325 (SAR 52411).	1 2 4 6 17 18
	Figure 25 • FC1152 Package Drawing Figure 27 • FG676 Package Drawing Figure 30 • FCS325 Package Drawing are new package drawings for the FC1152, FG676 and FCS325 (SAR 52411).	44 46 49
	Figure 6 • SmartFusion2 M2S090TS/M2S090T/M2S090-FG484 I/O Bank Locations Figure 19 • SmartFusion2 M2S025TS/M2S025T/M2S025-FCS325 I/O Bank Locations are new I/O Bank Location Figures for the FG484 and FCS325 (SAR 52721).	4 – 18

Revision	Changes	Page
Revision 4 (June 2013)	Figure 11 • SmartFusion2 M2S150TS/M2S150T/M2S150-FCV484 I/O Bank Locations through Figure 15 • SmartFusion2 M2S010TS/M2S010T/M2S010-VF400 I/O Bank Locations are new for the VF400 package (SAR 47027).	6 – 16
	Updated Bank names in Table 1 • Organization of I/O Banks in SmartFusion2 Devices - FC1152, FCS536, FCV484, FG896, FG676, and FG484 (SAR 47532).	26
	VF400 was added to Table 1 • Organization of I/O Banks in SmartFusion2 Devices - FC1152, FCS536, FCV484, FG896, FG676, and FG484 (SAR 47027).	26
	Deleted incorrect references to 1.8 V from Table 4 • Reference Resistors (SAR 47736).	30
	Several table notes were revised in Table 6 • Supply Pins (SARs 47216 and 45299). Added recommendation for SERDES VDDAPLL supply when serdesif is unused (SAR 48490). Added VDD_2V5 as a supply with range 1.2 V to 2.5 V (SAR 48628).	33
	Updated the XTL pin names in Table 9 • Device Reset and Crystal Oscillator Pin Types and Descriptions (SAR 48302). Added description for DEVRST_N stating that "It is a dedicated I/O of type MSIO (3.3 V capable)" (SAR 48665).	37
	Table 11 • Special Pins was expanded to include additional pins (SAR 44597). Moved details for VDD_2V5 to Table 6 • Supply Pins (SAR 48628).	39
	Updated the Pin Table for the "FG484" package with M2S090 (SAR 48301).	47
	The "VF400" section is new (SAR 47027).	48
	The *Board Design Guidelines* application note has been released and references to it in this document are now hyperlinked to its location on the Microsemi website.	N/A
Revision 3 (February 2013)	The "SmartFusion2 Pin Descriptions" section has been separated from the rest of the SmartFusion2 datasheet and is now published separately. Pin tables have been removed from the document and replaced by links to sortable pin tables in an Excel spreadsheet. Pin tables for non-T devices are being reworked and will be included in a future release of the document (SAR 45184). The contents of the document have been reorganized (SAR 45275).	N/A
	Table 1 • Organization of I/O Banks in SmartFusion2 Devices - FC1152, FCS536, FCV484, FG896, FG676, and FG484 was corrected to change MSIOD to MSIO for bank 4 and bank 7, M2S010T and M2S025T devices on the FG484 package (SAR 45188).	26
	Notes were added to several tables giving instructions on how to handle pins if unused (SAR 45172): Table 4 • Reference Resistors Table 8 • Programming SPI Interface Table 9 • Device Reset and Crystal Oscillator Pin Types and Descriptions	 30 37 37
	The "Special Pins" section is new (SAR 44597).	39
	Connection information for some of the SERDES pins was clarified in the notes to Table 10 • SERDES I/O Port Names and Descriptions (SAR 45172).	38
Revision 2 (February 2013)	The document was revised extensively, including major changes to Table 6 • Supply Pins, new bank location diagrams, renaming of many pins and new pin tables for FG484 and FG896 (SARs 42905, 42497, 43861, 45081).	33

Revision	Changes	Page
Revision 1 (January 2013)	Table 6 • Supply Pins was revised to clarify instructions for unused pins (SAR 42435).	33
	Figure 1 • SmartFusion2 (M2S050T) I/O Bank Location and Naming was revised. The number of pairs in bank 1 was corrected to 10 (was 11) and the number of pairs in bank 3 was corrected to 23 (was 25). Table 2 • SmartFusion2 (M2S050T) I/O Bank Resource Usage is new (SAR 42412).	5
	Table 4 • Reference Resistors is new (SAR 42835).	30
	The description for the FLASH_GOLDEN pin in Table 8 • Programming SPI Interface was corrected to reverse the conditions for High and Low (SAR 42484).	37
	Table 10 • SERDES I/O Port Names and Descriptions was revised to clarify handling of pins with and without transceiver (SAR 42494).	38
	The "FG484" section is new, including pin tables for M2S010T, M2S025T, and M2S050T (SAR 42480).	47
Revision 0 (September 2012)	Initial Release.	N/A

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