PAC5532 Device User Guide

Power Application Controller®

Multi-Mode Power Manager™

Configurable Analog Front End™

Application Specific Power Drivers™

ARM® Cortex®-M4F Controller Core

www.active-semi.com

Rev 1.0

TABLE OF CONTENTS

1 OVERVIEW 11
2 STYLE AND FORMATTING CONVENTIONS 12
2.1 Number Representation 12
2.2 Formatting Styles 12
3 ARCHITECTURAL BLOCK DIAGRAM 13
4 ANALOG REGISTER ACCESS 14
4.1 Overview 14
4.2 Functional Description 14
4.3 USART Configuration 15
4.4 Protocol 15
4.5 Write Register Example 15
4.6 Read Register Example 17
5 PAC5532 IO 18
5.1 Overview 18
5.2 ADC Channels 19
5.3 Digital Peripheral Pins 20
6 CONFIGURABLE POWER MANAGER 22
6.1 Features 22
6.2 System Block Diagram 22
6.3 Functional Description 22
6.4 Register Summary 23
6.5 Register Detail 24
6.5.1 SOC.FAULT 24
6.5.2 SOC.STATUS 25
6.5.3 SOC.MISC 26
6.5.4 SOC.PWRCTL 27
6.5.5 SOC.FAULTMASK 28
6.5.6 SOC.WATCHDOG 29
6.5.7 SOC.SYSCONF 30

7 CONFIGURABLE ANALOG FRONT-END 31
7.1 Overview 31
7.2 Features 31
7.3 System Block Diagram 32
7.4 Functional Description 33
7.4.1 Enabling the CAFE 33
7.4.2 Integrated Temperature Sensor 33
7.5 AIO10 34
7.5.1 System Block Diagram 34
7.5.2 AIO1, AIO0 34
7.5.3 AIO1, AIO0 digital I/O Mode 34
7.5.4 AIO1, AIO0 differential Amplifier Mode 35
7.5.5 AIO1, AIO0 Protection 35
7.6 AIO32 37
7.6.1 System Block Diagram 37
7.6.2 AIO3, AIO2 37
7.6.3 AIO3, AIO2 digital I/O Mode 37
7.6.4 AIO3, AIO2 differential Amplifier Mode 38
7.6.5 AIO3, AIO2 Protection 38
7.7 AIO54 40
7.7.1 System Block Diagram 40
7.7.2 AIO5, AIO4 40
7.7.3 AIO5, AIO4 digital I/O Mode 40
7.7.4 AIO5, AIO4 differential Amplifier Mode 41
7.7.5 AIO5, AIO4 Protection 41
7.8 AIO6 43
7.8.1 System Block Diagram 43
7.8.2 AIO6 44
7.8.3 AIO6 digital I/O Mode 44
7.8.4 AIO6 Single Ended Amplifier Mode 44
7.8.5 AIO6 Comparator Mode 44
7.8.6 AIO6 Special Mode 45

7.8.7 AIO6 Push Button Mode 45
7.9 AIO7 47
7.9.1 System Block Diagram....47
7.9.2 AIO7 48
7.9.3 AIO7 digital I/O Mode....48
7.9.4 1.1.4. AIO7 Single Ended Amplifier Mode 48
7.9.5 1.1.5. AIO7 Comparator Mode 48
7.9.6 AIO7 Special Mode 49
7.10 AIO8 51
7.10.1 System Block Diagram....51
7.10.2 AIO8 52
7.10.3 AIO8 digital I/O Mode....52
7.10.4 AIO8 Single Ended Amplifier Mode 52
7.10.5 AIO8 Comparator Mode 52
7.10.6 AIO8 Special Mode 53
7.11 AIO9 55
7.11.1 System Block Diagram....55
7.11.2 AIO9 56
7.11.3 AIO9 digital I/O Mode....56
7.11.4 AIO9 Single Ended Amplifier Mode 56
7.11.5 AIO9 Comparator Mode 56
7.11.6 AIO9 Special Mode 57
7.12 EMUX and ADMUX....59
7.12.1 System Block Diagram....59
7.12.2 EMUX 59
7.12.3 EMUX Enable 59
7.12.4 EMUXD Packet Structure....59
7.12.5 ADMUX....61
7.13 Register Summary 62
7.14 Register Detail 63
7.14.1 SOC.CFGAIO0 63
7.14.2 SOC.CFGAIO1 64

7.14.3 SOC.CFGAIO2 65
7.14.4 SOC.CFGAIO3 66
7.14.5 SOC.CFGAIO4 67
7.14.6 SOC.CFGAIO5 68
7.14.7 SOC.CFGAIO6 69
7.14.8 SOC.CFGAIO7 70
7.14.9 SOC.CFGAIO8 71
7.14.10 SOC.CFGAIO9 72
7.14.11 SOC.SIGSET 73
7.14.12 SOC.HPDACH 74
7.14.13 SOC.HPDACL 74
7.14.14 SOC.LPDACH 74
7.14.15 SOC.LPDACL 74
7.14.16 SOC.SHCFG1 75
7.14.17 SOC.SHCFG2 76
7.14.18 SOC.PROTINTM 77
7.14.19 SOC.PROTSTAT 78
7.14.20 SOC.DOUTSIG0 79
7.14.21 SOC.DOUTSIG1 80
7.14.22 SOC.DINSIG0 81
7.14.23 SOC.DINSIG1 81
7.14.24 SOC.CFGIO1 82
7.14.25 SOC.CFGIO2 82
7.14.26 SOC.SIGINTM 83
7.14.27 SOC.SIGINTF 84
7.14.28 SOC.BLANKING 85
7.14.30 SOC.SPECCFG0 86
7.14.31 SOC.SPECCFG1 87
7.14.32 SOC.SPECCFG2 89
7.14.33 SOC.SPECCFG3 89
8 APPLICATION SPECIFIC POWER DRIVER 90
8.1 Overview 90

8.2 Features 90
8.3 System Block Diagram 90
8.4 Functional Description 91
8.4.1 Enabling the ASPD 91
8.4.2 Low-Side Gate Drivers 91
8.4.3 1.2.5. High-Side Gate Drivers 91
8.4.4 1.2.6. Driver Protection 91
8.4.5 1.2.7. PWM Input Signal Swap 91
8.4.6 1.2.8. Cycle by Cycle Current Limit 92
8.4.7 Break Before Make (BBM) 94
8.5 Register Summary 95
8.6 Register Detail 96
8.6.1 SOC.CFGDRV0 96
8.6.2 SOC.CFGDRV1 97
8.6.3 SOC.CFGDRV2 98
8.6.4 SOC.CFGDRV3 99
8.6.6 SOC.STATDRV 100
8.6.7 SOC.ENDRV 101
8.6.8 SOC.WDTPASS 101
9 LEGAL INFORMATION 102

LIST OF FIGURES

Figure 3-1 PAC5532 Architectural Block Diagram 13
Figure 4-1 PAC5532 Register Access 14
Figure 4-2 Analog Peripheral Register Write Timing 16
Figure 4-3 Analog Peripheral Register Read Timing 17
Figure 5-1 GPIO and DPM Block Diagram 18
Figure 6-1 CPM System Block Diagram 22
Figure 7-1 CAFE System Block Diagram 32
Figure 7-2 AIO10 Block Diagram 34
Figure 7-3 AIO32 Block Diagram 37
Figure 7-4 AIO54 Block Diagram 40
Figure 7-5 AIO6 System Block Diagram 43
Figure 7-6 AIO7 System Block Diagram 47
Figure 7-7 AIO8 System Block Diagram 51
Figure 7-8 AIO9 System Block Diagram 55
Figure 7-9 EMUX and ADMUX System Block Diagram 59
Figure 7-10 EMUX Timing Diagram 60
Figure 8-1 ASPD System Block Diagram 90
Figure 8-2 Cycle by Cycle Current Limit 92

LIST OF TABLES

Table 5-1 PAC5532 ADC Input Pins 19
Table 5-2 PAC5532 Digital Peripheral Pins.....20
Table 6-1 CPM Register Summary.....23
Table 7-1 EMUX Message Format.....59
Table 7-2 CAFE Register Summary.....62
Table 8-1 ASPD Register Summary.....95

LIST OF REGISTERS

Register 6-1 SOC.FAULT (Fault Condition, 00h) 24
Register 6-2 SOC.STATUS (System Status, 01h) 25
Register 6-3 SOC.MISC (SOC Miscellaneous Configuration, 02h) 26
Register 6-4 SOC.PWRCTL (Power Control, 03h) 27
Register 6-5 SOC.FAULTMASK (Fault mask, 04h) 28
Register 6-6 SOC.WATCHDOG (SOC Watchdog Configuration, 05h) 29
Register 6-7 SOC.SYSCONF (System Configuration, 2Bh) 30
Register 7-1 SOC.CFGAIO0 (AIO0 Configuration, 06h) 63
Register 7-2 SOC.CFGAIO1 (AIO1 Configuration, 07h) 64
Register 7-3 SOC.CFGAIO2 (AIO2 Configuration, 08h) 65
Register 7-4 SOC.CFGAIO3 (AIO3 Configuration, 09h) 66
Register 7-5 SOC.CFGAIO4 (AIO4 Configuration, 0Ah) 67
Register 7-6 SOC.CFGAIO5 (AIO5 Configuration, 0Bh) 68
Register 7-7 SOC.CFGAIO6 (AIO6 Configuration, 0Ch) 69
Register 7-8 SOC.CFGAIO7 (AIO7 Configuration, 0Dh) 70
Register 7-9 SOC.CFGAIO8 (AIO8 Configuration, 0Eh) 71
Register 7-10 SOC.CFGAIO9 (AIO9 Configuration, 0Fh) 72
Register 7-11 SOC.SIGSET (Signal Manager Configuration, 10h) 73
Register 7-12 SOC.HPDACH (HPDAC High Setting, 11h) 74
Register 7-13 SOC.HPDACL (HPDAC Low Setting, 12h) 74
Register 7-14 SOC.LPDACH (LPDAC High Setting, 13h) 74
Register 7-15 SOC.LPDAC1 (LPDAC Low Setting, 14h) 74
Register 7-16 SOC.SHCFG1 (Sample and Hold Configuration, 15h) 75
Register 7-17 SOC.SHCFG2 (Sample and Hold Configuration 2, 16h) 76
Register 7-18 SOC.PROTINTM (Protection Interrupt Mask, 17h) 77
Register 7-19 SOC.PROTSTAT (Protection Interrupt Status, 18h) 78
Register 7-20 SOC.DOUTSIG0 (Digital Output 0, 19h) 79
Register 7-21 SOC.DOUTSIG1 (Digital Output 1,1Ah) 80
Register 7-22 SOC.DINSIG0 (Digital Input 0, 1Bh) 81
Register 7-23 SOC.DINSIG1 (Digital Input 1, 1Ch) 81
Register 7-24 SOC.CFGIO1 (AIO10-AIO13 Configuration 1, 1Dh) 82
Register 7-25 SOC.CFGIO2 (AIO10-AIO13 Configuration 2, 1Eh) 82
Register 7-26 SOC.SIGINTM (AIO Interrupt Mask, 1Fh) 83
Register 7-27 SOC.SIGINTF (AIO Interrupt Flag, 20h) 84
Register 7-28 SOC.BLANKING (Comparator Blanking Configuration, 21h) 85
Register 7-29 SOC.SPECCFG0 (AIO7 Comparator Hysteresis Configuration, 22h) 86
Register 7-30 SOC.SPECCFG1 (AIO8/9 Comparator Hysteresis Configuration, 23h) 87
Register 7-31 SOC.SPECCFG2 (AIO7/8 Comparator MUX Input Configuration, 24h) 89
Register 7-32 SOC.SPECCFG3 (AIO9 Comparator MUX Input Configuration, 25h) 89
Register 8-1 SOC.CFGDRV0 (Driver Configuration 0, 26h) 96
Register 8-2 SOC.CFGDRV1 (Driver Configuration 1, 27h) 97

Register 8-3 SOC.CFGDRV2 (Driver Configuration 2, 28h) 98
Register 8-4 SOC.CFGDRV3 (Driver Configuration 3, 29h) 99
Register 8-5 SOC.STATDRV (Driver Status, 2Ah) 100
Register 8-6 SOC.ENDRV (Driver Manager Enable, 7Dh) 101
Register 8-7 SOC.WDTPASS (WDT Password, 7Eh) 101

1 OVERVIEW

This document is the PAC5532 Device User Guide. It details the operation of the analog peripherals in the PAC5532.

For detailed information on the MCU and Digital Peripherals in the PAC5532, see the *PAC55XX Family User Guide*.

2 STYLE AND FORMATTING CONVENTIONS

This chapter describes the formatting and styles used throughout this document.

2.1 Number Representation

Numbers other than decimal will have a postfix indicator. All numbers use little endian formatting, with the most significant bit/digit to the left. Digits for binary and hexadecimal representation are grouped with a single space every four digits to improve readability. Binary numbers use “b” as a postfix and hexadecimal numbers use “h” as a postfix.

For example, 1011b binary = Bh hexadecimal = 11 decimal.

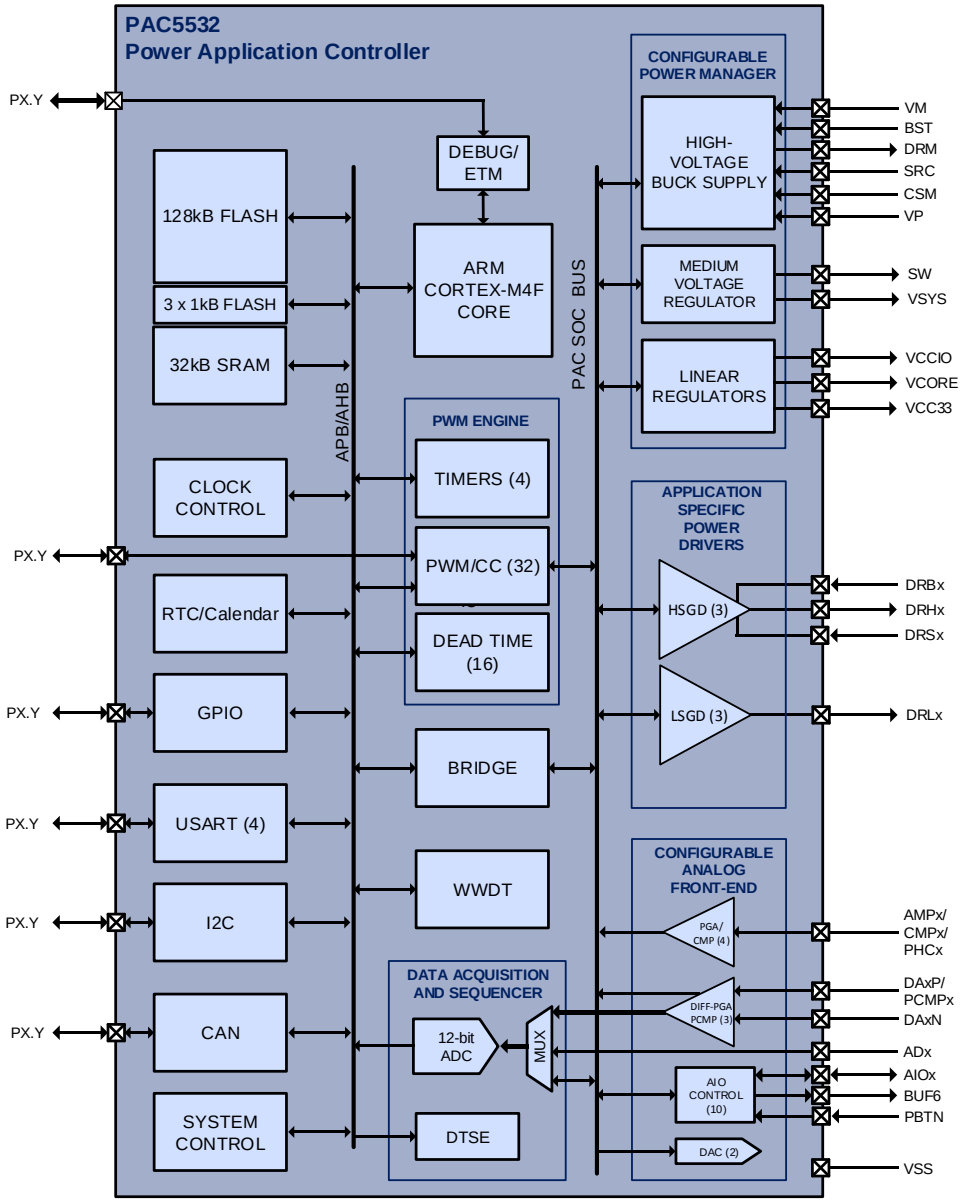
2.2 Formatting Styles

TYPE	EXAMPLE	DESCRIPTION
Register Name	**RTCCTL**	Register names use a capital letter and **boldface** type.
Register Bit(s)	**RTCCTL.RTCCLKDIV**	Register bits are always represented with the register name separated with a period.
Function selected by register bit(s)	**[RTCCTL.RTCCLKDIV]**	Within text blocks, functions selected with a register bit setting are set in brackets. For example **[RTCCTL.RTCCLKDIV]** means divider settings /2 to /65536.
Pin Function	PA5	Pin functions use capital letters
Internal signals	*PWMA3*	Internal signals use *italicized* font.
Formulas	`CLK = FCLK / DIV`	Formulas use `monospaced` text.
Links	Link	Hyperlinks are underlined and blue.
CPU Mnemonic	`MRS`	CPU Mnemonic uses `monospaced` text.
Operands	*`{Rd, }, Rn, Rm`*	Operands use *`monospaced italic`* text.
Code examples	`b loopA`	Code examples use monospaced text.

3 ARCHITECTURAL BLOCK DIAGRAM

For Below is an architecture block diagram of the PAC5532 device.

Figure 3-1 PAC5532 Architectural Block Diagram



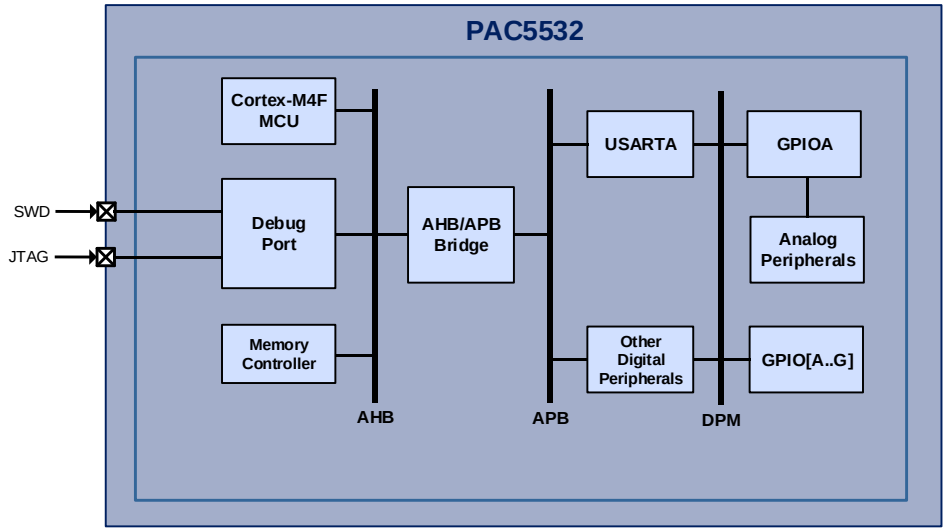
4 ANALOG REGISTER ACCESS

4.1 Overview

All analog registers in the PAC5532 are accessible through a SOC bus in the device. Unlike registers in the MCU (SRAM and digital peripheral registers), these analog registers are not memory mapped.

The block diagram below shows the different system busses that the MCU uses to access the different system registers.

Figure 4-1 PAC5532 Register Access



The PAC5532 contains two register buses: the AHB bus and the APB bus.

The AHB bus allows the MCU and Debug Port access to FLASH and SRAM via the Memory Controller. To access other digital peripheral connected to the APB bus, there is a bridge from the AHB to the APB bus so that the MCU or Debug Port can perform memory-mapped register access to all digital peripherals. Some digital peripherals such as timers are flexibly connected to IO using the DPM bus.

To access the Analog peripherals, the USARTA SPI peripheral is used to generate read and write transactions to the Analog registers using the DPM and GPIOA.

4.2 Functional Description

External programming interfaces such as JTAG and SWD or the Cortex-M4F MCU may perform memory-mapped accesses to USART A through the AHB and APB busses on the device.

USART A is a serial communication peripheral that supports a SPI-like protocol that can be used to communicate to the Analog Peripherals for read and write transactions. The Digital

Peripheral MUX (DPM) may be configured to connect the USART A SPI signals to GPIO A, where they are connected to the Analog peripherals.

4.3 USART Configuration

USART A acts as a SPI bus master to communicate with the Analog Peripherals. The USART A signals that are used for this communication are:

- *USASCLK* – USART A SPI Clock
- *USAMOSI* – USART A Master-Out/Slave-In
- *USAMISO* – USART A Master-In/Slave-Out
- *USASS* – USART A Slave Select

In order to communicate with the Analog Peripherals, the USART A should have the following configuration:

- 8-bit mode
- SCLK active high
- CPH is sample/setup
- SS active low

When communicating with the Analog Peripherals, the maximum SCLK frequency is 25MHz.

4.4 Protocol

The protocol for communicating with the Analog Peripherals is a simple two-byte protocol.

The first byte is always the address, which includes a 7-bit address [7:1] and a write bit [0]. For write operations, the write bit [0] is set to 1b. For read operations, the write bit [0] is set to 0b.

For write operations, the 2nd byte will be the 8-bit data to write to the given address.

For read operations, the 2nd byte is ignored and MISO will contain the 8-bit data read from the given address.

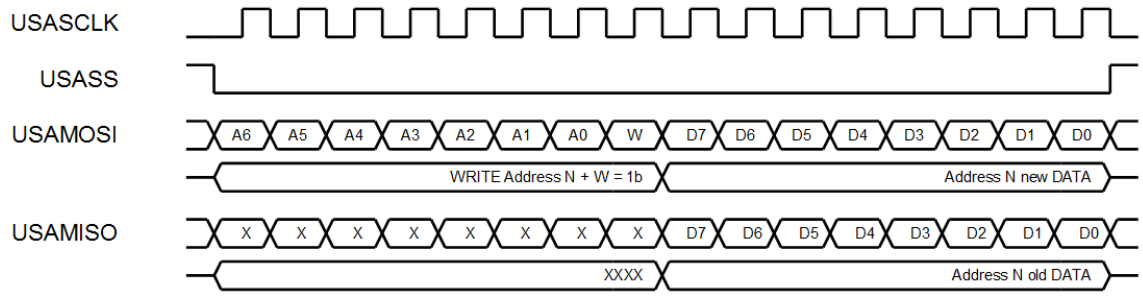
4.5 Write Register Example

To write the **HPDACH** register (address 11h) with the value 28h, issue the following transactions to USART A:

- Write **SSPADAT** with the value 23h (11h << 1 | 1b for write transaction)
- Write **SSPADAT** with the value 28h

The timing diagram from a write operation is shown below.

Figure 4-2 Analog Peripheral Register Write Timing



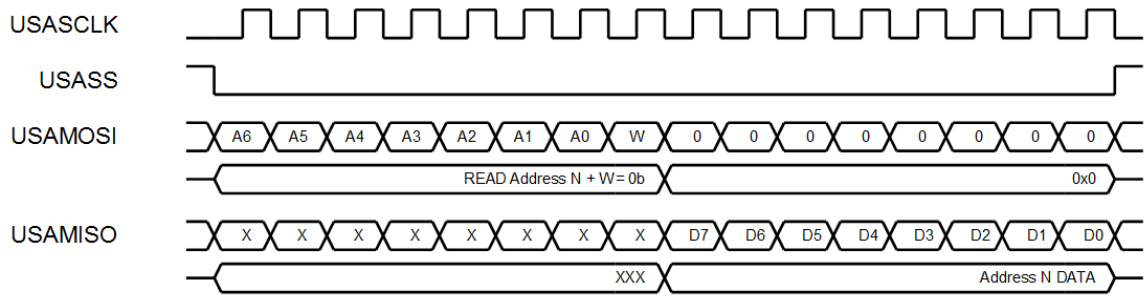
4.6 Read Register Example

To read the contents of the **HPDACH** register, issue the following transactions to USART A:

- Write **SSPADAT** with the value 22h (11h << 1 | 0b for read transaction)
- Write **SSPADAT** with a dummy character
- Read last data from MISO from **SSPADAT**, this is the register value

The timing diagram from a read operation is shown below.

Figure 4-3 Analog Peripheral Register Read Timing



For more information on how to configure the DPM to support the USART A peripheral for communicating with the Analog Registers, see the PAC55XX Family User Guide.

5 PAC5532 IO

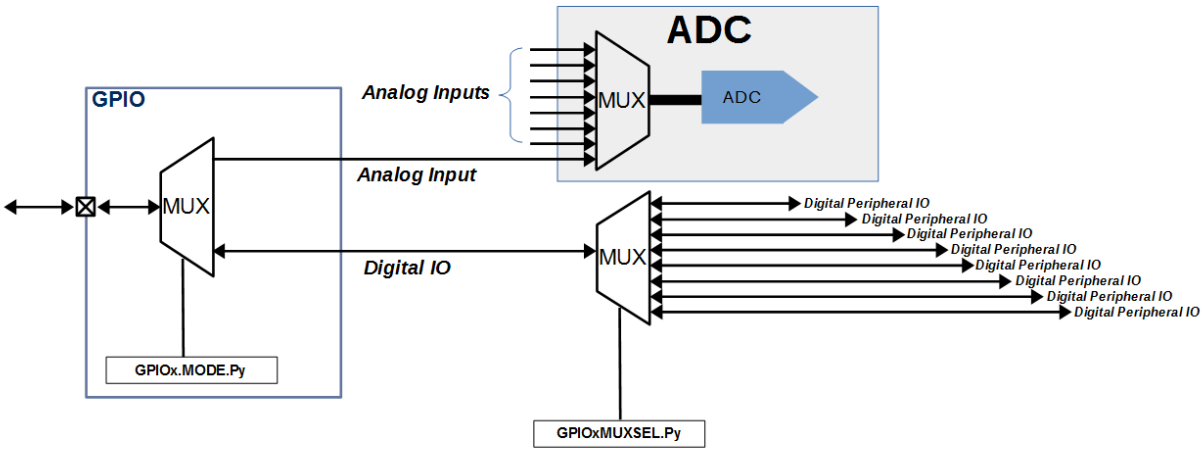
5.1 Overview

The Digital Peripheral MUX (DPM) on the PAC55XX family allows flexible assignment of peripheral functions to IO pins.

Each member of the family has a different set of IO pins that are available. It is important during application design that the designer consider the available IO pins to make sure the necessary peripherals will be available.

Below is a diagram of the GPIO and MUX structure.

Figure 5-1 GPIO and DPM Block Diagram



Each IO can be configured to select 1 of up to 8 digital peripheral signals. Some IOs also may be used as an ADC input. For information on how to configure the IO for each of these situations, see the PAC55XX Family User Guide.

The PAC5532 has the following IO pins available for application use:

- PA[7:0] – Reserved for MMPM, ASPD, CAFE
- PB[7:0] – Reserved for ASPD
- PC[5:4]
- PD[2:0]
- PE[3:0]
- PF[6:0]

5.2 ADC Channels

The ADC channels that are available on the PAC5532 are shown in the table below.

Table 5-1 PAC5532 ADC Input Pins

ADC Channel	IO PIN
ADC0	PG7[1]
ADC2	PD2
ADC3	PD1
ADC4	PD0, PF4[2]
ADC5	PF5
ADC6	PF6

[1] Available for sampling channels in the CAFE only
[2] For ADC channels that are available on more than on GPIO, the user must configure only one GPIO as the analog input

5.3 Digital Peripheral Pins

The digital peripheral functions that are available in the PAC5532 are shown below.

Table 5-2 PAC5532 Digital Peripheral Pins

PORT	Pin	GPIOxMUXS.Py							
		000b	001b	010b	011b	100b	101b	110b	111b
GPIOA	P0	**GPIOA0**							
	P1	GPIOA1	**EMUXD**						
	P2	GPIOA2	**EMUXC**						
	P3	GPIOA3	**USASCLK**	USBSCLK					
	P4	GPIOA4	**USAMOSI**	USBMOSI					
	P5	GPIOA5	**USAMISO**	USBMISO					
	P6	GPIOA6	**USASS**	USBSS					
	P7	**GPIOA7**							
GPIOB	P0	**GPIOB0**	TAPWM0	TBPWM0					
	P1	**GPIOB1**	TAPWM1	TBPWM1					
	P2	**GPIOB2**	TAPWM2	TBPWM2					
	P4	**GPIOB4**	TAPWM4	TBPWM4					
	P5	**GPIOB5**	TAPWM5	TBPWM5					
	P6	**GPIOB6**	TAPWM6	TBPWM6					
GPIOC	P4	**GPIOC4**	TBPWM4	TCPWM4	TCIDX	USBMOSI	USCSCLK	CANRXD	I2CSCL
	P5	**GPIOC5**	TBPWM5	TCPWM5	TCPHA	USBMISO	USCSS	CANTXD	I2CSDA
GPIOD	P0	**GPIOD0**	TBPWM0	TCPWM0	TDIDX	TCK/SWDCLK	USCSCLK	CANTXD	EMUXD
	P1	**GPIOD1**	TBPWM1	TCPWM1	TDPHA	TMS/SWDIO	USCSS	CANRXD	EMUXC
	P2	**GPIOD2**	TBPWM2	TCPWM2	TDPHB	TDI	USCMOSI		
GPIOE	P0	**GPIOE0**	TCPWM0	TDPWM0	TAIDX	TBIDX	USCSCLK	I2CSCL	EMUXC
	P1	**GPIOE1**	TCPWM1	TDPWM1	TAPHA	TBPHA	USCSS	I2CSDA	EMUXD
	P2	**GPIOE2**	TCPWM2	TDPWM2	TAPHB	TBPHB	USCMOSI	CANRXD	EXTCLK
	P3	**GPIOE3**	TCPWM3	TDPWM3	FRCLK		USCMISO	CANTXD	
GPIOF	P0	GPIOF0	TCPWM0	TDPWM0	**TMS/SWDCLK**	TBIDX	USBSCLK	TRACECLK	
	P1	GPIOF1	TCPWM1	TDPWM1	**TMS/SWDIO**	TBPHA	USBSS	TRACED0	
	P2	GPIOF2	TCPWM2	TDPWM2	**TDI**	TBPHB	USBMOSI	TRACED1	
	P3	GPIOF3	TCPWM3	TDPWM3	**TDO**	FRCLK	USBMISO	TRACED2	
	P4	GPIOF4	TCPWM4	TDPWM4	**TCK/SWDCLK**	TCIDX	USDSCLK	TRACED3	EMUXC
	P5	GPIOF5	TCPWM5	TDPWM5	**TMS/SWDIO**	TCPHA	USDSS		EMUXD
	P6	GPIOF6	TCPWM6	TDPWM6	**TDI**	TCPHB	USDMOSI	CANRXD	I2CSCL

For more information on how to configure the DPM for the PAC5532, see the PAC55XX Family User Guide.

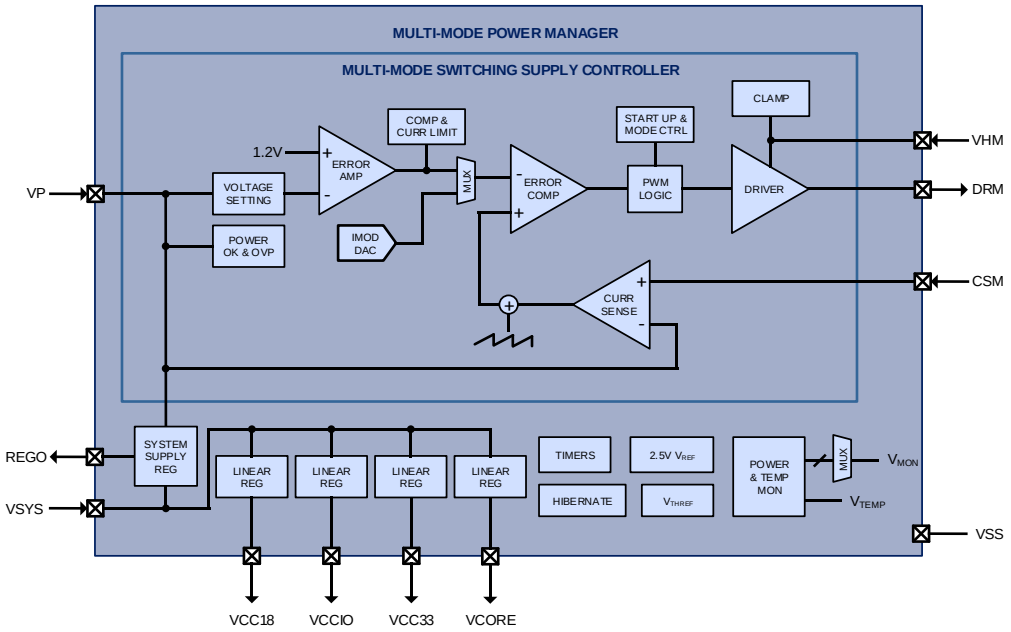
6 CONFIGURABLE POWER MANAGER

6.1 Features

- 160V Buck DC/DC Controller (HV-BUCK)
  - 25V – 160V input
- 5V Switching Regulator (MV-BUCK)
- 4 linear regulators with power and hibernate management, including V_{REF} for ADC
- Power and temperature monitor, warning, and fault detection

6.2 System Block Diagram

Figure 6-1 CPM System Block Diagram



6.3 Functional Description

The Configurable Power Manager (Figure 6-1) is optimized to efficiently provide “all-in-one” power management required by the PAC® and associated application circuitry. It incorporates a high-voltage power supply controller that is used to convert power from a DC input source to generate a main supply output V_P. There is also an integrated medium-voltage buck DC/DC regulator to generate V_{SYS}.

Three other linear regulators provide V_{CCIO}, V_{CC33}, V_{CC18} and V_{CORE} supplies for 3.3V I/O, 3.3V mixed signal, 1.8V analog and 1.9V microcontroller core circuitry. The power manager also handles system functions including internal reference generation, timers, hibernate mode management, and power and temperature monitoring.

6.4 Register Summary

Table 6-1 CPM Register Summary

ADDRESS	REGISTER	DESCRIPTION	RESET
00h	**SOC.FAULT**	Fault condition indication register	00h
01h	**SOC.STATUS**	Hardware status condition register	00h
02h	**SOC.MISC**	Miscellaneous features register	00h
03h	**SOC.PWRCTL**	Power Manager control register	00h
04h	**SOC.FAULTMASK**	Power Manager fault mask register	00h
05h	**SOC.WATCHDOG**	SOC Watchdog configuration register	00h
2Bh	**SOC.SYSCONF**	Power Manager system configuration register	0Ch

6.5 Register Detail

6.5.1 SOC.FAULT

Register 6-1 SOC.FAULT (Fault Condition, 00h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**TMPWARN**	R	0x0	Real-time temperature warning status. When the temperature is greater than the warning threshold, this bit is set to 1b. When the temperature less than the warning threshold, this bit is set to 0b. 0b: No temperature warning 1b: Temperature warning
6	**TMPWARN_LATCH**	R	0x0	Latched temperature warning status. If the temperature reaches the warning threshold and the **SOC.FAULTMASK.nTMPWARN** is not masked, this bit is set and nIRQ1 is asserted. Write 1b to clear when not masked. 0b: No temperature warning 1b: Temperature warning
5	**TMPFLT**	R	0x0	Temperature fault status. If the temperature reaches the fault threshold, this bit is set to 1b. Write 1b to clear. 0b: No temperature fault 1b: Temperature fault
4	**VPFLT**	R	0x0	DC/DC fault when VP is below UVLO or over-voltage. Set on fault, and cleared when written to 1b. 0b: No VP fault 1b: VP fault
3	**VSYSFLT**	R	0x0	VSYS fault when VSYS is below UVLO or over-voltage. Set on fault, and cleared when written to 1b. 0b: No VSYS fault 1b: VSYS fault
2	**VCCIOFLT**	R	0x0	VCCIO fault. Set on fault, and cleared when written to 1b. 0b: No VCCIO fault 1b: VCCIO fault
1	**VCC33FLT**	R	0x0	VCC33 fault. Set on fault, and cleared when written to 1b. 0b: No VCC33 fault 1b: VCC33 fault
0	**VCOREFLT**	R	0x0	VCORE fault. Set on fault, and cleared when written to 1b. 0b: No VCORE fault 1b: VCORE fault

6.5.2 SOC.STATUS

Register 6-2 SOC.STATUS (System Status, 01h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**HWRSTAT**	R	0x0	Hardware Reset Status. Bit is set on hardware reset and is cleared when written to 1b. 0b: No hardware reset 1b: Hardware reset
6	**SRST**	R	0x0	Soft Reset Event. Bit is set on software reset event and is cleared when written to 1b. 0b: No software reset 1b: Software reset
5	**WDTRSTAT**	R	0x0	Watchdog Timer Reset Status. When enabled, this bit is set on Watchdog Timer Reset and cleared when written to 1b. 0b: No WDT reset 1b: WDT Reset
4	**RFU**	R	0x0	Reserved
3	**VPLOW**	R	0x0	Real-time VP Low Status. 0b: No VP low 1b: VP low
2	**VPLOW_LATCH**	R	0x0	Latched VP Low Status. During VP low condition, this bit is set and the nIRQ signal is asserted. To clear this bit, write to 1b. 0b: No latched VP low 1b: Latched VP low
1	**PBSTAT**	R	0x0	Real-time Push-button Status. 0b: Push-button not active 1b: push-button active
0	**PBSTAT_LATCH**	R	0x0	Latched Push-button Status. This bit is set in normal operation as long as the push button is enabled and on for more than the deglitch time, if not masked. When this bit is set, it will assert the nIRQ signal. 0b: Latched push-button not active 1b: Latched push-button active

6.5.3 SOC.MISC

Register 6-3 SOC.MISC (SOC Miscellaneous Configuration, 02h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**HIB**	R/W	0x0	Hibernate Mode. This bit is automatically cleared when the power up sequence is initiated, after wake-up timer delay or external event. 0b: Normal 1b: Shutdown mode
6	**PBEN**	R/W	0x0	AIO6 Push-button Enable. 0b: Push-button not enabled 1b: Push-button enabled
5	**VREFSET**	R/W	0x0	ADC Reference Voltage Setting. 0b: 2.5V 1b: 3.0V
4	**CLKOUTEN**	R/W	0x0	Low-speed clock output (CLKOUT) enable. 0b: Not enabled 1b: Enabled
3	**MCUALIVE**	R/W	0x0	MCU Alive. Set by the MCU to indicate that it is alive. Before this bit is set, ignore all MCU commands (EMUX, gate driver) except SPI register commands. This bit will automatically be cleared when the reset signal to the MCU is asserted. 0b: MCU not alive 1b: MCU alive
2	**TPBD**	R/W	0x0	Push-button deglitch time: 0b: 32ms 1b: 1ms
1	**RFU**	R	0x0	Reserved
0	**SMEN**	R/W	0x0	Signal Manager Enable. This bit is automatically cleared when the reset signal to the MCU is asserted. 0b: Not enabled 1b: Enabled

6.5.4 SOC.PWRCTL

Register 6-4 SOC.PWRCTL (Power Control, 03h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:6	**CLKOUTFREQ**	R/W	0x0	Low-Speed Clock Output Frequency Setting (CLKOUT). 00b: 250Hz 01b: 500Hz 10b: 1kHz 11b: 2kHz
5:3	**PWRMON**	R/W	0x0	Power Monitor Signal. This field selects the signal to use for AB11 for ADC monitoring (buffered). 000b: VCORE 001b: VCORE x 4/10 010b: VCC33 x 4/10 011b: VCCIO x 4/10 100b: VSYS x 4/10 101b: ISENSE 110b: VPTAT 111b: VP x 1/10
2:0	**WUTIMER**	R/W	0x0	Wake-up Timer: 000b: infinite 001b: 125ms 010b: 250ms 011b: 500ms 100b: 1s 101b: 2s 110b: 4s 111b: 8s

6.5.5 SOC.FAULTMASK

Register 6-5 SOC.FAULTMASK (Fault mask, 04h)

BIT	NAME	ACCESS[3]	RESET	DESCRIPTION
7	**RFU**	R/W	0x0	Reserved
6	**nTMPWARN**	R/W	0x0	Temperature Warning Mask. 0b: Masked 1b: Not masked (asserts nIRQ1)
5	**nVPFLT**	R/W	0x0	VP Fault Mask. 0b: Masked 1b: Not masked
4	**nVSYSFLT**	R/W	0x0	VSYS Fault Mask. 0b: Masked 1b: Not masked
3	**RFU**	R	0x0	Reserved
2	**nLDOFLT**	R/W	0x0	LDO Fault Mask. 0b: Masked 1b: Not masked
1	**nPBINT**	R/W	0x0	Push-button Interrupt Mask. 0b: Masked 1b: Not masked
0	**nVPINT**	R/W	0x0	VP Low Interrupt Mask. 0b: Masked 1b: Not masked

[3] This byte is unlocked for writing when **UNLOCK** = 1b.

6.5.6 SOC.WATCHDOG

Register 6-6 SOC.WATCHDOG (SOC Watchdog Configuration, 05h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**SRST**	R/W	0x0	Soft Reset. This bit can be set to issue a system soft reset. This bit is always read as 0b. When set, the STATUS.SRST bit will be latched to a 1b so the MCU knows the system is being started after a soft reset. 0b: Do not issue soft reset 1b: Issue soft reset
6:4	**RFU**	R	0x0	Reserved
3	**WDTEN**	R/W	0x0	Watchdog Timer Enable. Cleared during hard reset. 0b: disabled 1b: enabled
2:0	**TWD**	R/W	0x0	Watch-dog Timer. 000b: 62.5ms 001b: 125ms 010b: 250ms 011b: 500ms 100b: 1s 101b: 2s 110b: 4s 111b: 8s

6.5.7 SOC.SYSCONF

Register 6-7 SOC.SYSCONF (System Configuration, 2Bh)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:4	**RFU**	R	0x0	Reserved
3	**VPSET**	R/W	0x1	VP Setting. 0b: 12V 1b: 15V
2:1	**HVBK_FREQ**	R/W	0x2	High-Voltage Buck Switching Frequency Setting. 00b: 50kHz 01b: 100kHz 10b: 200kHz 11b: 400kHz
0	**RFU**	R	0x0	Reserved

7 CONFIGURABLE ANALOG FRONT-END

7.1 Overview

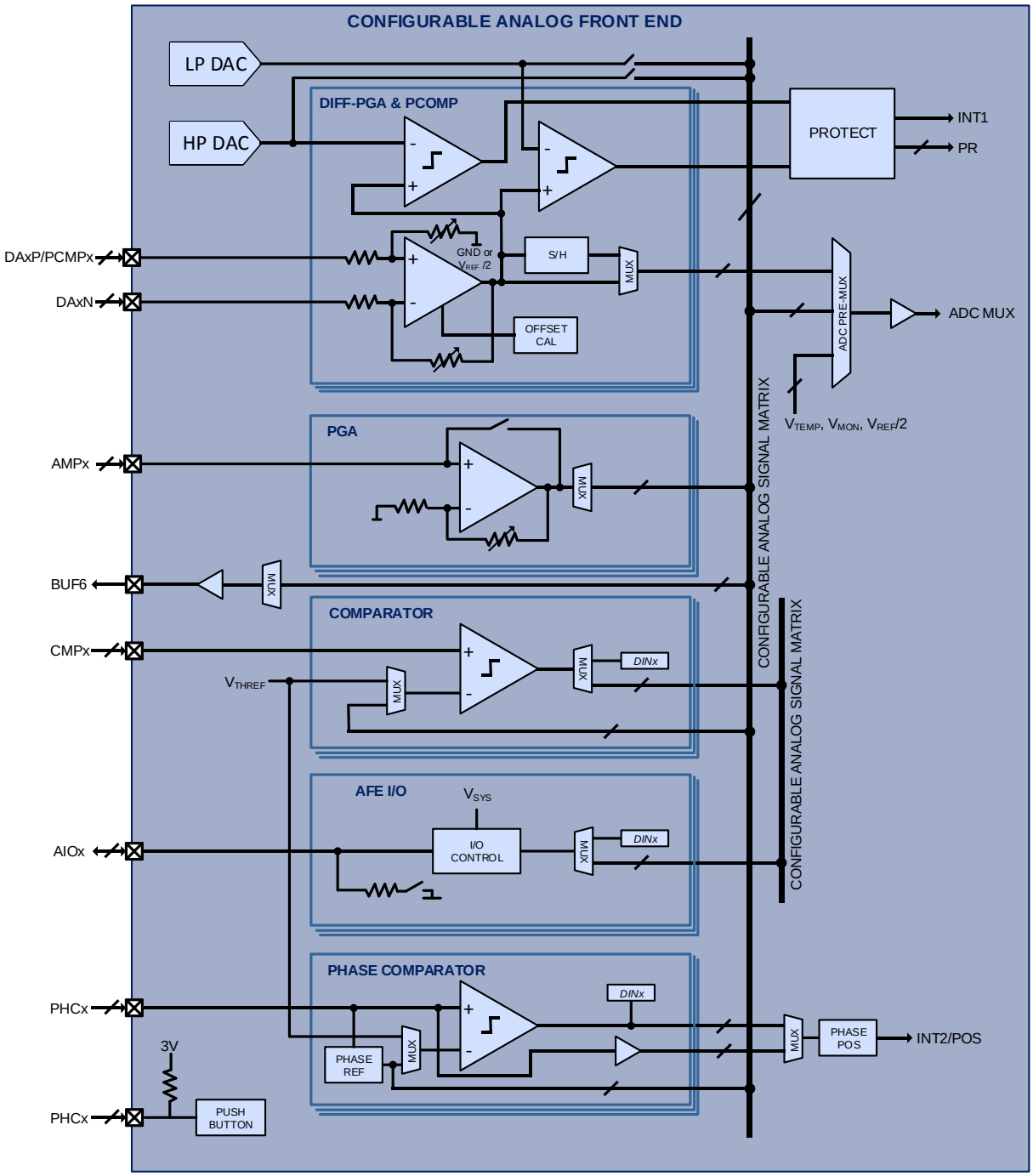
The device includes a Configurable Analog Front End (CAFE, Figure 7-1) accessible through 8 analog and I/O pins. These pins can be configured to form flexible interconnected circuitry made up of 3 differential programmable gain amplifiers, 4 single-ended programmable gain amplifiers, 4 general purpose comparators, 3 phase comparators, 10 protection comparators, and one buffer output. These pins can also be programmed as analog feed-through pins, or as analog front end I/O pins that can function as digital inputs or digital open-drain outputs. The PAC® proprietary configurable analog signal matrix (CASM) and configurable digital signal matrix (CDSM) allow real time asynchronous analog and digital signals to be routed in flexible circuit connections for different applications. A push button function is provided for optional push button on, hibernate, and off power management function.

7.2 Features

- 10 Configurable Analog I/O signals
  - Gain mode, comparator mode, I/O mode, special mode
- 3 High-Performance, Configurable Differential Amplifiers
- 4 High-Performance, Configurable Single-Ended Amplifiers
- Two high-speed comparators with protection functions
- Phase to phase, phase to center-tap modes
- Bi-directional, asymmetric configurable comparator hysteresis
- Push-button input for entering/exiting hibernate mode

7.3 System Block Diagram

Figure 7-1 CAFE System Block Diagram



7.4 Functional Description

7.4.1 Enabling the CAFE

Before the CAFE sub-system can be signal sampling, it must be enabled.

To enable this sub-system, set **SOC.MISC.SMEN** to 1b.

7.4.2 Integrated Temperature Sensor

The PAC5532 contains an integrated temperature sensor that can be sampled on the AB10 analog bus. To read the temperature, sample this ADC channel and convert the ADC counts to °C using the following formula:

°C = ((ADC counts – **TTEMPS**) >> 1) + **FTTEMP**.

The variables **TTEMPS** and **FTTEMP** can be found in INFO-1 memory.

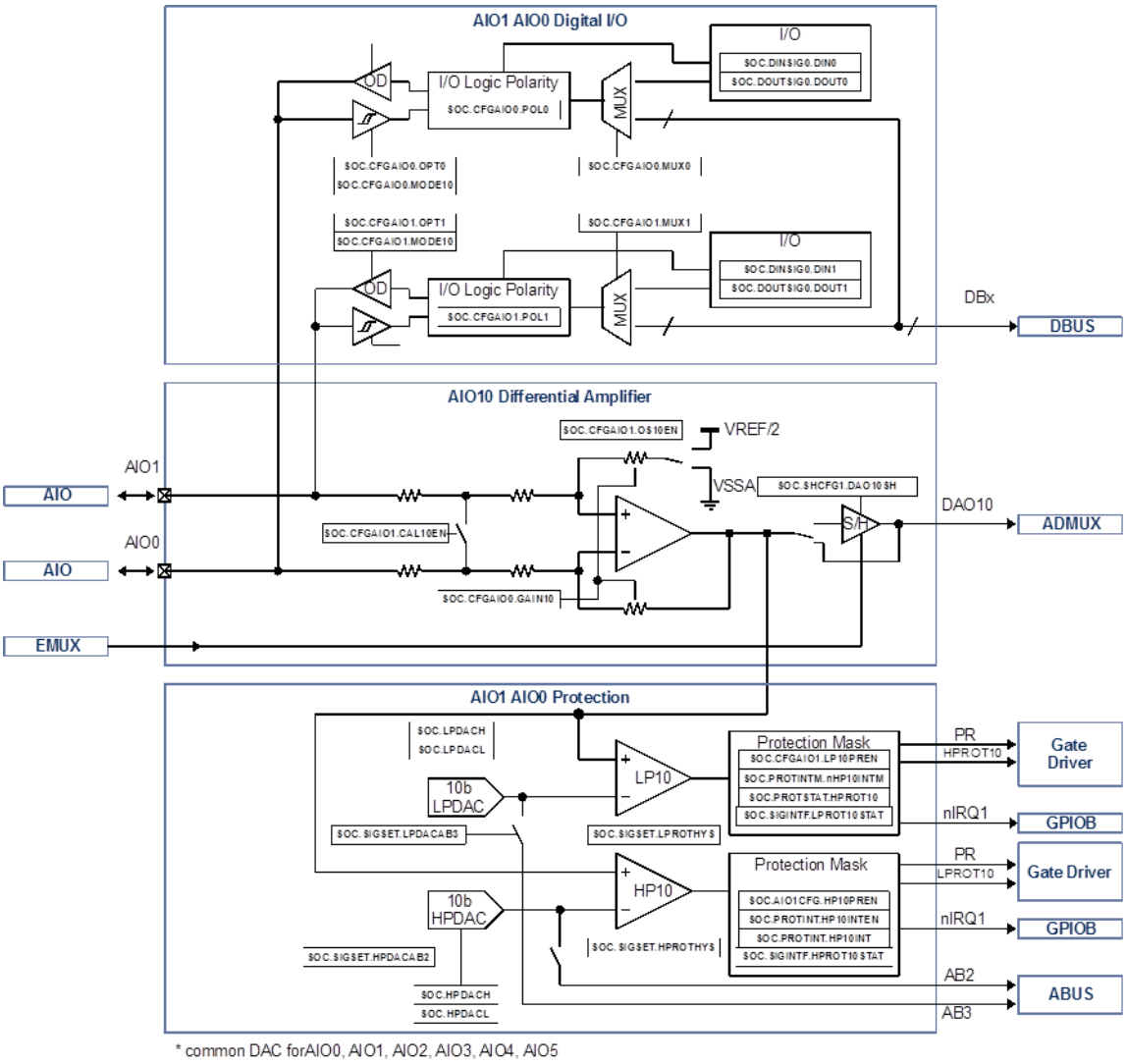
For more information on these variables, see the PAC55XX Family User Guide.

7.5 AIO10

AIO10 may be configured as digital inputs or as a differential amplifier with protection.

7.5.1 System Block Diagram

Figure 7-2 AIO10 Block Diagram



* common DAC forAIO0, AIO1, AIO2, AIO3, AIO4, AIO5

7.5.2 AIO1, AIO0

AIO1 and AIO0 can be configured as digital inputs or as differential amplifier pair with additional protection.

7.5.3 AIO1, AIO0 digital I/O Mode

Set **SOC.CFGAIO0.MODE10** = 00b to use AIO1 and AIO0 as digital inputs.

7.5.3.1 AIO0 IO

Set **SOC.CFGAIO0.OPT0** = 00b to use AIO0 as input. The input state can be read at **SOC.DINSIG0.DIN0**.

Set **SOC.CFGAIO0.OPT0** = 10b to use AIO0 as open drain output. Set **SOC.CFGAIO0.MUX0** = 00b to mux the output state from **SOC.DOUTSIG0.DOUT0**. Use **SOC.CFGAIO0.MUX0** to mux the output signal from the internal digital bus DBUS DB1 to DB7.

7.5.3.2 AIO1 IO

Set **SOC.CFGAIO1.OPT1** = 00b to use AIO1 as input. The input state can be read at **SOC.DINSIG0.DIN1**.

Set **SOC.CFGAIO1.OPT1** = 10b to use AIO1 as open drain output. Set **SOC.CFGAIO1.MUX1** = 00b to MUX the output state from **SOC.DOUTSIG0.D1OUT**. Use **SOC.CFGAIO1.MUX1** to MUX the output signal from the internal digital bus DBUS DB1 to DB7.

7.5.3.3 AIO0 Polarity

Use **SOC.CFGAIO0.POL0** to set logic polarity of the signal between AIO0 input/output and MUX0.

7.5.3.4 AIO1 Polarity

Use **SOC.CFGAIO0.POL1** to set logic polarity of the signal between AIO1 input/output and MUX1.

7.5.4 AIO1, AIO0 differential Amplifier Mode

Set **SOC.CFGAIO0.MODE10** = 01b to use AIO1 and AIO0 as input to a differential amplifier.

7.5.4.1 AIO1, AIO0 Differential Amplifier Gain

Use **SOC.CFGAIO0.GAIN10** to set to gain between 1x to 48x.

7.5.4.2 AIO1, AIO0 Differential Amplifier Reference

Use **SOC.CFGAIO1.OS10EN** to set the amplifier reference either VSSA or VREF/2.

7.5.4.3 AIO1, AIO0 Differential Amplifier Calibration

Use **SOC.1.CAL10EN** to short the input of the differential amplifier to allow reading of the amplifier offset.

7.5.5 AIO1, AIO0 Protection

In **SOC.CFGAIO0.MODE10** = 01b differential amplifier mode, a high side comparator protector HP10 and a low side comparator protector LP10 are also active that can be configured to disabled high-side or low-side drivers in the application specific power driver section.

7.5.5.1 HP10 Comparator

The HP10 comparator takes the AIO1 voltage referenced to VSSA and compares it against the HP-DAC voltage. The 10-bit HP-DAC is programmable with **SOC.HPDACH** and **SOC.HPDACL**.

Use **SOC.CFGAIO1.HP10EN** to enable HP10 comparator with different blanking times.

Use **SOC.SIGSET.HPROTHYS** to enable HP10 comparator hysteresis.

The output of HP10 comparator can be configured to trigger protection signal PR using **SOC.CFGAIO1.HP10PREN**.

The output of HP10 can also trigger the nIRQ1 interrupt using **SOC.PROTINTM.nHP10INTM** to un-mask the interrupt. The real-time status can be observed using **SOC.SIGINTF.HPROT10STAT** and the latched interrupt status can be observed using **SOC.PROTSTAT.HPROT10**.

7.5.5.2 LP10 Comparator

The LP10 comparator takes the output of the differential amplifier and compares it against the LP-DAC voltage. The 10-bit LP-DAC is programmable with **SOC.LPDACH** and **SOC.LPDACL**.

Use **SOC.CFGAIO0.LP10EN** to enable LP10 comparator with different blanking times.

Use **SOC.SIGSET.LPPROTHYS** to enable LP10 comparator hysteresis.

The output of LP10 comparator can be configured to trigger protection signal PR using **SOC.CFGAIO1.LP10PREN**.

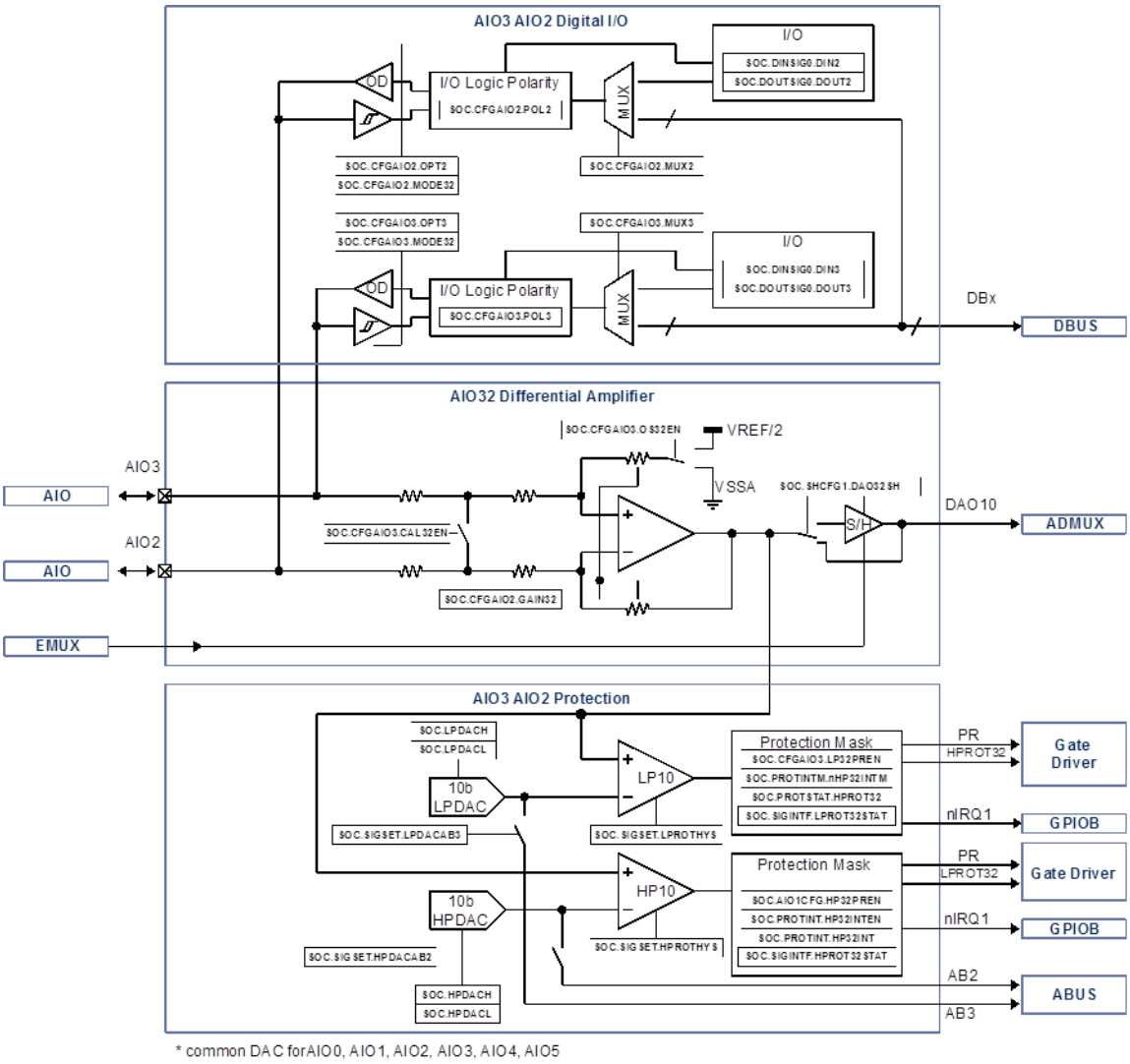
The output of LP10 can also trigger the nIRQ1 interrupt using **SOC.PROTINTM.nLP10INTM** to un-mask the interrupt. The real-time interrupt status can be observed with **SOC.SIGINTF.LPROT10STAT** and the latched interrupt status can be observed using **SOC.PROTSTAT.LPROT10**.

7.6 AIO32

AIO32 may be configured as digital inputs or as a differential amplifier with protection.

7.6.1 System Block Diagram

Figure 7-3 AIO32 Block Diagram



7.6.2 AIO3, AIO2

AIO3 and AIO2 can be configured as digital inputs or as differential amplifier pair with additional protection.

7.6.3 AIO3, AIO2 digital I/O Mode

Set **SOC.CFGAIO2.MODE32** = 00b to use AIO3 and AIO2 as digital inputs.

7.6.3.1 AIO2 IO

Set **SOC.CFGAIO2.OPT2** = 00b to use AIO2 as input. The input state can be read at **SOC.DINSIG0.DIN2**.

Set **SOC.CFGAIO2.OPT2** = 10b to use AIO2 as open drain output. Set **SOC.CFGAIO2.MUX2** = 00b to mux the output state from **SOC.DOUTSIG0.DOUT2**. Use **SOC.CFGAIO2.MUX2** to mux the output signal from the internal digital bus DBUS DB1 to DB7.

7.6.3.2 AIO3 IO

Set **SOC.CFGAIO3.OPT3** = 00b to use AIO3 as input. The input state can be read at **SOC.DINSIG0.DIN3**.

Set **SOC.CFGAIO3.OPT3** = 10b to use AIO3 as open drain output. Set **SOC.CFGAIO3.MUX3** = 00b to MUX the output state from **SOC.DOUTSIG0.DOUT3**. Use **SOC.CFGAIO3.MUX3** to MUX the output signal from the internal digital bus DBUS DB1 to DB7.

7.6.3.3 AIO2 Polarity

Use **SOC.CFGAIO2.POL2** to set logic polarity of the signal between AIO2 input/output and MUX2.

7.6.3.4 AIO3 Polarity

Use **SOC.CFGAIO3.POL3** to set logic polarity of the signal between AIO3 input/output and MUX3.

7.6.4 AIO3, AIO2 differential Amplifier Mode

Set **SOC.CFGAIO2.MODE32** = 01b to use AIO3 and AIO2 as input to a differential amplifier.

7.6.4.1 AIO3, AIO2 Differential Amplifier Gain

Use **SOC.CFGAIO2.GAIN32** to set to gain between 1x to 48x.

7.6.4.2 AIO3, AIO2 Differential Amplifier Reference

Use **SOC.CFGAIO3.OS32EN** to set the amplifier reference either VSSA or VREF/2.

7.6.4.3 AIO3, AIO2 Differential Amplifier Calibration

Use **SOC.CFGAIO3.CAL32EN** to short the input of the differential amplifier to allow reading of the amplifier offset.

7.6.5 AIO3, AIO2 Protection

In **SOC.CFGAIO2.MODE32** = 01b differential amplifier mode, a high side comparator protector HP32 and a low side comparator protector LP32 are also active that can be configured to disabled high-side or low-side drivers in the application specific power driver section.

7.6.5.1 HP32 Comparator

The HP32 comparator takes the AIO3 voltage referenced to VSSA and compares it against the HP-DAC voltage. The 10-bit HP-DAC is programmable with **SOC.HPDACH** and **SOC.HPDACL**.

Use **SOC.CFGAIO3.HP32EN** to enable HP32 comparator with different blanking times.

Use **SOC.SIGSET.HPROTHYS** to enable HP32 comparator hysteresis.

The output of HP32 comparator can be configured to trigger protection signal PR using **SOC.CFGAIO3.HP32PREN**.

The output of HP32 can also trigger the nIRQ1 interrupt using **SOC.PROTINTM.nHP32INTM** to un-mask the interrupt. The real-time status can be observed using **SOC.SIGINTF.HPROT32STAT** and the latched interrupt status can be observed using **SOC.PROTSTAT.HPROT32**.

7.6.5.2 LP32 Comparator

The LP32 comparator takes the output of the differential amplifier and compares it against the LP-DAC voltage. The 10-bit LP-DAC is programmable with **SOC.LPDACH** and **SOC.LPDACL**.

Use **SOC.CFGAIO2.LP32EN** to enable LP32 comparator with different blanking times.

Use **SOC.SIGSET.LPPROTHYS** to enable LP32 comparator hysteresis.

The output of LP32 comparator can be configured to trigger protection signal PR using **SOC.CFGAIO3.LP32PREN**.

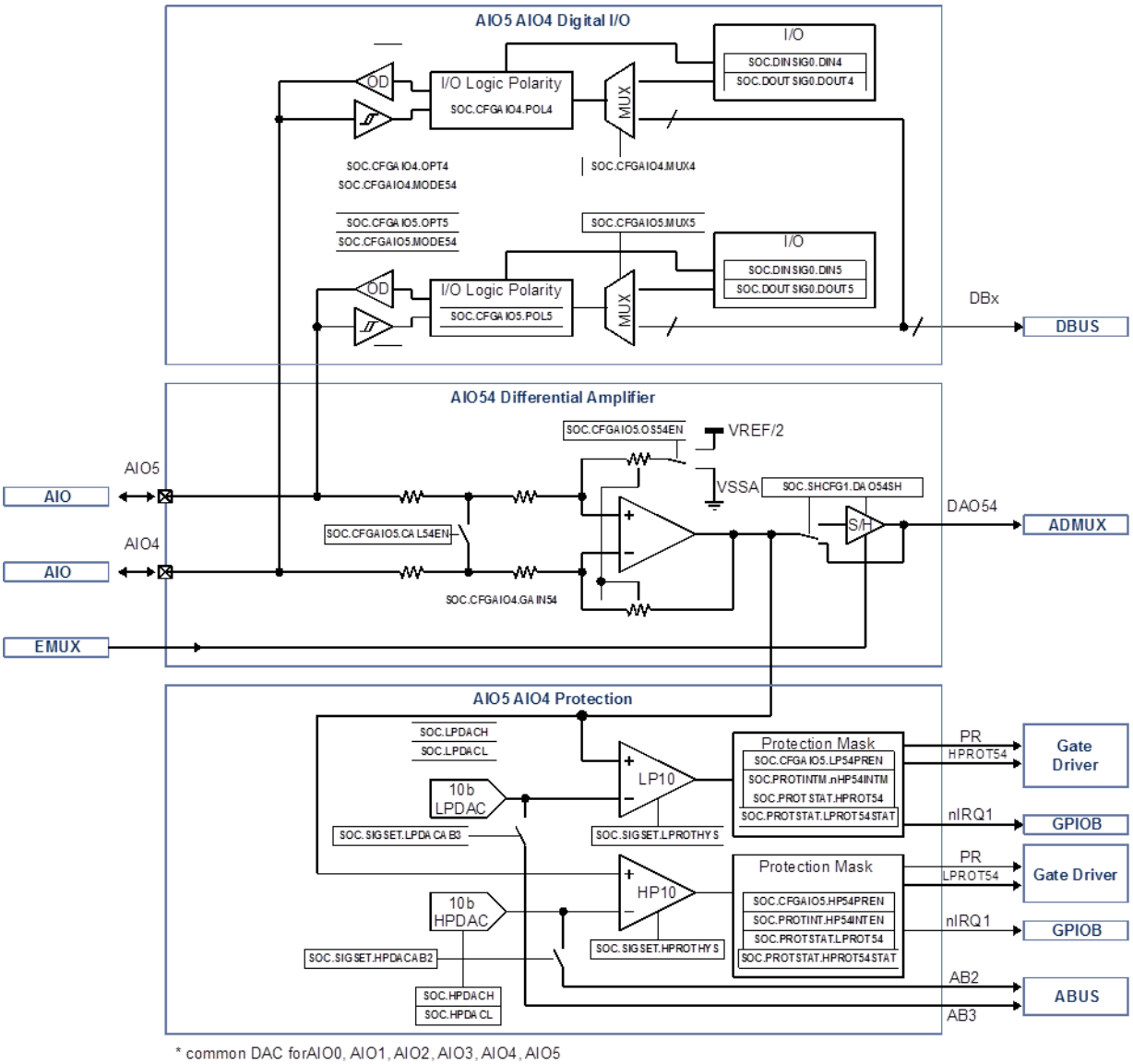
The output of LP32 can also trigger the nIRQ1 interrupt using **SOC.PROTINTM.nLP32INTM** to un-mask the interrupt. The real-time interrupt status can be observed with **SOC.SIGINTF.LPROT32STAT** and the latched interrupt status can be observed using **SOC.PROTSTAT.LPROT32**.

7.7 AIO54

AIO54 may be configured as digital inputs or as a differential amplifier with protection.

7.7.1 System Block Diagram

Figure 7-4 AIO54 Block Diagram



* common DAC forAIO0, AIO1, AIO2, AIO3, AIO4, AIO5

7.7.2 AIO5, AIO4

AIO5 and AIO4 can be configured as digital inputs or as differential amplifier pair with additional protection.

7.7.3 AIO5, AIO4 digital I/O Mode

Set **SOC.CFGAIO4.MODE54** = 00b to use AIO5 and AIO4 as digital inputs.

7.7.3.1 AIO4 IO

Set **SOC.CFGAIO4.OPT4** = 00b to use AIO4 as input. The input state can be read at **SOC.DINSIG0.DIN4**.

Set **SOC.CFGAIO4.OPT4** = 10b to use AIO4 as open drain output. Set **SOC.CFGAIO4.MUX4** = 00b to mux the output state from **SOC.DOUTSIG0.DOUT4**. Use **SOC.CFGAIO4.MUX4** to mux the output signal from the internal digital bus DBUS DB1 to DB7.

7.7.3.2 AIO5 IO

Set **SOC.CFGAIO5.OPT5** = 00b to use AIO5 as input. The input state can be read at **SOC.DINSIG0.DIN5**.

Set **SOC.CFGAIO5.OPT5** = 10b to use AIO5 as open drain output. Set **SOC.CFGAIO5.MUX5** = 00b to MUX the output state from **SOC.DOUTSIG0.DOUT5**. Use **SOC.CFGAIO5.MUX5** to MUX the output signal from the internal digital bus DBUS DB1 to DB7.

7.7.3.3 AIO4 Polarity

Use **SOC.CFGAIO4.POL4** to set logic polarity of the signal between AIO4 input/output and MUX4.

7.7.3.4 AIO5 Polarity

Use **SOC.CFGAIO5.POL5** to set logic polarity of the signal between AIO5 input/output and MUX5.

7.7.4 AIO5, AIO4 differential Amplifier Mode

Set **SOC.CFGAIO4.MODE54** = 01b to use AIO5 and AIO4 as input to a differential amplifier.

7.7.4.1 AIO5, AIO4 Differential Amplifier Gain

Use **SOC.CFGAIO4.GAIN54** to set to gain between 1x to 48x.

7.7.4.2 AIO5, AIO4 Differential Amplifier Reference

Use **SOC.CFGAIO5.OS54EN** to set the amplifier reference either VSSA or VREF/2.

7.7.4.3 AIO5, AIO4 Differential Amplifier Calibration

Use **SOC.CFGAIO5.CAL54EN** to short the input of the differential amplifier to allow reading of the amplifier offset.

7.7.5 AIO5, AIO4 Protection

In **SOC.CFGAIO4.MODE54** = 01b differential amplifier mode, a high side comparator protector HP54 and a low side comparator protector LP54 are also active that can be configured to disabled high-side or low-side drivers in the application specific power driver section.

7.7.5.1 HP54 Comparator

The HP54 comparator takes the AIO5 voltage referenced to VSSA and compares it against the HP-DAC voltage. The 10-bit HP-DAC is programmable with **SOC.HPDACH** and **SOC.HPDACL**.

Use **SOC.CFGAIO5.HP54EN** to enable HP54 comparator with different blanking times.

Use **SOC.SIGSET.HPROTHYS** to enable HP54 comparator hysteresis.

The output of HP54 comparator can be configured to trigger protection signal PR using **SOC.CFGAIO5.HP54PREN**.

The output of HP54 can also trigger the nIRQ1 interrupt using **SOC.PROTINTM.nHP54INTM** to un-mask the interrupt. The real-time status can be observed using **SOC.PROTSTAT.HPROT54STAT** and the latched interrupt status can be observed using **SOC.PROTSTAT.HPROT54**.

7.7.5.2 LP54 Comparator

The LP54 comparator takes the output of the differential amplifier and compares it against the LP-DAC voltage. The 10-bit LP-DAC is programmable with **SOC.LPDACH** and **SOC.LPDACL**.

Use **SOC.CFGAIO4.LP54EN** to enable LP54 comparator with different blanking times.

Use **SOC.SIGSET.LPPROTHYS** to enable LP54 comparator hysteresis.

The output of LP54 comparator can be configured to trigger protection signal PR using **SOC.CFGAIO5.LP54PREN**.

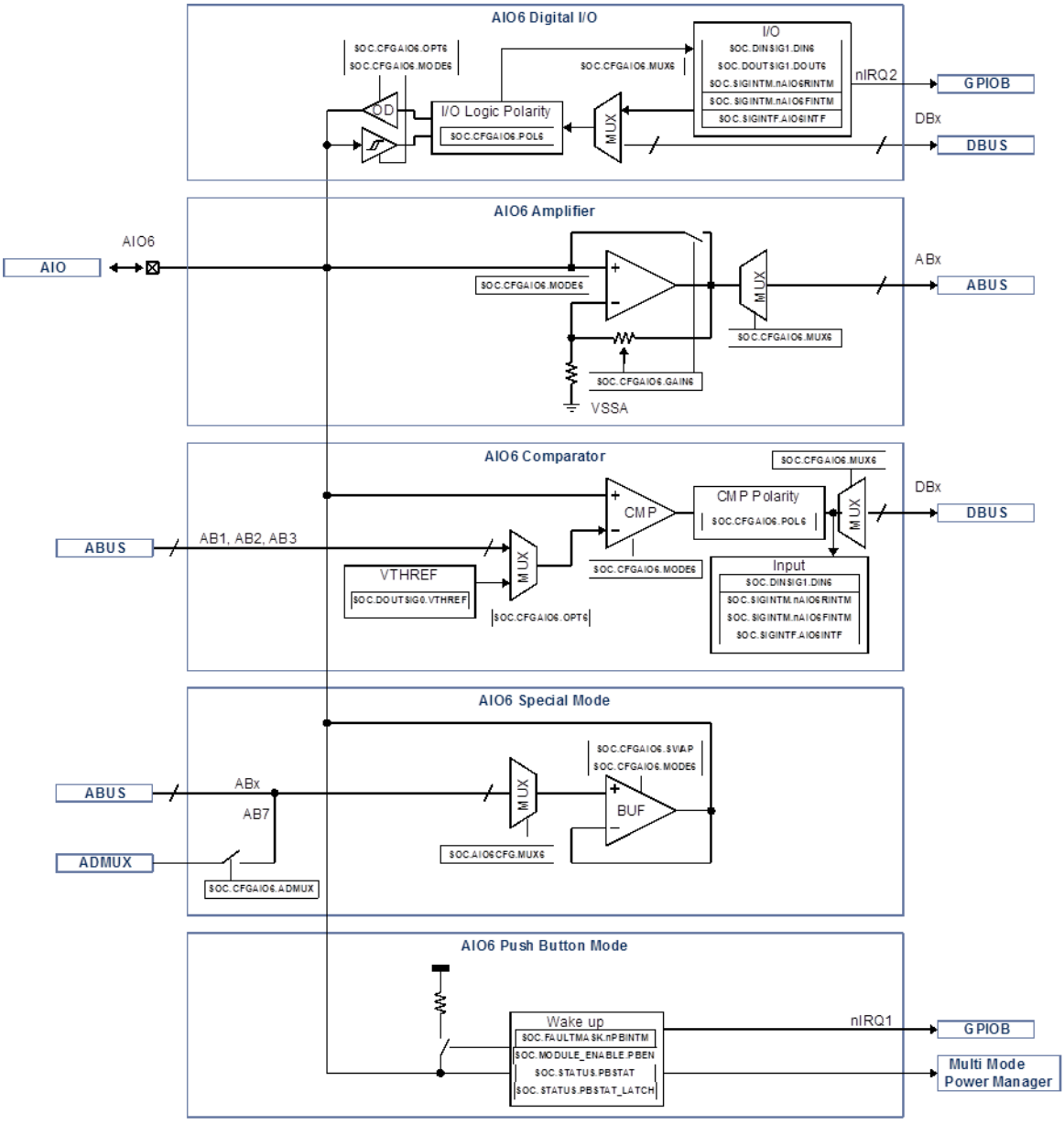
The output of LP54 can also trigger the nIRQ1 interrupt using **SOC.PROTINTM.nLP54INTM** to un-mask the interrupt. The real-time interrupt status can be observed with **SOC.PROTSTAT.LPROT54STAT** and the latched interrupt status can be observed using **SOC.PROTSTAT.LPROT54**.

7.8 AIO6

AIO6 may be configured as a digital input, single-ended programmable gain amplifier, comparator, output from analog ABUS or as a push-button input to wake up the device from total hibernate mode.

7.8.1 System Block Diagram

Figure 7-5 AIO6 System Block Diagram



7.8.2 AIO6

AIO6 can be configured as digital input, as singled ended programmable gain amplifier, as comparator, as output from the analog ABUS or as push button input to wake up the device from low power hibernate mode.

7.8.3 AIO6 digital I/O Mode

Set **SOC.MISC.PBEN** = 0b and **SOC.CFGAIO6.MODE6** = 00b to use AIO6 as digital IO.

7.8.3.1 AIO6 IO

Set **SOC.CFGAIO6.OPT6** = 00b to use AIO6 as input. The input state can be read at **SOC.DINSIG1.DIN6**.

Set **SOC.CFGAIO6.OPT6** = 10b to use AIO6 as open drain output. Set **SOC.CFGAIO6.MUX6** = 00b to MUX the output state from **SOC.DOUTSIG1.DOUT6**. Use **SOC.CFGAIO6.MUX6** to MUX the output signal from the internal digital bus DBUS DB1 to DB7.

7.8.3.2 AIO6 IO Interrupt

Set **SOC.SIGINTM.nAIO6RINTM** to allow nIRQ2 interrupt on AIO6 low high transition.

Set **SOC.SIGINTM. nAIO6FINTM** to allow nIRQ2 interrupt on AIO6 high low transition.

The interrupt status can be monitored with **SOC.SIGINTF.AIO6INTF** and cleared by writing **SOC.SIGINTF.AIO6INTF** to 1b.

7.8.3.3 AIO6 Polarity

Use **SOC.CFGAIO6.POL6** to set logic polarity of the signal between AIO6 input/output and MUX6.

7.8.4 AIO6 Single Ended Amplifier Mode

Set **SOC.MISC.PBEN** = 0b and **SOC.CFGAIO6.MODE6** = 01b to use AIO6 as input to a programmable gain amplifier.

7.8.4.1 AIO6 Amplifier Gain

Use **SOC.CFGAIO6.GAIN6** to set to gain between 1x to 48x or bidirectional amplifier bypassmode.

7.8.4.2 AIO6 Analog MUX

Use **SOC.CFGAIO6.MUX6** to switch the output of the amplifier to analog channel AB1 to AB7 on the analog bus ABUS.

7.8.5 AIO6 Comparator Mode

Set **SOC.MISC.PBEN** = 0b and **SOC.CFGAIO6.MODE6** = 10b to use AIO6 in comparator mode.

7.8.5.1 AIO6 Comparator setting

Use **SOC.CFGAIO6.OPT6** to set the compare value of the comparator to AB1, AB2, AB3 or VTHREF, setable with **SOC.DOUTSIG0.VTHREF**.

7.8.5.2 AIO6 Comparator Polarity

Use **SOC.CFGAIO6.POL6** to set the output polarity of the comparator.

7.8.5.3 AIO6 Comparator Output MUX

Use **SOC.AIO6CFG.MUX6** to set the output of the comparator to the digital bus DB1 to DB7 or **SOC.DINSIG1.DIN6**.

7.8.6 AIO6 Special Mode

Set **SOC.MODULE_ENABLE.PBEN** = 0b and **SOC.CFGAIO6.MODE6** = 11b to use AIO6 in special mode. In special mode the AIO6 can output a buffered signal from the internal ABUS, AB1 to AB7.

7.8.6.1 AIO6 Special Mode MUX

Use **SOC.CFGAIO6.MUX6** to set the ABx channel output to AIO6.

7.8.6.2 AIO6 Special Mode ADMUX

Use **SOC.CFGAIO6.ADMUX** set the MUX the ADMUX output to AB7.

7.8.6.3 AIO6 Special Mode OFFSET SWAP

Use **SOC.CFGAIO6.SWAP** to swap the random offset of the buffer for calibration reasons.

7.8.7 AIO6 Push Button Mode

Set **SOC.MISC.PBEN** = 1b to enable AIO6 Hibernate push button mode, where AIO6 has an internal weak pull up also active in hibernate mode. Set **SOC.FAULTMASK.nPBINTM** = 0b to enable nIRQ1 interrupt.

The real-time status of the push-button may be read using **SOC.STATUS.PBSTAT**. Use **SOC.STATUS.PBSTAT_LATCHED** to monitor interrupt status and write 1b to clear interrupt.

7.8.7.1 AIO6 Push Button Wake Up

In Hibernate Wake Mode and enabled push button mode, if AIO6 is pulled low for the de-bouncing time period, the **SOC.MISC.HIB** is cleared and the device powers up.

7.8.7.2 AIO6 Push Button Power Down

In normal mode the **SOC.STATUS.PBSTAT_LATCHED** is set when AIO6 is pulled low for the de-bouncing time period. The system then can be put into hibernate mode by setting **SOC.MISC.HIB** = 1b.

7.8.7.3 AIO6 Push Button Hard Reset

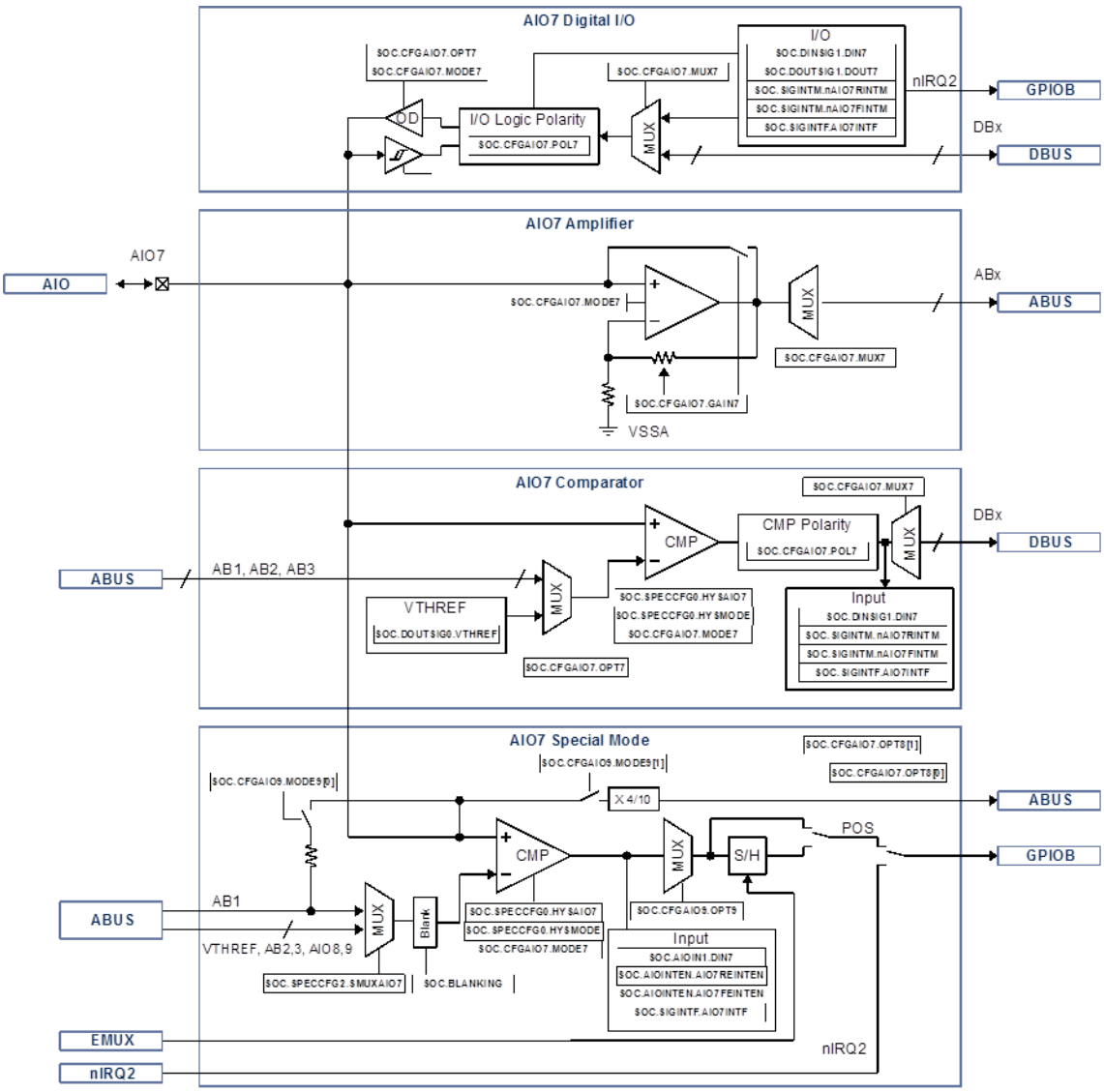
In normal operation if the AIO6 is pulled low for more than 8s, the nRST signal will be asserted and the MCU is reset. **SOC.STATUS.HWRSTAT** is set to indicate this condition.

7.9 AIO7

AIO7 may be configured as a digital input, single-ended programmable gain amplifier, comparator or output from analog ABUS.

7.9.1 System Block Diagram

Figure 7-6 AIO7 System Block Diagram



7.9.2 AIO7

AIO7 can be configured as digital input, as singled ended programmable gain amplifier, as comparator, as output from the analog ABUS or as push button input to wake up the device from low power hibernate mode.

7.9.3 AIO7 digital I/O Mode

Set **SOC.CFGAIO7.MODE7** = 00b to use AIO7 as digital IO.

7.9.3.1 AIO7 IO

Set **SOC.CFGAIO7.OPT7** = 00b to use AIO7 as input. The input state can be read at **SOC.DINSIG1.DIN7**.

Set **SOC.CFGAIO7.OPT7** = 10b to use AIO7 as open drain output. Set **SOC.CFGAIO7.MUX7** = 00b to MUX the output state from **SOC.DOUTSIG1.DOUT7**. Use **SOC.CFGAIO7.MUX7** to MUX the output signal from the internal digital bus DBUS DB1 to DB7.

7.9.3.2 AIO7 IO Interrupt

Set **SOC.SIGINTM.AIO7RINTM** to 0b to allow nIRQ2 interrupt on AIO7 low high transition.

Set **SOC.SIGINTM.AIO7FINTM** to 0b to allow nIRQ2 interrupt on AIO7 high low transition.

The interrupt status can be monitored with **SOC.SIGINTF.AIO7INTF** and cleared by writing **SOC.SIGINTF.AIO7INT** to 1b.

7.9.3.3 1.1.3.3. AIO7 Polarity

Use **SOC.CFGAIO7.POL7** to set logic polarity of the signal between AIO7 input/output and MUX7.

7.9.4 1.1.4. AIO7 Single Ended Amplifier Mode

Set **SOC.CFGAIO7.MODE7** = 01b to use AIO7 as input to a programmable gain amplifier.

7.9.4.1 1.1.4.1. AIO7 Amplifier Gain

Use **SOC.CFGAIO7.GAIN7** to set to gain between 1x to 48x or bidirectional amplifier bypassmode.

7.9.4.2 1.1.4.2. AIO7 Analog MUX

Use **SOC.CFGAIO7.MUX7** to switch the output of the amplifier to analog channel AB1 to AB7 on the analog bus ABUS.

7.9.5 1.1.5. AIO7 Comparator Mode

Set **SOC.CFGAIO7.MODE7** = 10b to use AIO7 in comparator mode.

7.9.5.1 AIO7 Comparator Hysteresis

Use **SOC.SPECCFG0.HYSMODE** and **SOC.SPECCFG0.HYSAIO7** to configure AIO7 comparator hysteresis.

7.9.5.2 AIO7 Comparator Reference

Use **SOC.CFGAIO7.OPT7** to set the compare value of the comparator to AB1, AB2, AB3 or VTHREF, setable with **SOC.DOUTSIG0.VTHREF**.

7.9.5.3 AIO7 Comparator Polarity

Use **SOC.CFGAIO7.POL7** to set the output polarity of the comparator.

7.9.5.4 AIO7 Comparator Output

The comparator output can be observed with **SOC.DINSIG1.DIN7**.

7.9.6 AIO7 Special Mode

Set **SOC.CFGAIO7.MODE7** = 11b to use AIO7 in special mode. In special mode the AIO7 comparator is enabled.

7.9.6.1 AIO7 Comparator Hysteresis

Use **SOC.SPECCFG0.HYSMODE** and **SOC.SPECCFG0.HYSAIO7** to configure AIO7 special mode comparator hysteresis.

7.9.6.2 AIO7 Comparator Reference

Use **SOC.SPECCFG2.SMUXAIO7** to set the compare value of the comparator to VTHREF, AB1, AB2, AB3 as well as AIO8 or AIO9 for phase to phase comparator functions.

7.9.6.3 AIO7 Comparator Reference Star Point

Use **SOC.CFGAIO9.MODE9[0]** =1b to connect AIO7, AIO8 and AIO9 to AB1 with a 100kOhm resistor to create a star point reference for the comparator.

With **SOC.CFGAIO9.MODE9[0]** =0b, the AB1 reference could for example come from AIO6 in amplifier mode **SOC.CFGAIO6.MODE6** = 01b and **SOC.CFGAIO6.GAIN6** = 000b direct mode and **SOC.CFGAIO6.MUX6** = 1b.

7.9.6.4 AIO7 Voltage Reading

Use **SOC.CFGAIO9.MODE9[1]** =1b to MUX AIO7 to AB7 with 40% attenuation, so ADC can read out AIO7 voltage.

7.9.6.5 AIO7 Comparator Output

Use **SOC.CFGAIO9.OPT9** to select AIO7, AIO8 or AIO9 comparator output signal for POS.

7.9.6.6 AIO7 POS S/H Bypass

Set **SOC.CFGAIO8.OPT8[1]** =0b bypass the POS S/H.

Set **SOC.CFGAIO8.OPT8[1]** =1b use POS S/H for use with EMUX.

7.9.6.7 AIO7 nIRQ2/POS Selector

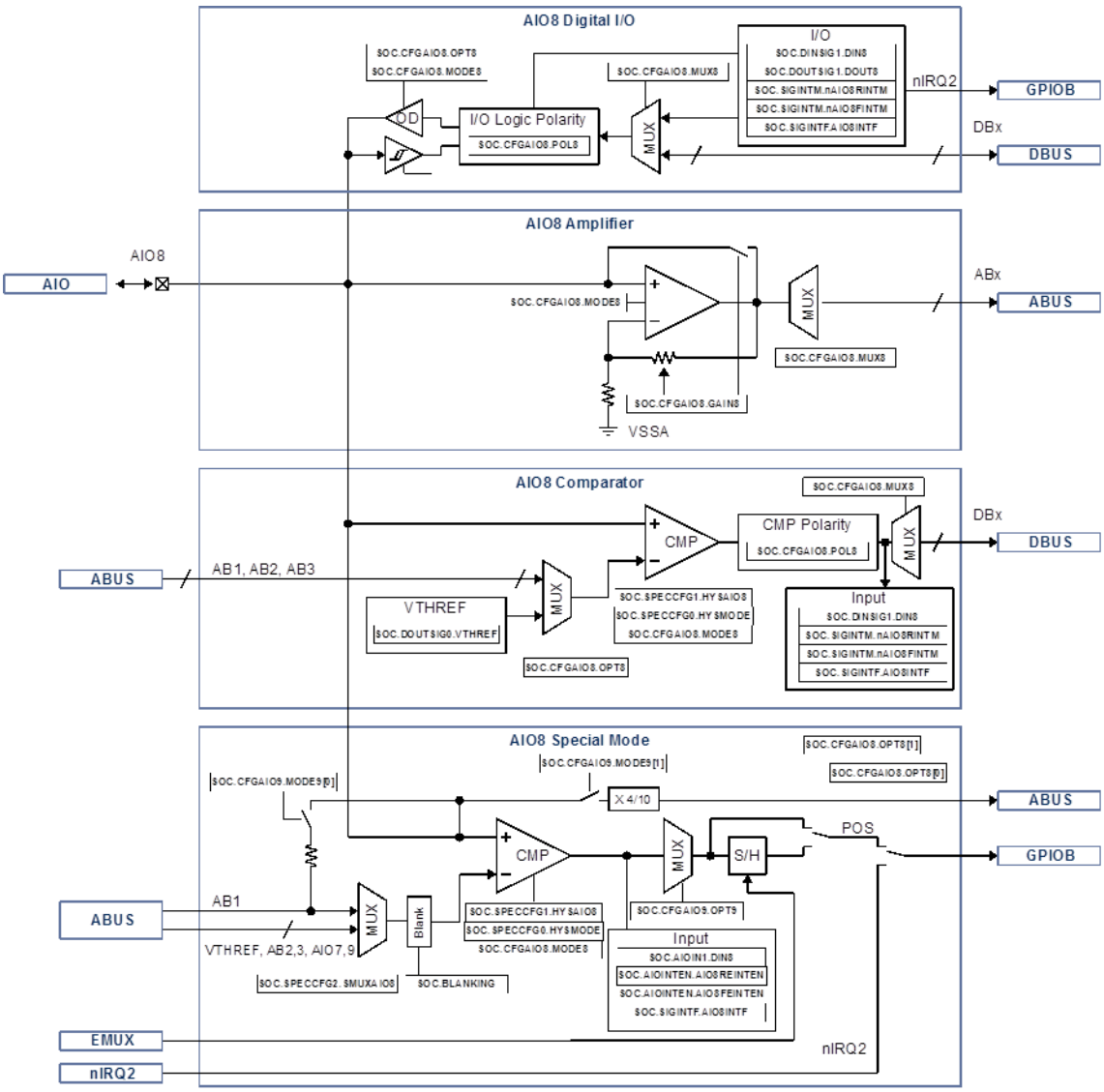
Use **SOC.CFGAIO8.OPT8[0]** to select POS or nIRQ2 output.

7.10 AIO8

AIO8 may be configured as a digital input, single-ended programmable gain amplifier, comparator or output from analog ABUS.

7.10.1 System Block Diagram

Figure 7-7 AIO8 System Block Diagram



7.10.2 AIO8

AIO8 can be configured as digital input, as singled ended programmable gain amplifier, as comparator, as output from the analog ABUS or as push button input to wake up the device from low power hibernate mode.

7.10.3 AIO8 digital I/O Mode

Set **SOC.CFGAIO8.MODE8** = 00b to use AIO8 as digital IO.

7.10.3.1 AIO8 IO

Set **SOC.CFGAIO8.OPT8** = 00b to use AIO8 as input. The input state can be read at **SOC.DINSIG1.DIN8**.

Set **SOC.CFGAIO8.OPT8** = 10b to use AIO8 as open drain output. Set **SOC.CFGAIO8.MUX8** = 00b to MUX the output state from **SOC.DOUTSIG1.DOUT8**. Use **SOC.CFGAIO8.MUX8** to MUX the output signal from the internal digital bus DBUS DB1 to DB8.

7.10.3.2 AIO8 IO Interrupt

Set **SOC.SIGINTM.AIO8RINTM** to 0b to allow nIRQ2 interrupt on AIO8 low high transition.

Set **SOC.SIGINTM.AIO8FINTM** to 0b to allow nIRQ2 interrupt on AIO8 high low transition.

The interrupt status can be monitored with **SOC.SIGINTF.AIO8INTF** and cleared by writing **SOC.SIGINTF.AIO8INT** to 1b.

7.10.3.3 AIO8 Polarity

Use **SOC.CFGAIO8.POL8** to set logic polarity of the signal between AIO8 input/output and MUX8.

7.10.4 AIO8 Single Ended Amplifier Mode

Set **SOC.CFGAIO8.MODE8** = 01b to use AIO8 as input to a programmable gain amplifier.

7.10.4.1 AIO8 Amplifier Gain

Use **SOC.CFGAIO8.GAIN8** to set to gain between 1x to 48x or bidirectional amplifier bypassmode.

7.10.4.2 AIO8 Analog MUX

Use **SOC.CFGAIO8.MUX8** to switch the output of the amplifier to analog channel AB1 to AB8 on the analog bus ABUS.

7.10.5 AIO8 Comparator Mode

Set **SOC.CFGAIO8.MODE8** = 10b to use AIO8 in comparator mode.

7.10.5.1 AIO8 Comparator Hysteresis

Use **SOC.SPECCFG0.HYSMODE** and **SOC.SPECCFG1.HYSAIO8** to configure AIO8 comparator hysteresis.

7.10.5.2 AIO8 Comparator Reference

Use **SOC.CFGAIO8.OPT8** to set the compare value of the comparator to AB1, AB2, AB3 or VTHREF, setable with **SOC.DOUTSIG0.VTHREF**.

7.10.5.3 AIO8 Comparator Polarity

Use **SOC.CFGAIO8.POL8** to set the output polarity of the comparator.

7.10.5.4 AIO8 Comparator Output

The comparator output can be observed with **SOC.DINSIG1.DIN8**.

7.10.6 AIO8 Special Mode

Set **SOC.CFGAIO8.MODE8** = 11b to use AIO8 in special mode. In special mode the AIO8 comparator is enabled.

7.10.6.1 AIO8 Comparator Hysteresis

Use **SOC.SPECCFG0.HYSMODE** and **SOC.SPECCFG0.HYSAIO8** to configure AIO8 special mode comparator hysteresis.

7.10.6.2 AIO8 Comparator Reference

Use **SOC.SPECCFG2.SMUXAIO8** to set the compare value of the comparator to VTHREF, AB1, AB2, AB3 as well as AIO7 or AIO9 for phase to phase comparator functions.

7.10.6.3 AIO8 Comparator Reference Star Point

Use **SOC.CFGAIO9.MODE9[0]** =1b to connect AIO8, AIO8 and AIO9 to AB1 with a 100kOhm resistor to create a star point reference for the comparator.

With **SOC.CFGAIO9.MODE9[0]** =0b, the AB1 reference could for example come from AIO6 in amplifier mode **SOC.CFGAIO6.MODE6** = 01b and **SOC.CFGAIO6.GAIN6** = 000b direct mode and **SOC.CFGAIO6.MUX6** = 1b.

7.10.6.4 AIO8 Voltage Reading

Use **SOC.CFGAIO9.MODE9[1]** =1b to MUX AIO8 to AB8 with 40% attenuation, so ADC can read out AIO8 voltage.

7.10.6.5 AIO8 Comparator Output

Use **SOC.CFGAIO9.OPT9** to select AIO8, AIO8 or AIO9 comparator output signal for POS.

7.10.6.6 AIO8 POS S/H Bypass

Set **SOC.CFGAIO8.OPT8[1]** =0b bypass the POS S/H.

Set **SOC.CFGAIO8.OPT8[1]** =1b use POS S/H for use with EMUX.

7.10.6.7 AIO8 nIRQ2/POS Selector

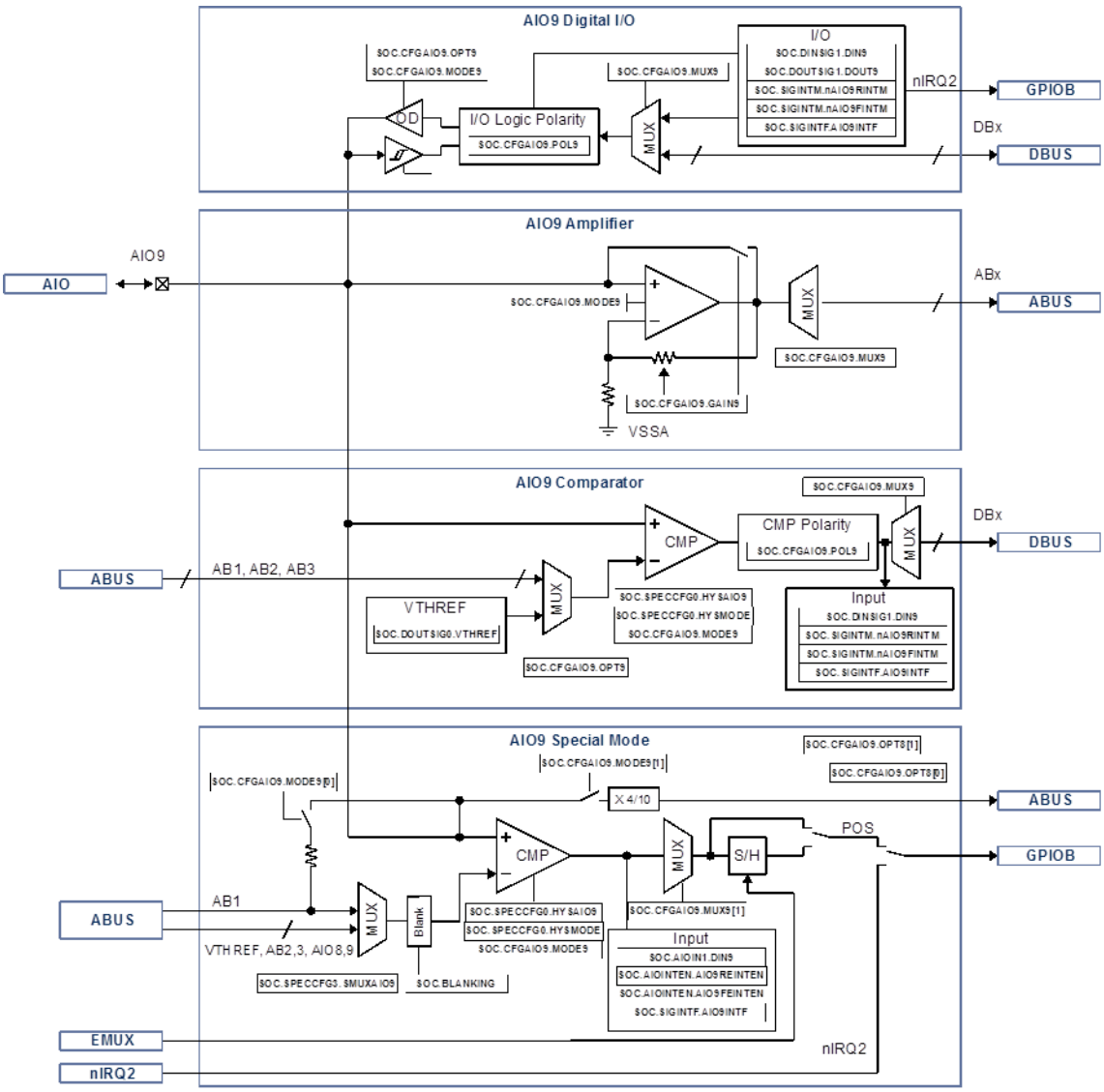
Use **SOC.CFGAIO8.OPT8[0]** to select POS or nIRQ2 output.

7.11 AIO9

AIO9 may be configured as a digital input, single-ended programmable gain amplifier, comparator or output from analog ABUS.

7.11.1 System Block Diagram

Figure 7-8 AIO9 System Block Diagram



7.11.2 AIO9

AIO9 can be configured as digital input, as singled ended programmable gain amplifier, as comparator, as output from the analog ABUS or as push button input to wake up the device from low power hibernate mode.

7.11.3 AIO9 digital I/O Mode

Set **SOC.CFGAIO9.MODE9** = 00b to use AIO9 as digital IO.

7.11.3.1 AIO9 IO

Set **SOC.CFGAIO9.OPT9** = 00b to use AIO9 as input. The input state can be read at **SOC.DINSIG1.DIN9**.

Set **SOC.CFGAIO9.OPT9** = 10b to use AIO9 as open drain output. Set **SOC.CFGAIO9.MUX9** = 00b to MUX the output state from **SOC.DOUTSIG1.DOUT9**. Use **SOC.CFGAIO9.MUX9** to MUX the output signal from the internal digital bus DBUS DB1 to DB9.

7.11.3.2 AIO9 IO Interrupt

Set **SOC.SIGINTM.AIO9RINTM** to 0b to allow nIRQ2 interrupt on AIO9 low high transition.

Set **SOC.SIGINTM.AIO9FINTM** to 0b to allow nIRQ2 interrupt on AIO9 high low transition.

The interrupt status can be monitored with **SOC.SIGINTF.AIO9INTF** and cleared by writing **SOC.SIGINTF.AIO9INT** to 1b.

7.11.3.3 AIO9 Polarity

Use **SOC.CFGAIO9.POL9** to set logic polarity of the signal between AIO9 input/output and MUX9.

7.11.4 AIO9 Single Ended Amplifier Mode

Set **SOC.CFGAIO9.MODE9** = 01b to use AIO9 as input to a programmable gain amplifier.

7.11.4.1 AIO9 Amplifier Gain

Use **SOC.CFGAIO9.GAIN9** to set to gain between 1x to 48x or bidirectional amplifier bypassmode.

7.11.4.2 AIO9 Analog MUX

Use **SOC.CFGAIO9.MUX9** to switch the output of the amplifier to analog channel AB1 to AB9 on the analog bus ABUS.

7.11.5 AIO9 Comparator Mode

Set **SOC.CFGAIO9.MODE9** = 10b to use AIO9 in comparator mode.

7.11.5.1 AIO9 Comparator Hysteresis

Use **SOC.SPECCFG0.HYSMODE** and **SOC.SPECCFG0.HYSAIO9** to configure AIO9 comparator hysteresis.

7.11.5.2 AIO9 Comparator Reference

Use **SOC.CFGAIO9.OPT9** to set the compare value of the comparator to AB1, AB2, AB3 or VTHREF, setable with **SOC.DOUTSIG0.VTHREF**.

7.11.5.3 AIO9 Comparator Polarity

Use **SOC.CFGAIO9.POL9** to set the output polarity of the comparator.

7.11.5.4 AIO9 Comparator Output

The comparator output can be observed with **SOC.DINSIG1.DIN9**.

7.11.6 AIO9 Special Mode

Set **SOC.CFGAIO9.MODE9** = 11b to use AIO9 in special mode. In special mode the AIO9 comparator is enabled.

7.11.6.1 AIO9 Comparator Hysteresis

Use **SOC.SPECCFG0.HYSMODE** and **SOC.SPECCFG1.HYSAIO9** to configure AIO9 special mode comparator hysteresis.

7.11.6.2 AIO9 Comparator Reference

Use **SOC.SPECCFG3.SMUXAIO9** to set the compare value of the comparator to VTHREF, AB1, AB2, AB3 as well as AIO8 or AIO9 for phase to phase comparator functions.

7.11.6.3 AIO9 Comparator Reference Star Point

Use **SOC.CFGAIO9.MODE9[0]** =1b to connect AIO9, AIO8 and AIO9 to AB1 with a 100kOhm resistor to create a star point reference for the comparator.

With **SOC.CFGAIO9.MODE9[0]** =0b, the AB1 reference could for example come from AIO6 in amplifier mode **SOC.CFGAIO6.MODE6** = 01b and **SOC.CFGAIO6.GAIN6** = 000b direct mode and **SOC.CFGAIO6.MUX6** = 1b.

7.11.6.4 AIO9 Voltage Reading

Use **SOC.CFGAIO9.MODE9[1]** =1b to MUX AIO9 to AB9 with 40% attenuation, so ADC can read out AIO9 voltage.

7.11.6.5 AIO9 Comparator Output

Use **SOC.CFGAIO9.OPT9** to select AIO9, AIO8 or AIO9 comparator output signal for POS.

7.11.6.6 AIO9 POS S/H Bypass

Set **SOC.CFGAIO8.OPT8[1]** =0b bypass the POS S/H.

Set **SOC.CFGAIO8.OPT8[1]** =1b use POS S/H for use with EMUX.

7.11.6.7 AIO9 nIRQ2/POS Selector

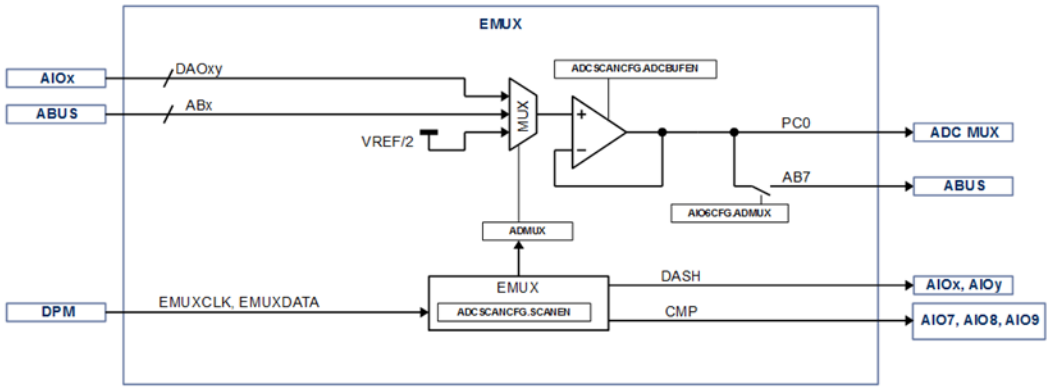
Use **SOC.CFGAIO8.OPT8[0]** to select POS or nIRQ2 output.

7.12 EMUX and ADMUX

The EMUX is a dedicated high-speed, low-latency serial interface to control the ADMUX, AIO7, AIO8, AIO9 POS S/H and the DAOxy S/H using the ADC DTSE sequencing engine.

7.12.1 System Block Diagram

Figure 7-9 EMUX and ADMUX System Block Diagram



7.12.2 EMUX

The EMUX is a dedicated high-speed low-latency serial interface to control the ADMUX, AIO7, AIO8, AIO9 POS S/H and the DAOxy S/H using the ADC DTSE.

7.12.3 EMUX Enable

Set **SOC.ADCSCAN.EMUX_EN** to 01b to enable the EMUX control of the **SOC.ADIN1** and DAIOxy sample and hold.

7.12.4 EMUXD Packet Structure

The EMUXD packet is transmitted MSB first.

Table 7-1 EMUX Message Format

BIT	NAME	DESCRIPTION
7	**COMP_SH**	EMUX Reset. This bit is always read as 0b. 1b: Reset EMUX
6	**HLD2**	DAO54 Sample and Hold Output: 1b: Hold 0b: Sample
5	**HLD1**	DAO32 Sample and Hold Output: 1b: Hold 0b: Sample
4	**HLD0**	DAO10 Sample and Hold Output: 1b: Hold 0b: Sample

3:0	**MUXA**	ADC MUX Selection: 1111b: VREF / 2 1110b: AB12 1101b: AB11 1100b: AB10 1011b: AB9 1010b: AB8 1001b: AB7 1000b: AB6 0111b: AB5 0110b: AB4 0101b: AB3 0100b: AB2 0011b: AB1 0010b: DAO54 0001b: DAO32 0000b: DAO10

The EMUXD packet is transmitted MSB first.

The BEMF sample and hold is toggled based on the COMP_SH bit in the EMUXD packet with the falling edge of the 1st clock cycle.

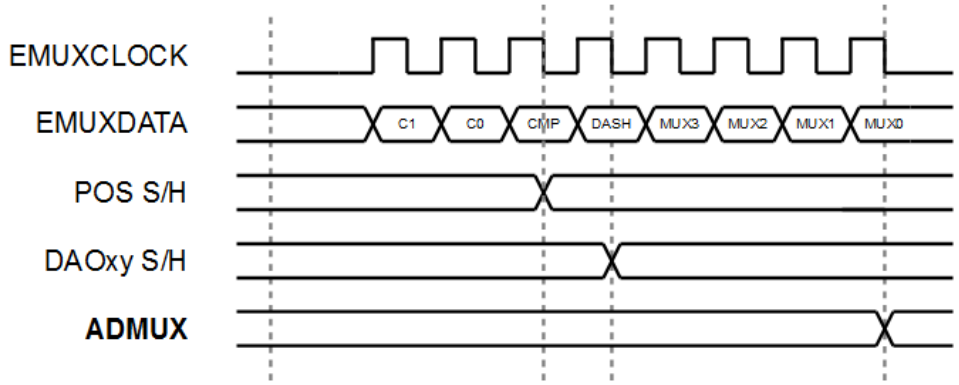
The DAO54 sample and hold is toggled based on the HLD2 bit in the EMUXD packet with the falling edge of the 2nd clock cycle.

The DAO32 sample and hold is toggled based on the HLD1 bit in the EMUXD packet with the falling edge of the 3rd clock cycle.

The DAO10 sample and hold is toggled based on the HLD0 bit in the EMUXD packet with the falling edge of the 4th clock cycle.

The ADMUX is switched with the falling edge of the 8th clock based on the data of bits 3:0 of the EMUXD packet.

Figure 7-10 EMUX Timing Diagram



7.12.5 ADMUX

The ADMUX is a dedicated analog MUX in the configurable analog front-end.

7.12.5.1 ADMUX Control

Use **SOC.ADIN1** to set the channel for the ADMUX.

When EMUX is enabled, the SOC.ADMUX can be controlled directly from the ASC0, ASC1 sequencers using EMUXD.

7.12.5.2 ADMUX Buffer

Use **SOC.ADCSCAN.ADCBUFEN** to enable the ADMUX buffer.

7.12.5.3 ADMUX

Use **SOC.AIO6CFG.ADIN1** to route the output of the ADMUX to AB7 for debug purposes.

7.13 Register Summary

Table 7-2 CAFE Register Summary

ADDRESS	REGISTER	DESCRIPTION	RESET
0x06	**SOC.CFGAIO0**	AIO0 Configuration	0x00
0x07	**SOC.CFGAIO1**	AIO1 Configuration	0x00
0x08	**SOC.CFGAIO2**	AIO2 Configuration	0x00
0x09	**SOC.CFGAIO3**	AIO3 Configuration	0x00
0x0A	**SOC.CFGAIO4**	AIO4 Configuration	0x00
0x0B	**SOC.CFGAIO5**	AIO5 Configuration	0x00
0x0C	**SOC.CFGAIO6**	AIO6 Configuration	0x00
0x0D	**SOC.CFGAIO7**	AIO7 Configuration	0x00
0x0E	**SOC.CFGAIO8**	AIO8 Configuration	0x00
0x0F	**SOC.CFGAIO9**	AIO9 Configuration	0x00
0x10	**SOC.SIGSET**	Signal manager Configuration	0x00
0x11	**SOC.HPDACH**	High Protection Threshold	0x00
0x12	**SOC.HPDACL**	High Protection Threshold	0x00
0x13	**SOC.LPDACH**	Low Protection Threshold	0x00
0x14	**SOC.LPDACL**	Low Protection Threshold	0x00
0x15	**SOC.SHCFG1**	Sample and Hold Configuration 1	0x00
0x16	**SOC.SHCFG2**	Sample and Hold Configuration 2	0x00
0x17	**SOC.PROTINTM**	Driver Protection Interrupt Mask	0x00
0x18	**SOC.PROTSTAT**	Driver Protection Interrupt Status	0x00
0x19	**SOC.DOUTSIG0**	AIO Data Output 0	0x00
0x1A	**SOC.DOUTSIG1**	AIO Data Output 1	0x00
0x1B	**SOC.DINSIG0**	AIO Data Input 0	0x00
0x1C	**SOC.DINSIG1**	AIO Data Input 1	0x00
0x1D	**SOC.CFGIO1**	AIO10-AIO13 Configuration 0	0x00
0x1E	**SOC.CFGIO2**	AIO10-AIO13 Configuration 1	0x00
0x1F	**SOC.SIGINTM**	AIO Interrupt Mask Configuration	0x00
0x20	**SOC.SIGINTF**	AIO Interrupt Flag Status	0x00
0x21	**SOC.BLANKING**	BEMF Comparator Blanking Configuration	0x00
0x22	**SOC.SPECCFG0**	AIO7 Hysteresis Configuration	0x00
0x23	**SOC.SPECCFG1**	AIO8/AIO9 Hysteresis Configuration	0x00
0x24	**SOC.SPECCFG2**	AIO7/AIO8 Comparator Input MUX Configuration	0x00
0x25	**SOC.SPECCFG3**	AIO9 Comparator Input MUX Configuration	0x00

7.14 Register Detail

7.14.1 SOC.CFGAIO0

Register 7-1 SOC.CFGAIO0 (AIO0 Configuration, 06h)

BIT	NAME	ACCESS	RESET	IO MODE	DIFFAMP MODE
7:6	**MODE10**	RW	00b	00b	01b
5:4	**OPT0**	RW	00b	**OPT0**: AIO0 Option: 00b: Input 01b: Hi-Z 10b: Open-drain output 11b: Hi-Z	**GAIN10:** Differential amplifier gain setting: 000b: 1x 010b: 1x 011b: 2x 001b: 4x 100b: 8x 101b: 16x 110b: 32x 111b: 48x
3	**POL0**	RW	0b	**POL0**: AIO0 Polarity If **CFGAIO0.OPT0** = 00b, AIO0 input polarity setting. If **CFGAIO0.OPT0** = 10b, AIO0 output polarity setting: 0b: active high 1b: active low	
2	**MUX0**	RW	0b	**MUX0**: AIO0 Digital MUX setting: 000b: DATAIO0 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	Reserved
1:0		RW	00b		**LP10EN:** LP10 Comparator option: 00b: disabled 01b: 1µs blanking time 10b: 2µs blanking time 11b: 4µs blanking time

7.14.2 SOC.CFGAIO1

Register 7-2 SOC.CFGAIO1 (AIO1 Configuration, 07h)

BIT	NAME	ACCESS	RESET	IO MODE	DIFFAMP MODE
7:6	**RFU**	R	00b	Reserved	Reserved
5:4	**OPT1**	RW	0b	**OPT1**: AIO1 IO Option: 00b: Input 01b: Hi-Z 10b: Open-drain output 11b: Hi-Z	**HP10PREN:** HPROT10 PR Protection enable: 0b: HP10 output to PR disabled 1b: HP10 output to PR enabled
		RW	0b		**LP10PREN:** LPROT10 PR Protection enable: 0b: LP10 output to PR disabled 1b: LP10 output to PR enabled
3	**POL1**	RW	0b	If **CFGAIO1.OPT1** = 00b, AIO1 input polarity setting. If **CFGAIO1.OPT1** = 10b, AIO1 output polarity setting: 0b: active high 1b: active low	**OS10EN:** Differential Amplifier Offset: 0b: Offset disabled 1b: Offset enabled, input signal shifted by $V_{REF}/2$
2	**MUX1**	RW	0b	**MUX1**: AIO1 Digital MUX: 000b: DATAIO1 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	**CAL10EN:** Differential Amplifier Offset Calibration: 0b: disabled 1b: enabled
1:0		RW	00b		**HP10EN:** HP10 Comparator setting: 00b: disabled 01b: 1µs blanking time 10b: 2µs blanking time 11b: 4µs blanking time

7.14.3 SOC.CFGAIO2

Register 7-3 SOC.CFGAIO2 (AIO2 Configuration, 08h)

BIT	NAME	ACCESS	RESET	IO MODE	DIFFAMP MODE
7:6	**MODE32**	RW	00b	00b	01b
5:4	**OPT2**	RW	0b	**OPT2**: AIO2 Option: 00b: Input 01b: Hi-Z 10b: Open-drain output 11b: Hi-Z	**GAIN32:** Differential amplifier gain setting: 000b: 1x 010b: 1x 011b: 2x 001b: 4x 100b: 8x 101b: 16x 110b: 32x 111b: 48x
3	**POL2**	RW	0b	If **CFGAIO2.OPT2** = 00b, AIO2 input polarity setting. If **CFGAIO2.OPT2** = 10b, AIO2 output polarity setting: 0b: active high 1b: active low	
2	**MUX2**	RW	0b	**MUX2**: AIO0 Digital MUX setting: 000b: DATAIO2 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	Reserved
1:0		RW	0b		**LP32EN:** LP32 Comparator setting: 00b: disabled 01b: 1µs blanking time 10b: 2µs blanking time 11b: 4µs blanking time

7.14.4 SOC.CFGAIO3

Register 7-4 SOC.CFGAIO3 (AIO3 Configuration, 09h)

BIT	NAME	ACCESS	RESET	IO MODE	DIFFAMP MODE
7:6	**RFU**	RW	0b	Reserved	Reserved
5	**OPT3**	RW	0b	**OPT3**: AIO3 IO Option: 00b: Input 01b: Hi-Z 10b: Open-drain output 11b: Hi-Z	**HP32PREN:** HPROT32 PR Protection enable: 0b: HP32 output to PR disabled 1b: HP32 output to PR enabled
4		RW	0b		**LP32PREN:** LPROT32 PR Protection enable: 0b: LP32 output to PR disabled 1b: LP32 output to PR enabled
3	**POL3**	RW	0b	If **CFGAIO3.OPT3** = 00b, AIO3 input polarity setting If **CFGAIO3.OPT3** = 10b, AIO3 output polarity setting: 0b: active high 1b: active low	**OS32EN:** Differential Amplifier Offset: 0b: Offset disabled 1b: Offset enabled, input signal shifted by $V_{REF}/2$
2	**MUX3**	RW	0b	**MUX3**: AIO3 Digital MUX: 000b: DATAIO3 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	**CAL32EN:** Differential Amplifier Offset Calibration: 0b: disabled 1b: enabled
1:0		RW	00b		**HP32EN:** HP32 Comparator setting: 00b: disabled 01b: 1µs blanking time 10b: 2µs blanking time 11b: 4µs blanking time

7.14.5 SOC.CFGAIO4

Register 7-5 SOC.CFGAIO4 (AIO4 Configuration, 0Ah)

BIT	NAME	ACCESS	RESET	IO MODE	DIFFAMP MODE
7:6	**MODE54**	RW	00b	00b	01b
5:4	**OPT4**	RW	0b	**OPT4**: AIO4 IO Option: 00b: Input 01b: Hi-Z 10b: Open-drain output 11b: Hi-Z	**GAIN54:** Differential amplifier gain setting: 000b: 1x 010b: 1x 011b: 2x 001b: 4x 100b: 8x 101b: 16x 110b: 32x 111b: 48x
3	**POL4**	RW	0b	If **CFGAIO4.OPT4** = 00b, AIO4 input polarity setting. If **CFGAIO4.OPT4** = 10b, AIO4 output polarity setting: 0b: active high 1b: active low	
2	**MUX4**	RW	0b	**MUX4**: AIO4 Digital MUX: 000b: DATAIO4 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	Reserved
		RW	00b		**LP54EN:** LP54 Comparator setting: 00b: disabled 01b: 1µs blanking time 10b: 2µs blanking time 11b: 4µs blanking time

7.14.6 SOC.CFGAIO5

Register 7-6 SOC.CFGAIO5 (AIO5 Configuration, 0Bh)

BIT	NAME	ACCESS	RESET	IO MODE	DIFFAMP MODE
7:6	**RFU**	RW	0b	Reserved	Reserved
5	**OPT5**	RW	0b	**OPT5**: AIO5 IO Option: 00b: Input 01b: Hi-Z 10b: Open-drain output 11b: Hi-Z	**HP54PREN:** HPROT54 PR Protection enable: 0b: HP54 output to PR disabled 1b: HP54 output to PR enabled
4		RW	0b		**LP54PREN:** LPROT54 PR Protection enable: 0b: LP54 output to PR disabled 1b: LP54 output to PR enabled
3	**POL5**	RW	0b	If **CFGAIO5.OPT5** = 00b, AIO5 input polarity setting. If **CFGAIO5.OPT5** = 10b, AIO5 output polarity setting: 0b: active high 1b: active low	**OS54EN:** Differential Amplifier Offset: 0b: Offset disabled 1b: Offset enabled, input signal shifted by $V_{REF}/2$
2	**MUX5**	RW	0b	**MUX5**: AIO5 Digital MUX: 000b: DATAIO5 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	**CAL54EN:** Differential Amplifier Offset Calibration: 0b: disabled 1b: enabled
1:0		RW	00b		**HP54EN:** HP54 Comparator setting: 00b: disabled 01b: 1µs blanking time 10b: 2µs blanking time 11b: 4µs blanking time

7.14.7 SOC.CFGAIO6

Register 7-7 SOC.CFGAIO6 (AIO6 Configuration, 0Ch)

BIT	IO MODE	GAIN MODE	COMPARATOR MODE	SPECIAL MODE
7:6	**MODE6:** 00b	**MODE6:** 01b	**MODE6:** 10b	**MODE6:** 11b
5	**OPT6:** AIO6 IO Option: 00b: Input 01b: Hi-Z 10b: Open-drain output 11b: Hi-Z	**GAIN6:** AIO6 Amplifier gain setting: 000b: Gain amplifier bypass, direct mode 001b: 1x 010b: 2x 011b: 4x 100b: 8x 101b: 16x 110b: 32x 111b: 48x	**OPT6:** AIO6 Comparator Reference select: 00b: VTHREF 01b: AB1 10b: AB2 11b: AB3	**ADMUX:** 1b: Switch ADCIN to AB7
4				**SWAP:** Buffer Swap: 0b: Do not swap buffer offset 1b: Swap buffer offset
3	**POL6:** AIO6 Polarity Setting: 00b: active-high 01b: active-low		**POL6:** AIO6 Comparator output polarity setting: 0b: active-high 1b: active-low	Reserved, write to 0b
2:0	**MUX6:** AIO6 Digital MUX Setting: 000b: DATAIO6 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	**MUX6:** Analog MUX Setting: 000b: AB6 001b: AB1 010b: AB2 011b: AB3 100b: AB4 101b: AB5 110b: AB6 111b: AB7	**MUX6:** AIO6 Digital MUX Setting: 000b: DATAIO6 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	**MUX6:** Analog MUX Setting: 000b: AB6 001b: AB1 010b: AB2 011b: AB3 100b: AB4 101b: AB5 110b: AB6 111b: AB7

7.14.8 SOC.CFGAIO7

Register 7-8 SOC.CFGAIO7 (AIO7 Configuration, 0Dh)

BIT	IO MODE	GAIN MODE	COMPARATOR MODE	SPECIAL MODE
7:6	**MODE7:** 00b	**MODE7:** 01b	**MODE7:** 10b	**MODE7:** 11b
5	**OPT7:** AIO7 IO Option: 00b: Input 01b: Hi-Z 10b: Open-drain output 11b: Hi-Z	**GAIN7:** AIO7 Amplifier gain setting: 000b: Gain amplifier bypass, direct mode 001b: 1x 010b: 2x 011b: 4x 100b: 8x 101b: 16x 110b: 32x 111b: 48x	**OPT7:** AIO7 Comparator Reference select: 00b: VTHREF 01b: AB1 10b: AB2 11b: AB3	Reserved, write as 0b
4				Reserved, write as 0b
3	**POL7**: AIO7 Polarity Setting: 00b: active-high 01b: active-low		**POL7:** AIO7 Comparator polarity setting: 0b: active-high 1b: active-low	**POL7:** AIO7 Comparator polarity setting: 0b: active-high 1b: active-low
2:0	**MUX7:** AIO7 Digital MUX: 000b: DATAIO7 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	**MUX7:** AIO7 Analog MUX Setting: 000b: AB7 001b: AB1 010b: AB2 011b: AB3 100b: AB4 101b: AB5 110b: AB6 111b: AB7	**MUX7:** AIO7 Digital MUX: 000b: DATAIO7 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	Reserved, write as 000b

7.14.9 SOC.CFGAIO8

Register 7-9 SOC.CFGAIO8 (AIO8 Configuration, 0Eh)

BIT	IO MODE	GAIN MODE	COMPARATOR MODE	SPECIAL MODE
7:6	**MODE8:** 00b	**MODE8:** 01b	**MODE8:** 10b	**MODE8:** 11b
5	**OPT8:** AIO8 IO Option: 00b: Input 01b: Hi-Z 10b: Open-drain output 11b: Hi-Z	**GAIN8** Amplifier gain setting: 000b: Gain amplifier bypass, direct mode 001b: 1x 010b: 2x 011b: 4x 100b: 8x 101b: 16x 110b: 32x 111b: 48x	**OPT8:** AIO8 Comparator Reference select: 00b: VTHREF 01b: AB1 10b: AB2 11b: AB3	**OPT8[1]:** S/H bypass for POS: 0b: Bypass S/H for POS signal 1b: Do not bypass S/H for POS signal
4				**OPT8[2]:** nIRQ2/POS output: 0b: Select nIRQ2/POS output POS (BEMF) 1b: Select nIRQ2/POS output nIRQ2 (INT)
3	**POL8:** AIO8 Polarity Setting: 00b: active-high 01b: active-low		**POL8:** AIO8 Comparator polarity setting: 0b: active-high 1b: active-low	**POL8:** AIO8 Comparator polarity setting: 0b: active-high 1b: active-low
2:0	**MUX8:** AIO8 Digital MUX: 000b: DATAIO8 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	**MUX8:** AIO8 Analog MUX: 000b: AB8 001b: AB1 010b: AB2 011b: AB3 100b: AB4 101b: AB5 110b: AB6 111b: AB7	**MUX8:** AIO8 Digital MUX: 000b: DATAIO8 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	Reserved, write as 000b.

7.14.10 SOC.CFGAIO9

Register 7-10 SOC.CFGAIO9 (AIO9 Configuration, 0Fh)

BIT	IO MODE	GAIN MODE	COMPARATOR MODE	SPECIAL MODE
7	**MODE9:** 00b	**MODE9:** 01b	**MODE9:** 10b	**MODE9[1]:** Switch (4/10)*AIO7/8/9 to AB7/8/9
6				**MODE9[0]:** Switch AIO7/8/9 to CT resistors to generate CT at AB1
5	**OPT9:** AIO9 IO Option: 00b: Input 01b: Hi-Z 10b: Open-drain output 11b: Hi-Z	**GAIN9:** AIO9 Amplifier gain setting: 000b: Gain amplifier bypass, direct mode 001b: 1x 010b: 2x 011b: 4x 100b: 8x 101b: 16x 110b: 32x 111b: 48x	**OPT9:** AIO9 Comparator Reference select: 00b: VTHREF 01b: AB1 10b: AB2 11b: AB3	**OPT9:** AIO789 comparator output to POS: 00b: not connected 01b: MUX AIO7 comparator output to POS 10b: MUX AIO8 comparator output to POS 11b: MUX AIO9 comparator output to POS
4				
3	**POL9:** AIO9 Polarity Setting: 00b: active-high 01b: active-low		**POL9:** AIO9 Comparator polarity setting: 0b: active-high 1b: active-low	**POL9:** AIO9 Comparator polarity setting: 0b: active-high 1b: active-low
2:1	**MUX9:** AIO9 Digital MUX: 000b: DATAIO9 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	**MUX9**: AIO9 Analog MUX Setting: 000b: AB9 001b: AB1 010b: AB2 011b: AB3 100b: AB4 101b: AB5 110b: AB6 111b: AB7	**MUX9:** AIO9 Digital MUX: 000b: DATAIO9 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	Reserved, write to 00b.
0				**BEMF9**: Switch MUXed raw comparator output to DB6.

7.14.11 SOC.SIGSET

Register 7-11 SOC.SIGSET (Signal Manager Configuration, 10h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:4	**RFU**	R	0b	Reserved, write to 000b
3	**HPROTHYS**	RW	0b	HPx Hysteresis: 1b: Comparator Hysteresis enabled 0b: Comparator Hysteresis disabled
2	**LPROTHYS**	RW	0b	LPx Hysteresis: 1b: Comparator Hysteresis enabled 0b: Comparator Hysteresis disabled
1	**LPDACAB3**	RW	0b	Connect LPDAC output to AB3: 1b: LPDAC output connected to AB3 0b: LPDAC output not connected to AB3
0	**HPDACAB2**	RW	0b	Connect HPDAC output to AB2: 1b: HPDAC output connected to AB2 0b: HPDAC output not connected to AB2

7.14.12 SOC.HPDACH

Register 7-12 SOC.HPDACH (HPDAC High Setting, 11h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:0	**HPDAC[9:2]**	RW	0	HPDAC MSB setting bits 9:2

7.14.13 SOC.HPDACL

Register 7-13 SOC.HPDACL (HPDAC Low Setting, 12h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:2	**RFU**	R	0	Reserved, write to 0
1:0	**HPDAC[1:0]**	RW	0	HPDAC MSB setting bits 1:0

7.14.14 SOC.LPDACH

Register 7-14 SOC.LPDACH (LPDAC High Setting, 13h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:0	**LPDAC[9:2]**	RW	0	LPDAC MSB setting bits 9:2

7.14.15 SOC.LPDACL

Register 7-15 SOC.LPDAC1 (LPDAC Low Setting, 14h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:2	**Reserved**	R	0b	Reserved, write to 0.
1:0	**LPDAC[1:0]**	RW	0b	LPDAC Setting bits 1:0

7.14.16 SOC.SHCFG1

Register 7-16 SOC.SHCFG1 (Sample and Hold Configuration, 15h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:5	**RFU**	R	000b	Reserved, write to 0
4	**EMUXEN**	RW	0b	EMUX Enable: 1b: enabled 0b: disabled
3	**ADCBUFEN**	RW	0b	ADCBUF Circuit Enable: 1b: enabled 0b: disabled
2	**DAO54SH**	RW	0b	DAO54 Sample and Hold buffer enable: 1b: enable S/H 0b: disable and bypass S/H
1	**DAO32SH**	RW	0b	DAO32 Sample and Hold buffer enable: 1b: enable S/H 0b: disable and bypass S/H
0	**DAO10SH**	RW	0b	DAO10 Sample and Hold buffer enable: 1b: enable S/H 0b: disable and bypass S/H

7.14.17 SOC.SHCFG2

Register 7-17 SOC.SHCFG2 (Sample and Hold Configuration 2, 16h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**COMP_SH**	RW	0b	Comparator Toggle: 0b: Sample POS value 1b: Hold POS value
6	**HLD2**	RW	0b	DAO54 Sample and Hold Output: 0b: Sample 1b: Hold
5	**HLD1**	RW	0b	DAO32 Sample and Hold Output: 0b: Sample 1b: Hold
4	**HLD0**	RW	0b	DAO10 Sample and Hold Output: 0b: Sample 1b: Hold
3:0	**MUXA**	RW	0b	ADC Mux Channel Selector when **SHCFG1.EMUX_E**N is 0b: 1111b: VREF / 2 1110b: AB12 1101b: AB11 1100b: AB10 1011b: AB9 1010b: AB8 1001b: AB7 1000b: AB6 0111b: AB5 0110b: AB4 0101b: AB3 0100b: AB2 0011b: AB1 0010b: DAO54 0001b: DAO32 0000b: DAO10

7.14.18 SOC.PROTINTM

Register 7-18 SOC.PROTINTM (Protection Interrupt Mask, 17h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**RFU**	R	0b	Reserved, write to 0.
6	**HP54INTEN**	RW	0b	HPROT54 Interrupt enable: 1b: enable 0b: disabled
5	**HP32INTEN**	RW	0b	HPROT32 Interrupt enable: 1b: enable 0b: disabled
4	**HP10INTEN**	RW	0b	HPROT10 Interrupt enable: 1b: enable 0b: disabled
3	**RFU**	R	0b	Reserved, write to 0.
2	**LP54INTEN**	RW	0b	LPROT54 Interrupt enable: 1b: enable 0b: disabled
1	**LP32INTEN**	RW	0b	LPROT32 Interrupt enable: 1b: enable 0b: disabled
0	**LP10INTEN**	RW	0b	LPROT10 Interrupt enable: 1b: enable 0b: disabled

7.14.19 SOC.PROTSTAT

Register 7-19 SOC.PROTSTAT (Protection Interrupt Status, 18h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**HP54STAT**	R	0b	HPROT54 Real-time status: 0b: Comparator output low 1b: Comparator output high
6	**HP54INT**	RW	0b	HPROT54 Interrupt: 0b: No interrupt 1b: Interrupt, write 1 to clear
5	**HP32INT**	RW	0b	HPROT32 Interrupt: 0b: No interrupt 1b: Interrupt, write 1 to clear
4	**HP10INT**	RW	0b	HPROT10 Interrupt: 0b: No interrupt 1b: Interrupt, write 1 to clear
3	**LP54STAT**	R	0b	LPROT54 Real-time status: 0b: Comparator output low 1b: Comparator output high
2	**LP54INT**	RW	0b	LPROT54 Interrupt: 0b: No interrupt 1b: Interrupt, write 1 to clear
1	**LP32INT**	RW	0b	LPROT32 Interrupt: 0b: No interrupt 1b: Interrupt, write 1 to clear
0	**LP10INT**	RW	0b	LPROT10 Interrupt: 0b: No interrupt 1b: Interrupt, write 1 to clear

7.14.20 SOC.DOUTSIG0

Register 7-20 SOC.DOUTSIG0 (Digital Output 0, 19h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:6	**VTHREF**	RW	00b	Threshold voltage for comparators in AIO<9:6>: 00b: 0.1V 01b: 0.2V 10b: 0.5V 11b: 1.25V
5	**DOUT5**	RW	0b	Data output to AIO5.
4	**DOUT4**	RW	0b	Data output to AIO4.
3	**DOUT3**	RW	0b	Data output to AIO3.
2	**DOUT2**	RW	0b	Data output to AIO2.
1	**DOUT1**	RW	0b	Data output to AIO1.
0	**DOUT0**	RW	0b	Data output to AIO0.

7.14.21 SOC.DOUTSIG1

Register 7-21 SOC.DOUTSIG1 (Digital Output 1,1Ah)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**DOUT13**	RW	0b	Data output to CLKOUT.
6:4	**RFU**	R	00b	Reserved, write to 0.
3	**DOUT9**	RW	0b	Data output to AIO9.
2	**DOUT8**	RW	0b	Data output to AIO8.
1	**DOUT7**	RW	0b	Data output to AIO7.
0	**DOUT6**	RW	0b	Data output to AIO6.

7.14.22 SOC.DINSIG0

Register 7-22 SOC.DINSIG0 (Digital Input 0, 1Bh)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:6	**RFU**	RW	00b	Reserved, write to 0.
5	**DIN5**	R	0b	Data input from AIO5.
4	**DIN4**	R	0b	Data input from AIO4.
3	**DIN3**	R	0b	Data input from AIO3.
2	**DIN2**	R	0b	Data input from AIO2.
1	**DIN1**	R	0b	Data input from AIO1.
0	**DIN0**	R	0b	Data input from AIO0.

7.14.23 SOC.DINSIG1

Register 7-23 SOC.DINSIG1 (Digital Input 1, 1Ch)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**DIN13**	R	0b	Data input from CLKOUT.
6:4	**RFU**	R	000b	Reserved, write to 0.
3	**DIN9**	R	0b	Data input from AIO9.
2	**DIN8**	R	0b	Data input from AIO8.
1	**DIN7**	R	0b	Data input from AIO7.
0	**DIN6**	R	0b	Data input from AIO6.

7.14.24 SOC.CFGIO1

Register 7-24 SOC.CFGIO1 (AIO10-AIO13 Configuration 1, 1Dh)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:5	**RFU**	R	000b	Reserved, write as 0.
4	**EN_AIO6_OCP**	RW	0b	Enable AIO6 comparator output to disable gate driver on OC event.
3	**VREFBP**	RW	0b	Switch VREF signal to AB5 so that it can be buffered out on AIO6.
2:0	**RFU**	R	000b	Reserved, write as 0.

7.14.25 SOC.CFGIO2

Register 7-25 SOC.CFGIO2 (AIO10-AIO13 Configuration 2, 1Eh)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**CLKOUT_OPT**	RW	0b	CLKOUT option: 0b: Open drain output, if **MISC.CLKOUTEN** = 0b. 1b: Input
6	**CLKOUT_POL**	RW	0b	CLKOUT polarity: 0b: Active low 1b: Active high
5:0	**RFU**	R	0 0000b	Reserved, write as 0.

7.14.26 SOC.SIGINTM

Register 7-26 SOC.SIGINTM (AIO Interrupt Mask, 1Fh)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**AIO9REINTEN**	RW	0b	AIO9 digital input rising edge interrupt enable. 0b: disabled 1b: enabled
6	**AIO8REINTEN**	RW	0b	AIO8 digital input rising edge interrupt enable. 0b: disabled 1b: enabled
5	**AIO7REINTEN**	RW	0b	AIO7 digital input rising edge interrupt enable. 0b: disabled 1b: enabled
4	**AIO6REINTEN**	RW	0b	AIO6 digital input rising edge interrupt enable. 0b: disabled 1b: enabled
3	**AIO9FEINTEN**	RW	0b	AIO9 digital input falling edge interrupt enable. 0b: disabled 1b: enabled
2	**AIO8FEINTEN**	RW	0b	AIO8 digital input falling edge interrupt enable. 0b: disabled 1b: enabled
1	**AIO7FEINTEN**	RW	0b	AIO7 digital input falling edge interrupt enable. 0b: disabled 1b: enabled
0	**AIO6FEINTEN**	RW	0b	AIO6 digital input falling edge interrupt enable. 0b: disabled 1b: enabled

7.14.27 SOC.SIGINTF

Register 7-27 SOC.SIGINTF (AIO Interrupt Flag, 20h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**HP32STAT**	R	0b	HPROT32 Real-time status: 0b: Comparator output low 1b: Comparator output high
6	**LP32STAT**	R	0b	LPROT32 Real-time status: 0b: Comparator output low 1b: Comparator output high
5	**HP10STAT**	R	0b	HPROT10 Real-time status: 0b: Comparator output low 1b: Comparator output high
4	**LP10STAT**	R	0b	LPROT10 Real-time status: 0b: Comparator output low 1b: Comparator output high
3	**AIO9INT**	RW	0b	AIO9 Interrupt: 0b: No Interrupt 1b: Interrupt, nIRQ2 asserted. Write 1b to clear.
2	**AIO8INT**	RW	0b	AIO8 Interrupt: 0b: No Interrupt 1b: Interrupt, nIRQ2 asserted. Write 1b to clear.
1	**AIO7INT**	RW	0b	AIO7 Interrupt: 0b: No Interrupt 1b: Interrupt, nIRQ2 asserted. Write 1b to clear.
0	**AIO6INT**	RW	0b	AIO6 Interrupt: 0b: No Interrupt 1b: Interrupt, nIRQ2 asserted. Write 1b to clear.

7.14.28 SOC.BLANKING

Register 7-28 SOC.BLANKING (Comparator Blanking Configuration, 21h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:4	**BLANKTIME**	RW	0000b	Blanking time for BEMF Comparator: 1111b: 6000ns 1110b: 5500ns 1101b: 5000ns 1100b: 4500ns 1011b: 4000ns 1010b: 3500ns 1001b: 3000ns 1000b: 2500ns 0111b: 2000ns 0110b: 1500ns 0101b: 1250ns 0100b: 1000ns 0011b: 750ns 0010b: 500ns 0001b: 250ns 0000b: 100ns
3:2	**RFU**	R	00b	Reserved, write as 0.
1:0	**BLANKMODE**	R/W	00b	BEMF Comparator Blanking Mode: 11b: Leading and trailing edge blanking 10b: Trailing edge blanking 01b: Leading edge blanking 00b: Disabled

7.14.30 SOC.SPECCFG0

Register 7-29 SOC.SPECCFG0 (AIO7 Comparator Hysteresis Configuration, 22h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**HYSMODE**	RW	0x0	AIO7 Special Mode Comparator Hysteresis Mode: 1b: Hysteresis = 0/24/48/96 mV 0b: Hysteresis = 0/6/12/24 mV
6:4	**RFU**	R	0x0	Reserved
3:0	**AIO7HYS**	R/W	0x0	AIO7 Special Mode Comparator Rising/Falling Hysteresis for **SOC.SPECCFG0.HYSMODE** = 0: 1111b: Rising = 24mV, Falling = 24mV 1110b: Rising = 24mV, Falling = 12mV 1101b: Rising = 24mV, Falling = 6mV 1100b: Rising = 24mV, Falling = 0mV 1011b: Rising = 12mV, Falling = 24mV 1010b: Rising = 12mV, Falling = 12mV 1001b: Rising = 12mV, Falling = 6mV 1000b: Rising = 12mV, Falling = 0mV 0111b: Rising = 6mV, Falling = 24mV 0110b: Rising = 6mV, Falling = 12mV 0101b: Rising = 6mV, Falling = 6mV 0100b: Rising = 6mV, Falling = 0mV 0011b: Rising = 0mV, Falling = 24mV 0010b: Rising = 0mV, Falling = 12mV 0001b: Rising = 0mV, Falling = 6mV 0000b: Rising = 0mV, Falling = 0mV AIO7 Special Mode Comparator Rising/Falling Hysteresis for **SOC.SPECCFG0.HYSMODE** = 1: 1111b: Rising = 96mV, Falling = 96mV 1110b: Rising = 96mV, Falling = 48mV 1101b: Rising = 96mV, Falling = 24mV 1100b: Rising = 96mV, Falling = 0mV 1011b: Rising = 48mV, Falling = 96mV 1010b: Rising = 48mV, Falling = 48mV 1001b: Rising = 48mV, Falling = 24mV 1000b: Rising = 48mV, Falling = 0mV 0111b: Rising = 24mV, Falling = 96mV 0110b: Rising = 24mV, Falling = 48mV 0101b: Rising = 24mV, Falling = 24mV 0100b: Rising = 24mV, Falling = 0mV 0011b: Rising = 0mV, Falling = 96mV 0010b: Rising = 0mV, Falling = 48mV 0001b: Rising = 0mV, Falling = 24mV 0000b: Rising = 0mV, Falling = 0mV

7.14.31 SOC.SPECCFG1

Register 7-30 SOC.SPECCFG1 (AIO8/9 Comparator Hysteresis Configuration, 23h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:4	**AIO8HYS**	R/W	0x0	AIO8 Special Mode Comparator Rising/Falling Hysteresis for **SOC.SPECCFG0.HYSMODE** = 0: 1111b: Rising = 24mV, Falling = 24mV 1110b: Rising = 24mV, Falling = 12mV 1101b: Rising = 24mV, Falling = 6mV 1100b: Rising = 24mV, Falling = 0mV 1011b: Rising = 12mV, Falling = 24mV 1010b: Rising = 12mV, Falling = 12mV 1001b: Rising = 12mV, Falling = 6mV 1000b: Rising = 12mV, Falling = 0mV 0111b: Rising = 6mV, Falling = 24mV 0110b: Rising = 6mV, Falling = 12mV 0101b: Rising = 6mV, Falling = 6mV 0100b: Rising = 6mV, Falling = 0mV 0011b: Rising = 0mV, Falling = 24mV 0010b: Rising = 0mV, Falling = 12mV 0001b: Rising = 0mV, Falling = 6mV 0000b: Rising = 0mV, Falling = 0mV AIO8 Special Mode Comparator Rising/Falling Hysteresis for **SOC.SPECCFG0.HYSMODE** = 1: 1111b: Rising = 96mV, Falling = 96mV 1110b: Rising = 96mV, Falling = 48mV 1101b: Rising = 96mV, Falling = 24mV 1100b: Rising = 96mV, Falling = 0mV 1011b: Rising = 48mV, Falling = 96mV 1010b: Rising = 48mV, Falling = 48mV 1001b: Rising = 48mV, Falling = 24mV 1000b: Rising = 48mV, Falling = 0mV 0111b: Rising = 24mV, Falling = 96mV 0110b: Rising = 24mV, Falling = 48mV 0101b: Rising = 24mV, Falling = 24mV 0100b: Rising = 24mV, Falling = 0mV 0011b: Rising = 0mV, Falling = 96mV 0010b: Rising = 0mV, Falling = 48mV 0001b: Rising = 0mV, Falling = 24mV 0000b: Rising = 0mV, Falling = 0mV
3:0	**AIO9HYS**	R/W	0x0	AIO9 Special Mode Comparator Rising/Falling Hysteresis for **SOC.SPECCFG0.HYSMODE** = 0: 1111b: Rising = 24mV, Falling = 24mV 1110b: Rising = 24mV, Falling = 12mV 1101b: Rising = 24mV, Falling = 6mV 1100b: Rising = 24mV, Falling = 0mV 1011b: Rising = 12mV, Falling = 24mV 1010b: Rising = 12mV, Falling = 12mV 1001b: Rising = 12mV, Falling = 6mV 1000b: Rising = 12mV, Falling = 0mV 0111b: Rising = 6mV, Falling = 24mV 0110b: Rising = 6mV, Falling = 12mV 0101b: Rising = 6mV, Falling = 6mV 0100b: Rising = 6mV, Falling = 0mV 0011b: Rising = 0mV, Falling = 24mV 0010b: Rising = 0mV, Falling = 12mV 0001b: Rising = 0mV, Falling = 6mV 0000b: Rising = 0mV, Falling = 0mV

				AIO8 Special Mode Comparator Rising/Falling Hysteresis for **SOC.SPECCFG0.HYSMODE** = 1: 1111b: Rising = 96mV, Falling = 96mV 1110b: Rising = 96mV, Falling = 48mV 1101b: Rising = 96mV, Falling = 24mV 1100b: Rising = 96mV, Falling = 0mV 1011b: Rising = 48mV, Falling = 96mV 1010b: Rising = 48mV, Falling = 48mV 1001b: Rising = 48mV, Falling = 24mV 1000b: Rising = 48mV, Falling = 0mV 0111b: Rising = 24mV, Falling = 96mV 0110b: Rising = 24mV, Falling = 48mV 0101b: Rising = 24mV, Falling = 24mV 0100b: Rising = 24mV, Falling = 0mV 0011b: Rising = 0mV, Falling = 96mV 0010b: Rising = 0mV, Falling = 48mV 0001b: Rising = 0mV, Falling = 24mV 0000b: Rising = 0mV, Falling = 0mV

7.14.32 SOC.SPECCFG2

Register 7-31 SOC.SPECCFG2 (AIO7/8 Comparator MUX Input Configuration, 24h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**RFU**	R	0b	Reserved, write to 0.
6:4	**SMUXAIO7**	RW	000b	Special Mode Comparator Input MUX Selection for AIO7: 000b: VTHREF 001b: AB1 (virtual center-tap) 010b: AB2 011b: AB3 100b: AIO8 (phase to phase compare) 101b: AIO9 (phase to phase compare) 110b: RFU 111b: RFU
3	**RFU**	R	0b	Reserved, write to 0.
2:0	**SMUXAIO8**	RW	000b	Special Mode Comparator Input MUX Selection for AIO8: 000b: VTHREF 001b: AB1 (virtual center-tap) 010b: AB2 011b: AB3 100b: AIO7 (phase to phase compare) 101b: AIO9 (phase to phase compare) 110b: RFU 111b: RFU

7.14.33 SOC.SPECCFG3

Register 7-32 SOC.SPECCFG3 (AIO9 Comparator MUX Input Configuration, 25h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**RFU**	R	0b	Reserved, write to 0.
6:4	**SMUXAIO9**	RW	000b	Special Mode Comparator Input MUX Selection for AIO7: 000b: VTHREF 001b: AB1 (virtual center-tap) 010b: AB2 011b: AB3 100b: AIO7 (phase to phase compare) 101b: AIO8 (phase to phase compare) 110b: RFU 111b: RFU
3:0	**RFU**	R	000b	Reserved, write to 0.

8 APPLICATION SPECIFIC POWER DRIVER

8.1 Overview

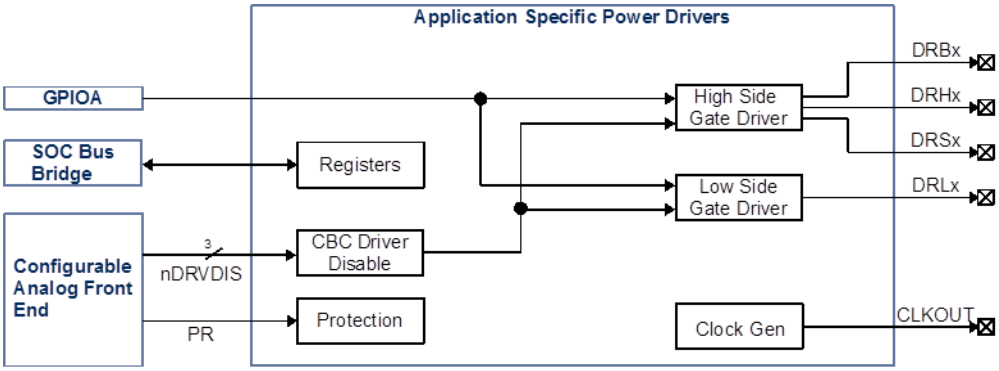
The Application Specific Power Drivers (ASPD) module handles power driving for power and motor control applications. The ASPD contains three low-side gate drivers (DRLx), three high-side gate drivers (DRHx). Each gate driver can drive an external MOSFET or IGBT switch in response to high-speed control signals from the microcontroller ports, and a pair of high-side and low-side gate drivers can form a half-bridge driver.

8.2 Features

- 3 low-side and 3 high-side gate drivers
- 2A gate driving capability
- Configurable delays and fast fault protection
- Cycle-by-cycle control (CBCCTL)

8.3 System Block Diagram

Figure 8-1 ASPD System Block Diagram



8.4 Functional Description

8.4.1 Enabling the ASPD

To enable the ASPD, set **SOC.ENDRV.ENDRV** to 1b.

8.4.2 Low-Side Gate Drivers

The ASPD contains 3 low-side gate drivers. The DRL<2:0> outputs of the ASPD are used to drive the gate of an external low-side power MOSFET up to 20V.

There are 4 programmable levels of driver propagation delay. The low-side gate drivers may sink or source up to 2A.

8.4.3 1.2.5. High-Side Gate Drivers

The ASPD contains 3 level-shifted high-side gate drivers. The gate driver is formed by the DRH<5:3>, DRB<5:3> and DRS<5:3> signals.

The incoming PWM signal is first level-shifted to the high-side rail (DRS<5:3>) which may operate up to 120V (200V absolute maximum). The DRH<5:3> is the gate driver signal, which can be driven at 20V relative to each respective DRS<5:3>.

Like the low-side gate drivers, there are 3 levels of programmable driver propagation delay and the driver may sink or source up to 2A.

8.4.4 1.2.6. Driver Protection

During operation the ASPD may disable the gate drivers when events such as over-current occur.

The ASPD has a protection input signal (PR) that notifies the ASPD of a protection event. If the ASPD has unmasked the high-side PR protection (**CFGDRV1.nHSPRM** = 1b) then the high-side gate drivers will be disabled.If the ASPD has unmasked the low-side PR protection (**CFGDRV1.nLSPRM** = 1b), then the low-side gate drivers will be disabled.

Once the gate drivers have been disabled, the MCU must reset the ASPD by setting **ENDRV.ENDRV** to 0b, then back to 1b in order to re-enable the ASPD.

8.4.5 1.2.7. PWM Input Signal Swap

The ASPD may be configured to swap the high-side and low-side PWM input signals for each of the half-bridge gate drivers.

To swap the DRH3/DRL0, set the **CFGDRV2.PWMSWAP30** to 1b. To swap DRH4/DRL1, set the **CFGDRV2.PWMSWAP41** to 1b. To swap DRH5/DRL2, set the **CFGDRV2.PWMSWAP52** to 1b.

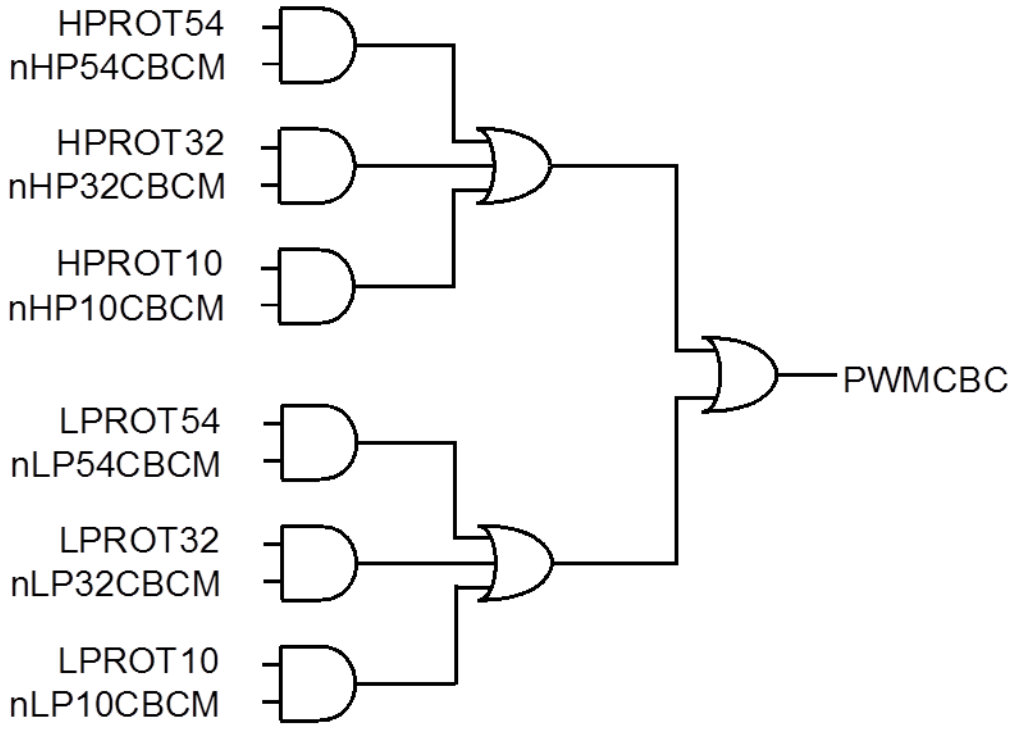
8.4.6 1.2.8. Cycle by Cycle Current Limit

To provide hardware assist for current limit, the ASPD may be configured to temporarily disable the gate drivers, when the current is over a configured threshold.

During these events, the ASPD may turn off all the high-side, low-side or high-side and low-side gate drivers based on the state of the Signal Manager HPCOMP/LPCOMP comparators. This can allow applications to have cycle by cycle current limit, without intervention of the MCU.

The diagram below shows how the protection comparators can be used to generate an event signal PWMCBC, which can be used to control this operation.

Figure 8-2 Cycle by Cycle Current Limit



The mask signal (**CFGDRV2.nDRVxyDISM**) is used to select which half-bridge to enable cycle-by-cycle current limit on, while **CFGDRV2.LPCBCHS** and **CFGDRV2.LPCBCLS** are used to select the high-side or low-side gate driver for the half-bridge to disable.

The real-time status of which half-bridge is in cycle-by-cycle current limit operation is available in **STATDRV.DRVxyDISSTAT**. The latched status is available in **STATDRV.DRVxyDIS**.

During operation, if the PWMCBC signal is high, then the output to the configured gate drivers is temporarily disabled, until the PWMCBC becomes available again. The following shows which drivers are disabled during this condition:

PWMCBC = high:

- If **CFGDRV2.LPCBCHS** = 1b and **CFGDRV2.nDRV52DISM** = 1b, disable DRH5
- If **CFGDRV2.LPCBCLS** = 1b and **CFGDRV2.nDRV52DISM** = 1b, disable DRL2

PWMCBC = high:

- If **CFGDRV2.LPCBCHS** = 1b and **CFGDRV2.nDRV41DISM** = 1b, disable DRH4
- If **CFGDRV2.LPCBCLS** = 1b and **CFGDRV2.nDRV41DISM** = 1b, disable DRL1

PWMCBC = high:

- If **CFGDRV2.LPCBCHS** = 1b and **CFGDRV2.nDRV30DISM** = 1b, disable DRH3
- If **CFGDRV2.LPCBCLS** = 1b and **CFGDRV2.nDRV30DISM** = 1b, disable DRL0

8.4.7 Break Before Make (BBM)

The ASPD supports a Break Before Make (BBM) configuration option for hardware protection against current shoot-through.

There are two types of BBM support:

- Single-driver BBM
- Half-bridge BBM

Single-driver BBM is always enabled and guarantees that the internal PMOS and NMOS FETs for a single gate driver are not on at the same time.

Half-bridge BBM can be enabled by setting **CFGDRV1.ENBBM** to 1b. When enabled, the half-bridge BBM function inserts 100ns of dead-time between in each of the half-bridge drivers (DRH3/DRL0, DRH4/DRL1, DRH5/DRL2).

8.5 Register Summary

Table 8-1 ASPD Register Summary

ADDRESS	REGISTER	DESCRIPTION	RESET
26h	**SOC.CFGDRV0**	Driver Configuration 0	00h
27h	**SOC.CFGDRV1**	Driver Configuration 1	00h
28h	**SOC.CFGDRV2**	Driver Configuration 2	00h
29h	**SOC.CFGDRV2**	Driver Configuration 3	00h
2Ah	**SOC.STATDRV**	Driver Status	00h
7Dh	**SOC.MODULE_ENABLE**	Driver Manager Enable	00h
7Eh	**SOC.WDTPASS**	SOC Watchdog Timer Password	00h

8.6 Register Detail

8.6.1 SOC.CFGDRV0

Register 8-1 SOC.CFGDRV0 (Driver Configuration 0, 26h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:6	**PROP3**	RW	00b	Propagation delay for DRH3: 00b: 0ns 01b: 50ns 10b: 100ns 11b: 200ns
5:4	**PROP2**	RW	00b	Propagation delay for DRL2: 00b: 0ns 01b: 50ns 10b: 100ns 11b: 200ns
3:2	**PROP1**	RW	00b	Propagation delay for DRL1: 00b: 0ns 01b: 50ns 10b: 100ns 11b: 200ns
1:0	**PROP0**	RW	00b	Propagation delay for DRL0: 00b: 0ns 01b: 50ns 10b: 100ns 11b: 200ns

8.6.2 SOC.CFGDRV1

Register 8-2 SOC.CFGDRV1 (Driver Configuration 1, 27h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:6	**PROP5**	RW	00b	Propagation delay for DRH5: 00b: 0ns 01b: 50ns 10b: 100ns 11b: 200ns
5:4	**PROP4**	RW	00b	Propagation delay for DRH4: 00b: 0ns 01b: 50ns 10b: 100ns 11b: 200ns
3	**HSPREN**	RW	0b	High side PR protection enable: 0b: PR1 disabled 1b: PR1 enabled
2	**LSPREN**	RW	0b	Low side PR protection enable: 0b: PR1 disabled 1b: PR1 enabled
1	**PEXTDIS**	RW	0b	PWM Pulse Extension Disable: 0b: Pulse Extension Enabled 1b: Pulse Extension Disabled
0	**ENBBM**	RW	0b	Enable Break-before-make. When enabled, inserts 100ns dead-time between the high and low-side PWM signal of each pair of half-bridges (DRH3/DRL0, DRH4/DRL1, DRH5/DRL2): 0b: disabled 1b: enabled

8.6.3 SOC.CFGDRV2

Register 8-3 SOC.CFGDRV2 (Driver Configuration 2, 28h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**PWMSWAP52**	RW	0b	When set, swap PWM input signal between DRH5 and DRL2: 0b: no swap 1b: swap
6	**PWMSWAP41**	RW	0b	When set, swap PWM input signal between DRH4 and DRL1: 0b: no swap 1b: swap
5	**PWMSWAP30**	RW	0b	When set, swap PWM input signal between DRH3 and DRL0: 0b: no swap 1b: swap
4	**nDRV52DISM**	R/W	0b	Mask signal for DRH5/DRL2 high-side, low-side or both driver disable. Used for PWM pulse cycle-by-cycle current limit: 0b: not masked 1b: masked
3	**nDRV41DISM**	R/W	0b	Mask signal for DRH4/DRL1 high-side, low-side or both driver disable. Used for PWM pulse cycle-by-cycle current limit: 0b: not masked 1b: masked
2	**nDRV30DISM**	R/W	0b	Mask signal for DRH3/DRL0 high-side, low-side or both driver disable. Used for PWM pulse cycle-by-cycle current limit: 0b: not masked 1b: masked
1	**LPCBCLS**	R/W	0b	Control signal for low-side gate drivers disable. Used for PWM pulse cycle-by-cycle current limit: 0b: Do not disable 1b: Disable when commanded
0	**LPCBCHS**	R/W	0b	Control signal for high-side gate drivers disable. Used for PWM pulse cycle-by-cycle current limit: 0b: Do not disable 1b: Disable when commanded

8.6.4 SOC.CFGDRV3

Register 8-4 SOC.CFGDRV3 (Driver Configuration 3, 29h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**nHP54CBCM**	R/W	0b	Mask signal for HPROT54 for PWM pulse cycle-by-cycle current limit: 0b: masked 1b: not masked
6	**nLP54CBCM**	R/W	0b	Mask signal for LPROT54 for PWM pulse cycle-by-cycle current limit: 0b: masked 1b: not masked
5	**nHP32CBCM**	R/W	0b	Mask signal for HPROT32 for PWM pulse cycle-by-cycle current limit: 0b: masked 1b: not masked
4	**nLP54CBCM**	R/W	0b	Mask signal for LPROT32 for PWM pulse cycle-by-cycle current limit: 0b: masked 1b: not masked
3	**nHP10CBCM**	R/W	0b	Mask signal for HPROT10 for PWM pulse cycle-by-cycle current limit: 0b: masked 1b: not masked
2	**nLP10CBCM**	R/W	0b	Mask signal for LPROT10 for PWM pulse cycle-by-cycle current limit: 0b: masked 1b: not masked
1	**RFU**	R	0b	Reserved, write as 0.
0	**RFU**	R	0b	Reserved, write as 0.

8.6.6 SOC.STATDRV

Register 8-5 SOC.STATDRV (Driver Status, 2Ah)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**RFU**	R	0b	Reserved, write as 0.
6	**RFU**	R	0b	Reserved, write as 0.
5	**DRV52DISSTAT**	R	0b	Real-time status of DRV52DIS signal: 0b: Driver disable inactive 1b: Driver disable active
4	**DRV41DISSTAT**	R	0b	Real-time status of DRV41DIS signal: 0b: Driver disable inactive 1b: Driver disable active
3	**DRV30DISSTAT**	R	0b	Real-time status of DRV30DIS signal: 0b: Driver disable inactive 1b: Driver disable active
2	**DRV52DIS**	R	0b	Latched status of DRV54DIS signal. To clear, write this bit to a 1b: 0b: No driver disable event 1b: Driver disable event occurred
1	**DRV32DIS**	R	0b	Latched status of DRV32DIS signal. To clear, write this bit to a 1b: 0b: No driver disable event 1b: Driver disable event occurred
0	**DRV10DIS**	R	0b	Latched status of DRV10DIS signal. To clear, write this bit to a 1b: 0b: No driver disable event 1b: Driver disable event occurred

8.6.7 SOC.ENDRV

Register 8-6 SOC.ENDRV (Driver Manager Enable, 7Dh)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:1	**RFU**	R	000 0000b	Reserved, write as 0.
0	**ENDRV**	RW	0b	Driver Manager Enable: 0b: Disable 1b: Enable

8.6.8 SOC.WDTPASS

Register 8-7 SOC.WDTPASS (WDT Password, 7Eh)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:0	**WDTPASS**	RW	0000 0000b	To reset the SOC Watchdog Timer, write this field to ACh.

9 LEGAL INFORMATION

All information provided in this document is subject to legal disclaimers.

Active-Semi reserves the right to modify its products, circuitry or product specifications without notice. Active-Semi products are not intended, designed, warranted or authorized for use as critical components in life-support, life-critical or safety-critical devices, systems, or equipment, nor in applications where failure or malfunction of any Active-Semi product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Active-Semi accepts no liability for inclusion and/or use of its products in such equipment or applications. Active-Semi does not assume any liability arising out of the use of any product, circuit, or any information described in this document. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of Active-Semi or others. Active-Semi assumes no liability for any infringement of the intellectual property rights or other rights of third parties which would result from the use of information contained herein. Customers should evaluate each product to make sure that it is suitable for their applications. Customers are responsible for the design, testing, and operation of their applications and products using Active-Semi products. Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. All products are sold subject to Active-Semi's terms and conditions of sale supplied at the time of order acknowledgment. Exportation of any Active-Semi product may be subject to export control laws.

Active-Semi® and Power Application Controller® are registered trademarks of Active-Semi, Inc.

The Active-Semi logo, Solutions for Sustainability™, Micro Application Controller™, Multi-Mode Power Manager™, Configurable Analog Front End™, and Application Specific Power Drivers™ are trademarks of Active-Semi, Inc.

ARM® and Cortex® are registered trademarks of ARM Limited. All referenced brands and trademarks are the property of their respective owners.

For more information on this and other products, contact sales@active-semi.com or visit www.active-semi.com.