AS1506

256-Tap Digital Potentiometer with SPI Interface and High Endurance EEPROM

1 General Description

The AS1506 is a linear, 256-tap digital potentiometer specifically designed to replace discrete/mechanical potentiometers and is ideal for applications requiring a low-temperature-coefficient variable resistor, such as low-drift, programmable gain, and amplifier circuit configurations.

The device is controlled via a 3-wire SPI-compatible interface and features an internal EEPROM for storing wiper positions.

Several device variants are available differentiated by end-to-end resistance as shown in Table 1 (see also Ordering Information on page 16).

Table 1. Standard Products

Model	End-to-End Resistance (kΩ)
AS1506-10	10
AS1506-50	50
AS1506-100	100

The 3-wire SPI-compatible serial interface allows communication at data rates up to 5MHz.The internal EEPROM stores the last wiper position for initialization during power-up and a low-power standby mode.

The devices are available in an 8-pin TDFN 3x3mm package.

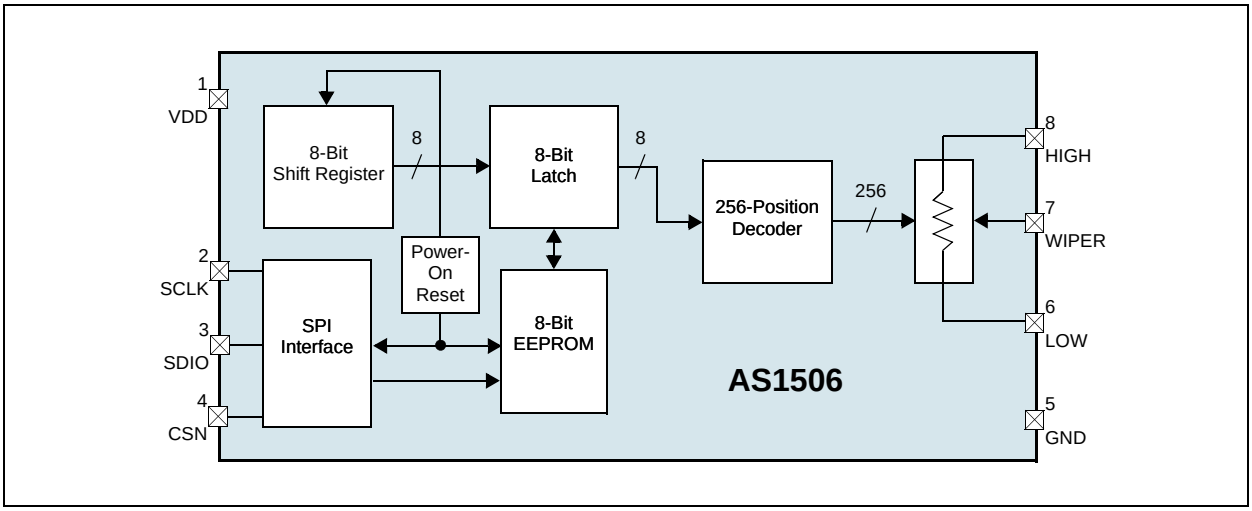
2 Key Features

- High Endurance: EEPROM up to 10M cycles
- High Reliability: EEPROM up to 150 years data retention @ 85°C
- Wiper Position Retained in EEPROM and loaded at Power-Up
- 256 Tap Positions
- ±0.5LSB DNL in Voltage Divider Mode
- ±0.5LSB INL in Voltage Divider Mode
- End-to-End Resistance: 10/50/100kΩ
- Low End-to-End Resistance Temperature Coefficient: 90ppm/ºC
- Low-Power Standby Mode: 100nA
- 5MHz SPI-Compatible Serial Interface
- Single-Supply Operation: +2.7V to +5.5V
- 8-pin TDFN 3x3mm Package

3 Applications

The device is ideal for mechanical potentiometer replacement, low-drift programmable gain amplifiers, audio volume control, LCD contrast control, and low-drift programmable filters.

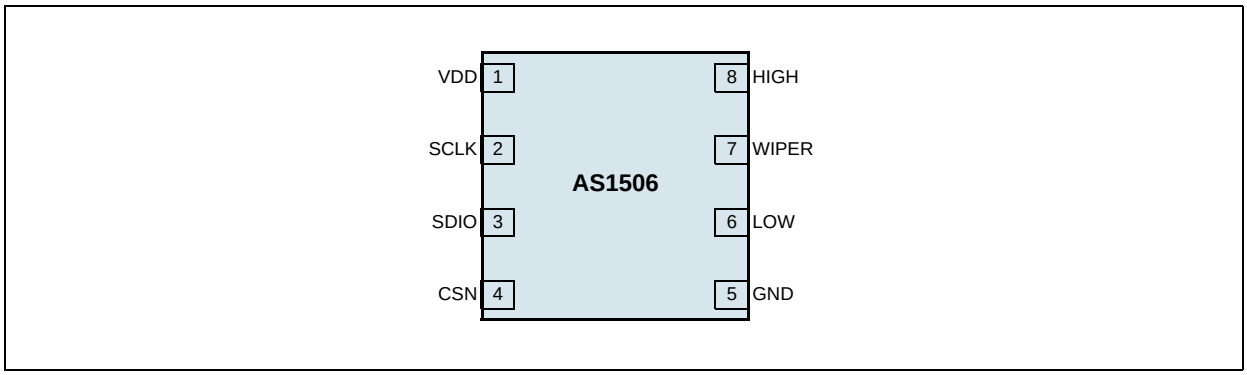
Figure 1. AS1506 - Block Diagram



4 Pinout

Pin Assignments

Figure 2. Pin Assignments (Top View)



Pin Descriptions

Table 2. Pin Descriptions

Pin Number	Pin Name	Description
1	VDD	**2.7V to 5.5V Supply Voltage.** Bypass with a 0.1µF capacitor to GND.
2	SCLK	**Serial Clock Input**
3	SDIO	**Serial Data Input/Output**
4	CSN	**Active-Low Chip Select**
5	GND	**Ground**
6	LOW	**Low Terminal.** The voltage at this pin can be greater than or less than the voltage at pin HIGH. Current can flow into or out of this pin.
7	WIPER	**Wiper Terminal**
8	HIGH	**High Terminal.** The voltage at this pin can be greater than or less than the voltage at pin LOW. Current can flow into or out of this pin.
N/A	Exposed Pad	The exposed pad is not internally connected. Leave floating.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 3 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute Maximum Ratings

Parameter		Min	Max	Units	Comments
V_{DD} to GND		-0.3	+7.0	V	
All Other Pins to GND		-0.3	V_{DD} + 0.3	V	
Maximum Continuous Current into Pins HIGH, WIPER, and LOW	AS1506-10	+0.55		mA	
	AS1506-50	+0.55			
	AS1506-100	+0.55			
Electrostatic Discharge		1		kV	*HBM MIL-Std. 883E 3015.7* methods
Latch-Up[1]		-100	100	mA	*JEDEC 78*
Thermal Resistance Θ_{JA}		48		ºC/W	on PCB
Operating Temperature Range		-40	+85	ºC	
Storage Temperature Range		-60	+150	ºC	
Junction Temperature			+150	ºC	
Package Body Temperature			+260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020D "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).

1. The maximum rating voltage must not be exceeded during Latch-up test of the device.

6 Electrical Characteristics

V_{DD} = +2.7 to +5.5V, HIGH = V_{DD}, LOW = GND, T_{AMB} = -40 to +85ºC. Typ values are at V_{DD} = +5.0V, T_{AMB} = +25ºC (unless otherwise specified).

Table 4. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Power Supply						
V_{DD}			2.70		5.5	V
I_{DD}	Standby Current	Digital Inputs = V_{DD} or GND, T_{AMB} = +25ºC		0.1	0.5	µA
I_{OP}	Operating Current (CMOS write)	Includes Non-Volatile Write to Memory [1]		110	200	µA
DC Performance (Voltage Divider Mode)						
N	Resolution		256			Taps
INL	Integral Linearity [2]	AS1506-10		±0.5	±1	LSB
		AS1506-50 & -100		±0.25	±0.5	
DNL	Differential Non-Linearity [2]	AS1506-10		±0.5	±1	LSB
		AS1506-50 & -100		±0.25	±0.5	
TC_R	End-to-End Resistance Temperature Coefficient	*T_{AMB} = 0 to +85ºC*		90		ppm/ºC
	Full Scale Error	AS1506-10		2.5	4	LSB
		AS1506-50		1.5	2.5	
		AS1506-100		1.5	2.5	
	Zero Scale Error	AS1506-10		1	2	LSB
		AS1506-50		0.1	0.7	
		AS1506-100		0.1	0.7	
DC Performance (Variable Resistor Mode)						
INL	Integral Linearity [3]	AS1506-10		±1	±2	LSB
		AS1506-50 & -100 @ 3V		±0.6	±1.5	
		AS1506-50 & -100 @ 5V		±0.5	±1	
DNL	Differential Non-Linearity	AS1506-10		±0.5	±1	LSB
		AS1506-50 & -100		±0.5	±1	
DC Performance (Resistor Characteristics)						
R_W	Wiper Resistance [4]	V_{DD} = 3V		200		Ω
		V_{DD} = 5V		120		
C_W	Wiper Capacitance			15		pF
R_{EE}	End-to-End Resistance	AS1506-10	7.5	10	12.5	kΩ
		AS1506-50	37.5	50	62.5	
		AS1506-100	75	100	125	
Inputs and Outputs						
	WIPER Voltage Range		GND-0.3		V_{DD}+0.3	V
	HIGH Voltage Range					
	LOW Voltage Range					
V_{IH}	Digital Input High Voltage [5]	V_{DD} = 3V	2.1			V
		V_{DD} = 5V	2.4			
V_{IL}	Digital Input Low Voltage [5]	V_{DD} = 3V			0.6	V
		V_{DD} = 5V			0.8	
I_{LEAK}	Digital Input Leakage Current			200	500	nA
C_{IN}	Digital Input Capacitance			5		pF
I_{CONT}	Continuous DAC current				560	µA

Table 4. Electrical Characteristics (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Dynamic Characteristics						
	Wiper -3dB Bandwidth [6]	AS1506-10		1200		kHz
		AS1506-50		220		
		AS1506-100		120		
tS	Wiper Settling Time [7]	AS1506-10		1100		ns
		AS1506-50		1600		
		AS1506-100		2200		
Non-Volatile Memory Reliability						
	Data Retention [8]	TAMB = +85ºC		150		Years
	Endurance [8]	TAMB = +25ºC		10M		Write Cycles
		TAMB = +85ºC		1M		
tBUSY	Write Non-Volatile Register Busy Time				20	ms

1. The programming current operates only during power-up and non-volatile memory writes.
2. DNL and INL are measured with the potentiometer configured as a voltage-divider with HIGH = VDD and LOW = GND. The wiper terminal is unloaded and measured with a high-input-impedance voltmeter.
3. DNL and INL are measured with the potentiometer configured as a variable resistor. HIGH is unconnected and LOW = GND. For the 5V condition, the wiper terminal is driven with a source current of 400µA @ 10kΩ, 80µA @ 50kΩ, 40µA @ 100kΩ. In 3V conditions, the wiper terminal is driven with a source current of 200µA @ 10kΩ, 40µA @ 50kΩ, 20µA @ 100kΩ.
4. The wiper resistance is measured using the source currents given in Note 3. The number is the worst case resistance over TAP positions.
5. The device draws higher supply current when the digital inputs are driven with voltages between (VDD - 0.5V) and (GND + 0.5V).
6. Wiper at midscale with a 10pF load (DC measurement) VDD = 5V, LOW = GND. An AC source (5V peak to peak sinus signal) is applied to HIGH and the WIPER output is measured. A 3dB bandwidth occurs when the AC WIPER/HIGH value is 3dB lower than the DC WIPER/HIGH value.
7. Wiper-settling time is the worst-case 0 to 50% rise-time measured between successive wiper positions. HIGH = VDD, LOW = GND; WIPER is unloaded and measured with a 10pF load.
8. This parameter is not tested but ensured by characterization.

Timing Characteristics

VDD = +2.7 to +5.5V, HIGH = VDD, LOW = GND, TAMB = -40 to +85ºC. Typ values are at VDD = +5.0V, TAMB = +25ºC (unless otherwise specified). See Figure 20 on page 9. Digital timing data is guaranteed by design and characterization, and is not production tested.

Table 5. Timing Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
fSCLK	SCLK Frequency				5	MHz
tCP	SCLK Clock Period		200			ns
tCH	SCLK Pulse-Width High		40			ns
tCL80	SCLK Pulse-Width Low		40			ns
tCSS	CSN-Fall to SCLK Rise Setup		40			ns
tCSH	SCLK-Rise to CSN-Rise Hold		40			ns
tDS	SDIO to SCLK Setup		10			ns
tDH	SDIO Hold after SCLK		0			ns
tCS0	SCLK-Rise to CSN-Fall Delay		40			ns
tCS1	CSN-Rise to SCLK-Rise Hold		40			ns
tCSW	CSN Pulse-Width High		200			ns
tBUSY	Write Non-Volatile Register Busy Time				20	ms

7 Typical Operating Characteristics

V_{DD} = 5V (unless otherwise specified).

Figure 3. DNL vs. TAP Position 10kΩ, Divider Mode

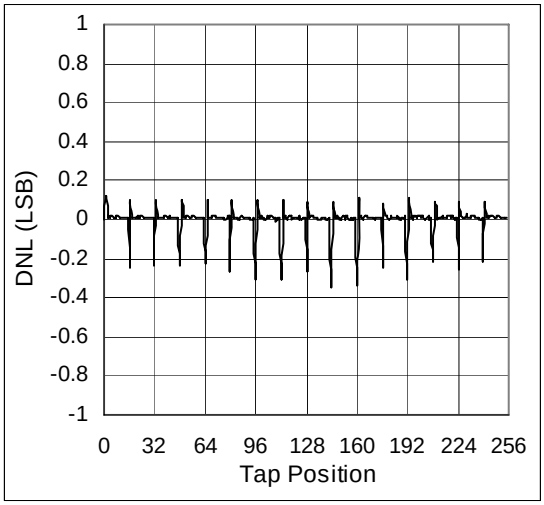


Figure 4. INL vs. TAP Position 10kΩ, Divider Mode

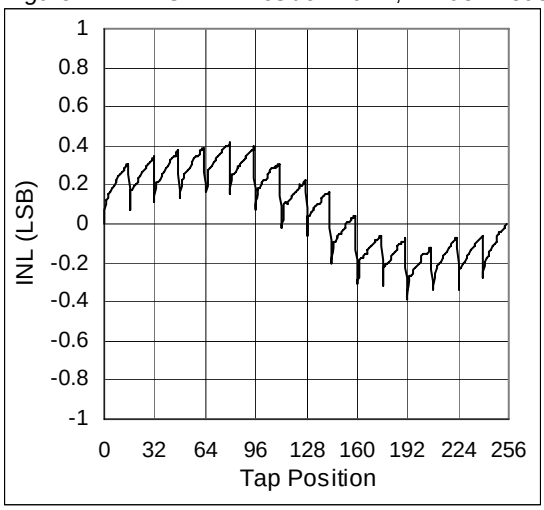


Figure 5. DNL vs. TAP Position 50kΩ, Divider Mode

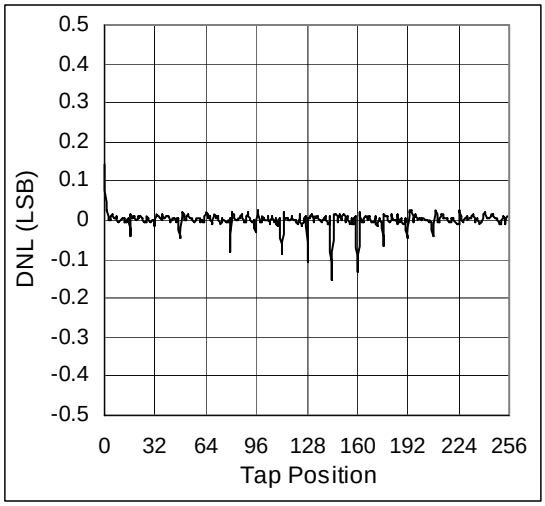


Figure 6. INL vs. TAP Position 50kΩ, Divider Mode

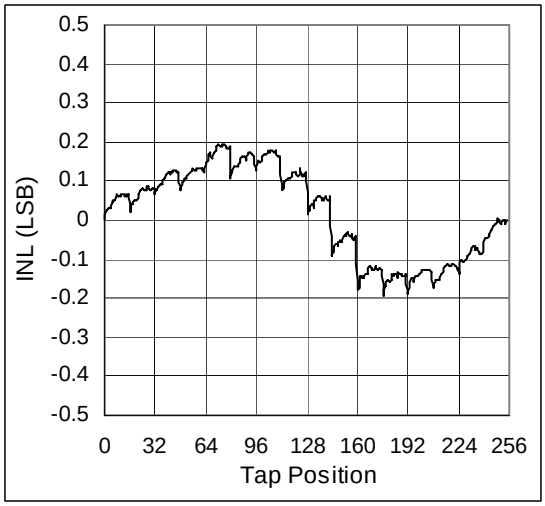


Figure 7. DNL vs. TAP Position 100kΩ, Divider Mode

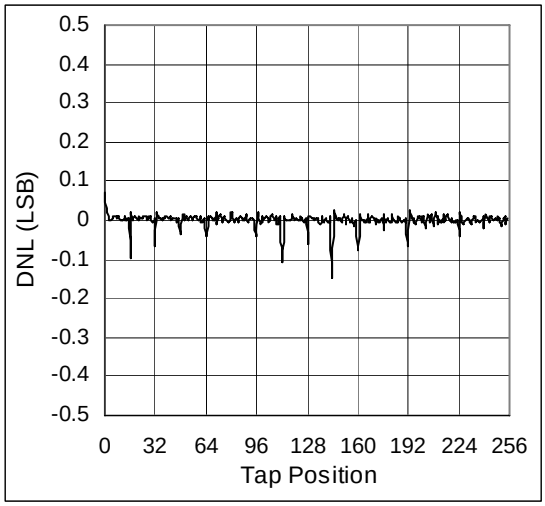


Figure 8. INL vs. TAP Position 100kΩ, Divider Mode

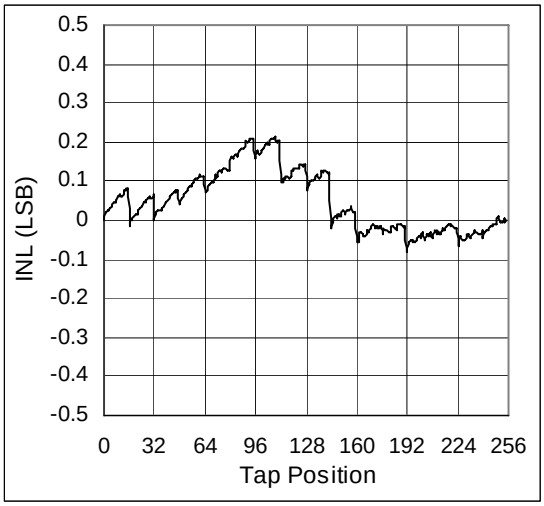


Figure 9. DNL vs. TAP Position 10kΩ, Varistor Mode

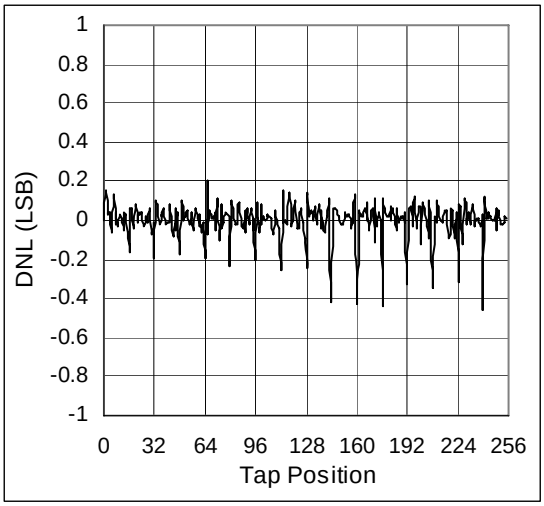


Figure 10. INL vs. TAP Position 10kΩ, Varistor Mode

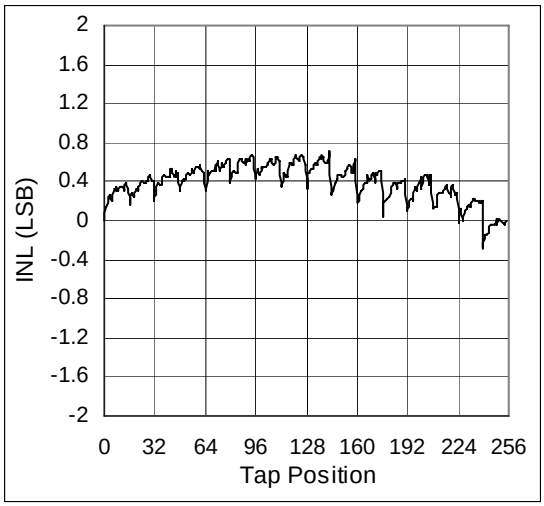


Figure 11. DNL vs. TAP Position 50kΩ, Varistor Mode

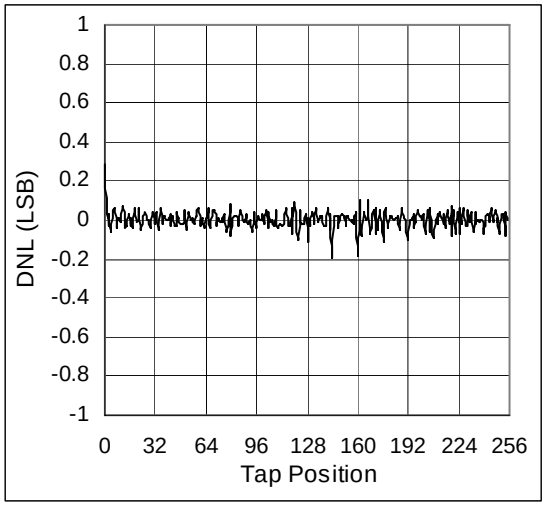


Figure 12. INL vs. TAP Position 50kΩ, Varistor Mode

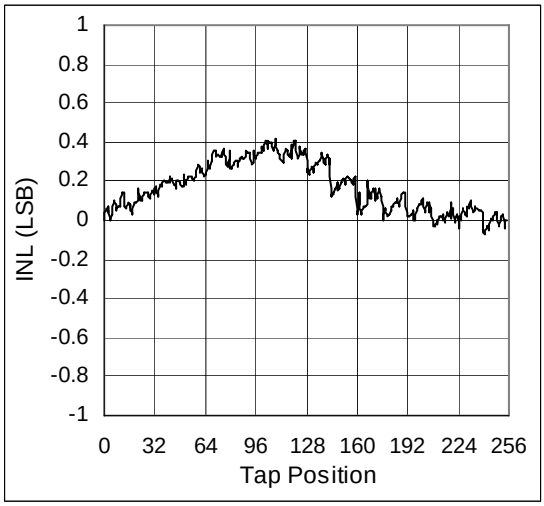


Figure 13. DNL vs. TAP Position 100kΩ, Varistor Mode
Mode

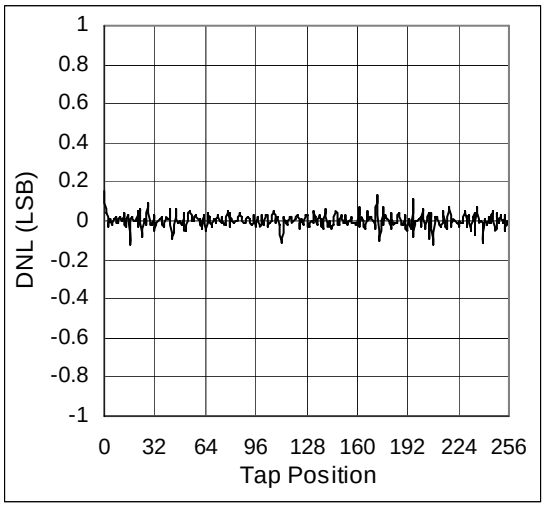


Figure 14. INL vs. TAP Position 100kΩ, Varistor

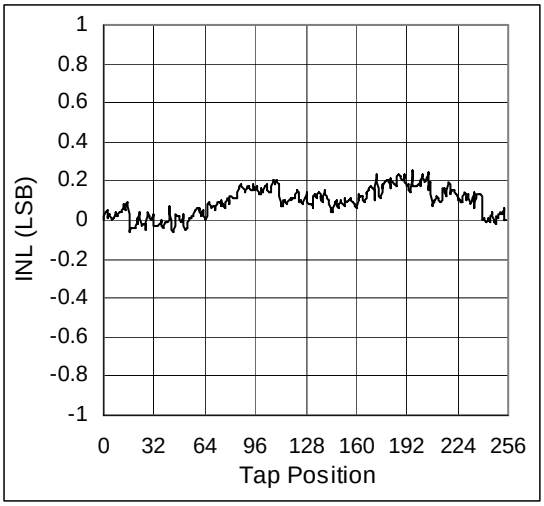


Figure 15. Wiper Resistance vs. TAP; 5V

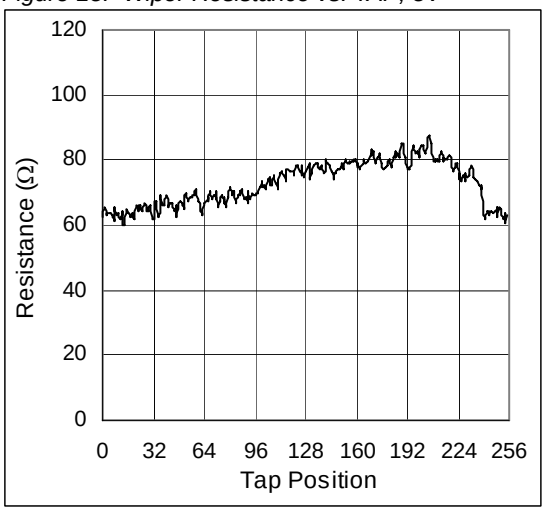


Figure 16. Wiper Resistance vs. TAP; 3V

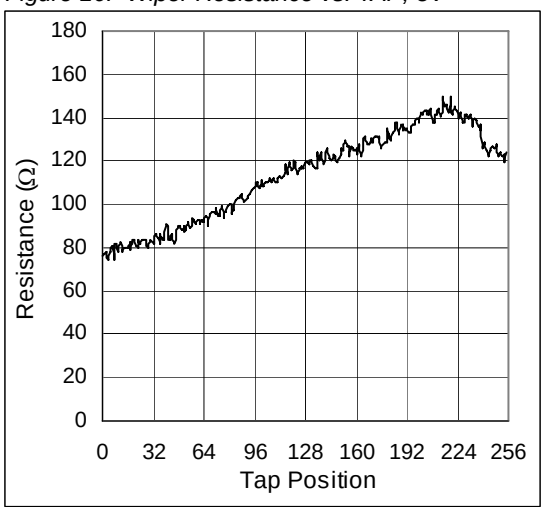


Figure 17. DAC Resistor vs. Temperature

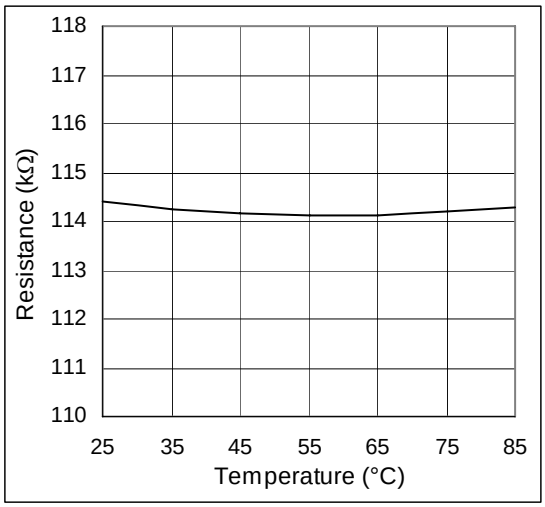


Figure 18. Gain vs. Bandwidth

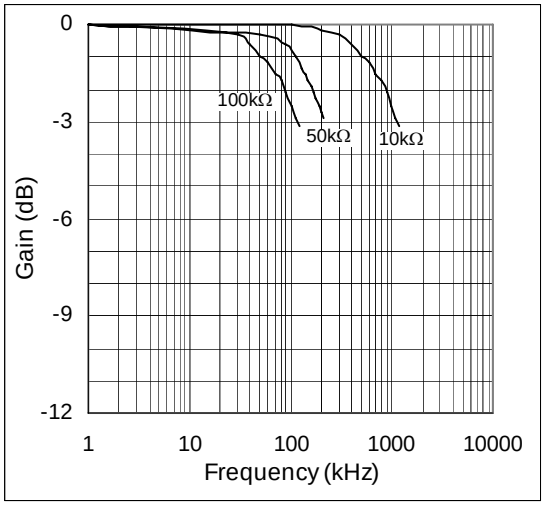
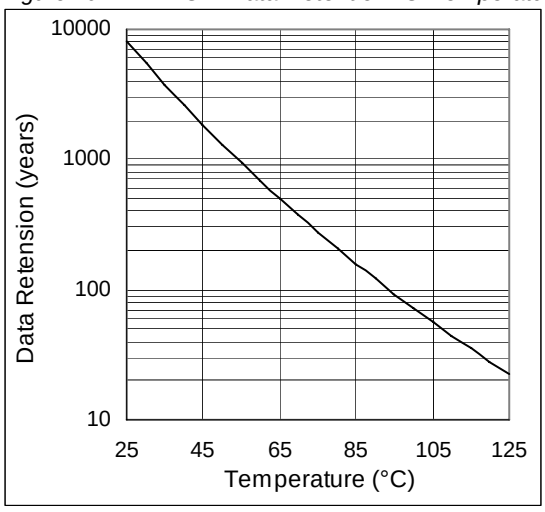


Figure 19. EEPROM Data Retention vs. Temperature



8 Detailed Description

The AS1506 contains a resistor array with 255 resistive elements (tap points), and has a total end-to-end resistance of 10, 50, or 100kΩ (see Ordering Information on page 16).

The device provides high, low, and wiper terminals for a standard voltage-divider configuration. Pins HIGH, LOW, and WIPER can be connected in any configuration as long as their voltages fall between GND and V_{DD}.

A 3-wire, SPI-compatible serial interface controls movement of the wiper among the 256 tap points. The EEPROM stores the wiper position and recalls the stored wiper position upon power-up. The EEPROM typically holds wiper data for 150 years and up to 10M wiper store cycles.

Analog Circuit

The 256 tap points are accessible to the wiper along the resistor string between pins HIGH and LOW (similar to the end terminals of a mechanical potentiometer). The wiper tap point is selected by programming 8 data bits and a control byte via the 3-wire serial interface (see Programming the Device on page 10).

Note: Integrated power-on reset circuitry loads the wiper position from the EEPROM at power-up.

Digital Interface

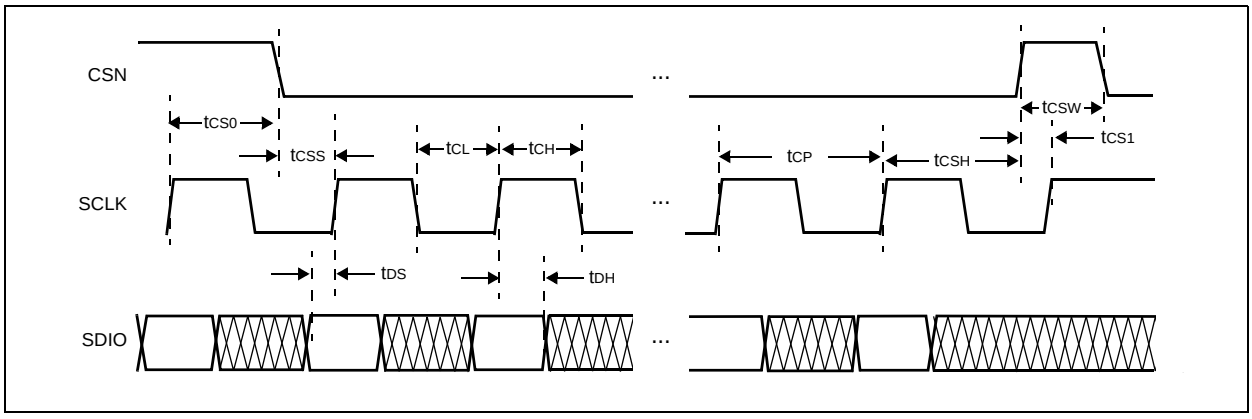
The AS1506 uses an SPI-compatible 3-wire interface for command settings of the device consisting of two input signals (chip-select - CSN, and data clock - SCLK) and one bi-directional data pin (SDIO). Driving CSN low enables serial interface and the command/data are passed into the device synchronously by each SCLK rising edge.

There are 16-bit commands for write data into the wiper register or the non-volatile memory, and 8-bit commands for transferring data between wiper register and non-volatile memory and to read the data stored in the wiper register or non-volatile memory. The 8-bit commands can be implemented in 16-bit command structure alternatively. In this case the first 8 bits shifted through the SPI interface are not significant. The data byte passed at writing commands represents the position of the wiper.

After loading the 8- or 16-bit command while CSN is low, the loaded command is executed at the next rising edge of CSN, simultaneously the serial interface is disabled. The CSN signal must be low during the whole serial input stream through the SPI, otherwise data on the SPI interface are corrupted.

Note: If the data-in stream does not exactly contain 8 or 16 digits, no command is executed at the rising edge of CSN.

Figure 20. Serial Data Timing



Standby Mode

Low-power standby mode is enable at CSN high. After an read access standby mode is entered 2 cycles of SCLK after issuing the last bit of the data wiper or non-volatile register. If the digital inputs are stable V_{DD} or GND there is only leakage power dissipation of the device.

This power dissipation is defined with 0.1uA (typ) at 25ºC.

EEPROM (Non-Volatile Register)

There is an internal EEPROM register implemented to retain the wiper position after power down. During an ongoing write cycle of the non-volatile register (t_{BUSY} time) the system must not be powered down.

Data retention defines the ability of an EEPROM to retain data over time. The qualification has been done according to JEDEC Retention Lifetime Specification (A117). The EEPROM is cycled to the specified endurance limit before the data retention test is done. Based on activation energy of 0.6eV the data retention time derates over temperature as shown in Figure 19 on page 8.
For the non-volatile register 1M endurance cycles and a data retention of 150 years are typical at 85 ºC. The non-volatile register is factory trimmed to mid-scale.

Power-Up

The AS1506 contains an integrated power-up circuit. At power up, the data are transferred from the non-volatile memory to the wiper register. The wiper register moves to the stored position. This data transfer takes 5µs after the supply has reached the POR trigger level.

Programming the Device

Write commands (see Table 6) require 16 clock cycles (see Figure 22 on page 12) to clock in the command and data.

Copy and Read commands (see Table 6) can use 8 clock cycles to clock in the command (see Figure 21 on page 11) or 16 clock cycles. At 16 clock cycle commands the 8 data bits (D7:D0) are insignificant.

Table 6. Command/Data Word Format

Command	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	C7	C6	C5	C4	C3	C2	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
Write Wiper Register	0	0	0	0	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0
Write to Non-Volatile Register	0	0	0	1	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0
Copy Wiper Register to Non-Volatile Register	0	0	1	0	0	0	0	0	-	-	-	-	-	-	-	-
Copy Non-Volatile Register to Wiper Register	0	0	1	1	0	0	0	0	-	-	-	-	-	-	-	-
Read Non-Volatile Register	0	0	1	0	1	0	0	0	-	-	-	-	-	-	-	-
Read Wiper Register	0	1	1	0	1	0	0	0	-	-	-	-	-	-	-	-

Commands

Write Wiper Register

This is a 16-bit command (see Figure 22 on page 12). The first byte represents the command word starting with the MSB bit of the command, the second byte represents the data written to the wiper register (starting with the MSB). Data 0000 0000 the wiper moves the closest position to LOW, with data 1111 1111 the wiper moves to the closest position to HIGH.

Note: At power-up the wiper position stored in the non-volatile memory are automatically loaded into the wiper register, the wiper moves to the related position.

Write to Non-Volatile Register

This is a 16-bit command (see Figure 22 on page 12). The first byte represents the command word starting with the MSB bit of the command, the second byte represents the data written to the non-volatile memory. The wiper position is not changed by this command, since the wiper register is not affected.

There is a write non-volatile register time defined in the timing specification, which is required for storing the data in the non-volatile register. During this time the device must not be powered down, otherwise the data stored in the non-volatile register is corrupted.

Copy Wiper Register to Non-Volatile Register

This command can be implemented as an 8- or 16-bit command. The data stored in the wiper register are transferred to the non-volatile memory, to keep the data during power-down. There is no automatic trigger of this command during power-down of the device. This command must be triggered before powering down the device.

There is a write non-volatile register time defined in the timing specification, which is required for storing the data in the non-volatile register. During this time the device must not be powered down, otherwise the data stored in the non-volatile register is corrupted.

Copy Non-Volatile Register to Wiper Register

This command can be implemented as an 8- or 16-bit command. The data stored in the non-volatile register are transferred to the wiper register, the wiper register moves to the stored position. This command is automatically executed during power up of the system.

Read Non-Volatile Register

The AS1506 features the capability to read the data from the non-volatile register via the SPI interface (see Figure 23 on page 12). This command can be implemented as an 8- or 16-bit command. The SDIO pin is a bi-directional pin. During the CSN low phase of the sequence the SDIO pin is used as input pin to set the command byte. After CSN rising edge the pin SDIO is set as output pin, the data stored in the non-volatile register are read serially, MSB first.

The data propagation starts at the second rising edge of SCLK after the rising edge of CSN. CSN must be high during the read operation. With the next falling edge of CSN the SDIO pin is set to an input pin again.

Read Wiper Register

The AS1506 features the capability to read the data from the wiper register via the SPI interface (see Figure 23 on page 12). This command can be implemented as an 8- or 16-bit command. The SDIO pin is a bi-directional pin. During the CSN low phase of the sequence, the SDIO pin is used as input pin to set the command byte. After CSN rising edge the pin SDIO is set as output pin, the data stored in the wiper register are read serially, MSB first. The wiper position is unchanged.

The data propagation starts at the second rising edge of SCLK after the rising edge of CSN. CSN must be high during the read operation. With the next falling edge of CSN the SDIO pin is set to an input pin again.

Figure 21. 8-Bit Command Word

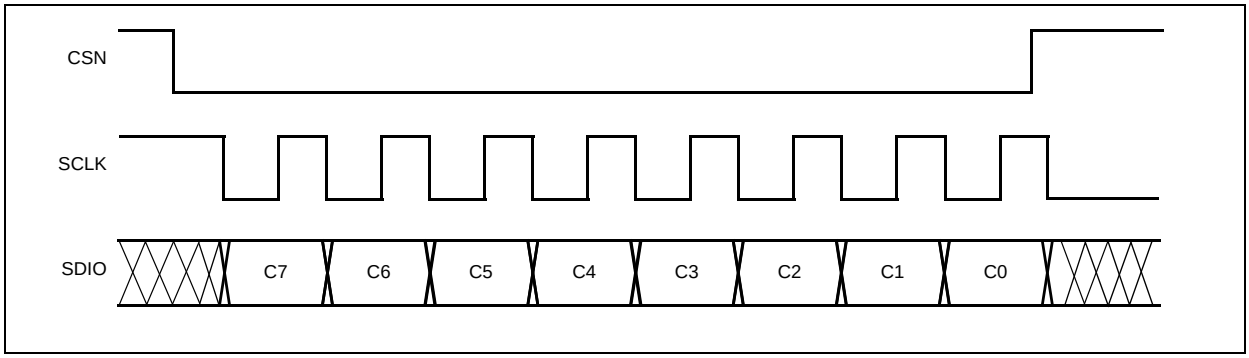


Figure 22. 16-Bit Command/Data Word

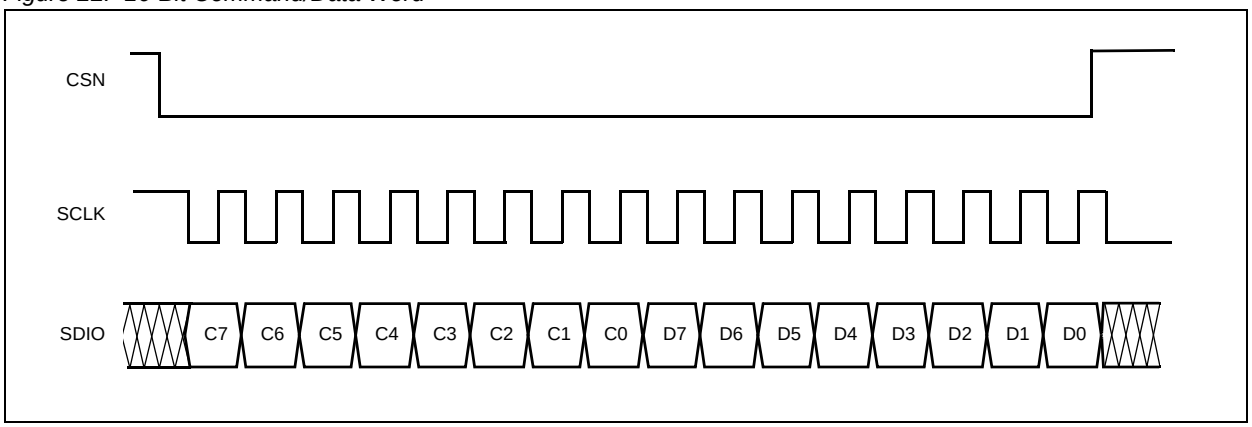
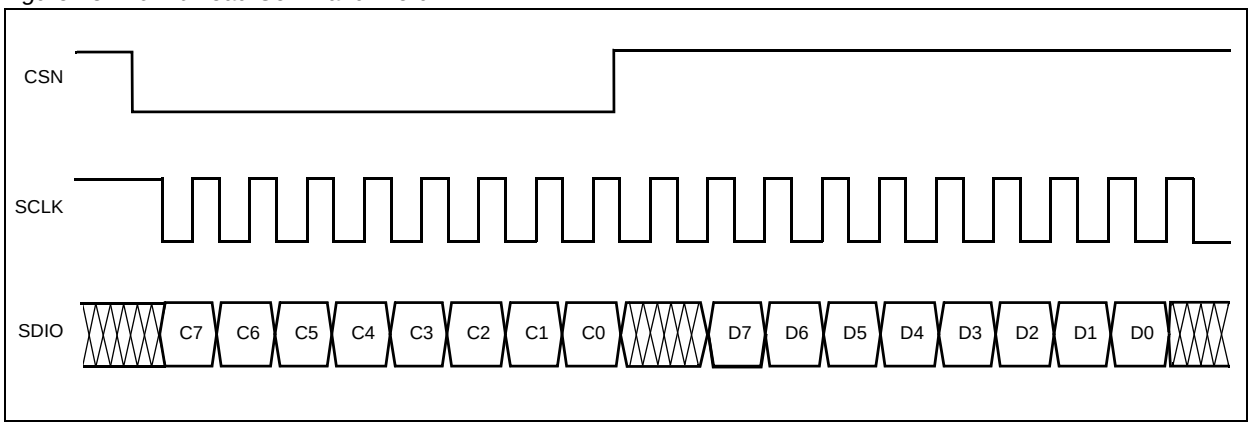


Figure 23. 16-Bit Read Command Word



9 Application Information

The AS1506 is intended for circuits requiring digitally controlled adjustable resistance, such as LCD contrast control (where voltage biasing adjusts the display contrast), or programmable filters with adjustable gain and/or cutoff frequency.

Programmable Filter

Figure 24 shows the configuration for a 1st-order programmable filter.

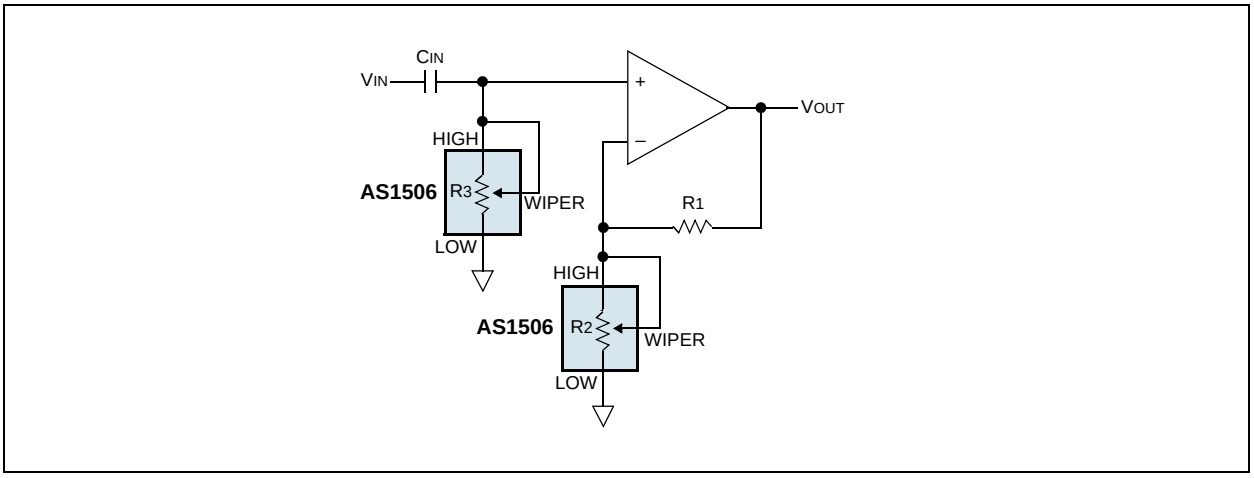
The DC gain of the filter is adjusted by R_2 and can be calculated as:

$$G = 1 + (R_1/R_2) \quad \text{(EQ 1)}$$

The cutoff frequency (f_C) is adjusted by R_3, and can be calculated as:

$$f_C = 1/(2\pi \times R_3 \times C) \quad \text{(EQ 2)}$$

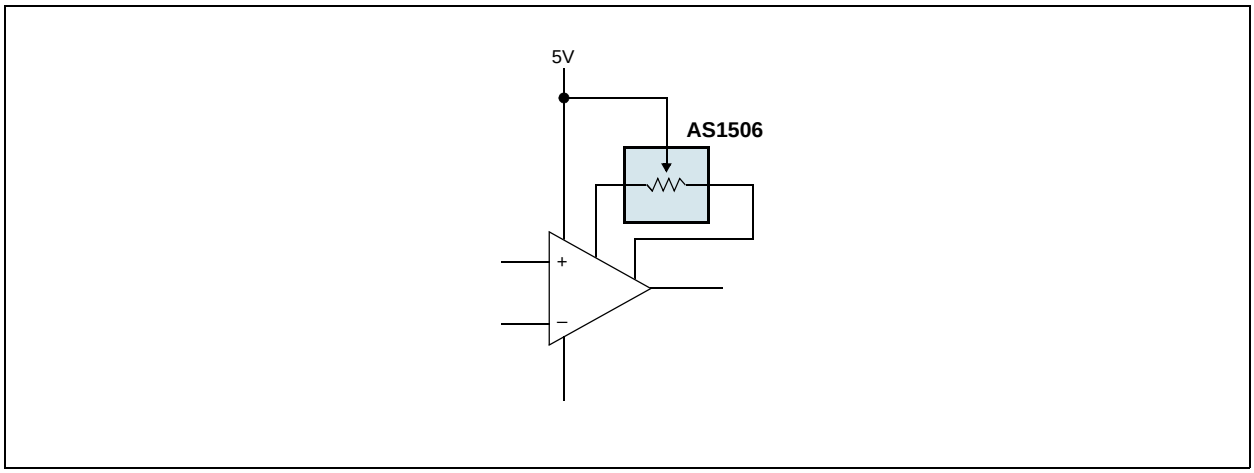
Figure 24. Programmable Filter Circuit



Offset Voltage and Gain Adjustment

Connect the AS1506 to an op amp to nullify the offset voltage over the operating temperature range. Install another AS1506 potentiometer in the feedback path to adjust the gain of the op amp (Figure 25).

Figure 25. Offset Voltage Adjustment Circuit



Positive LCD Bias Control

The device can be used in applications where a voltage-divider or variable resistor is used to make an adjustable, positive LCD-bias voltage, such as for the AS1120 LCD Driver. The op amp provides buffering and gain to the resistor-divider network made by the potentiometer (Figure 26) or to a fixed resistor and a variable resistor (Figure 27).

Figure 26. Positive LCD Bias Control using a Voltage Divider

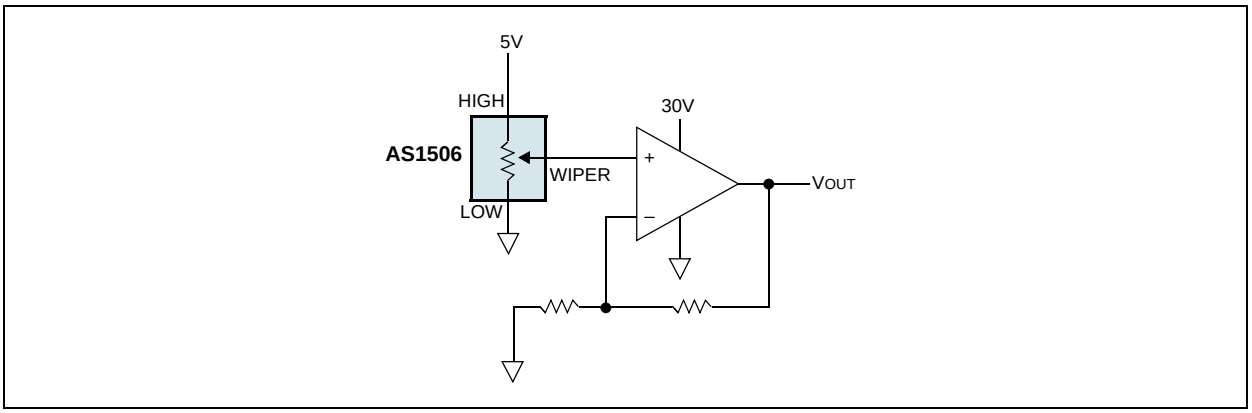
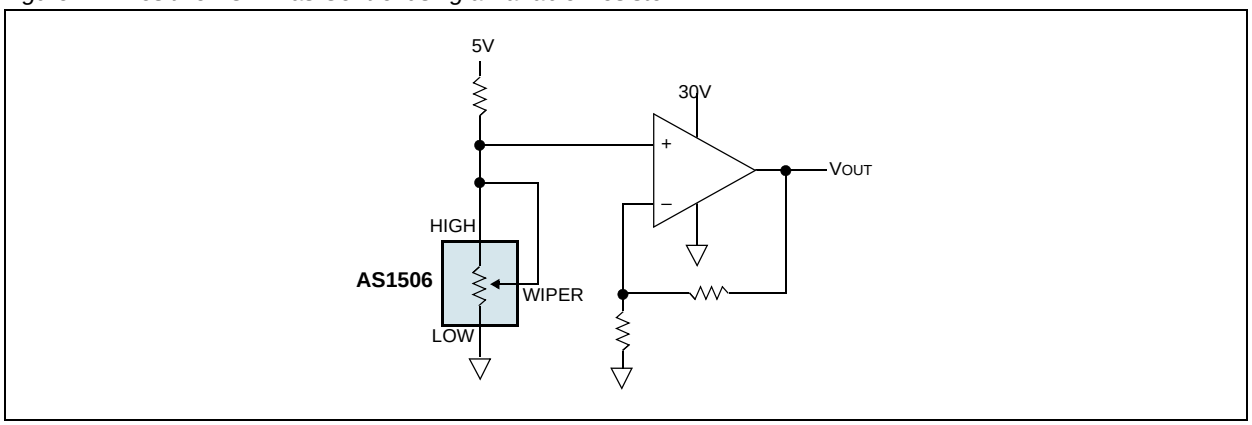


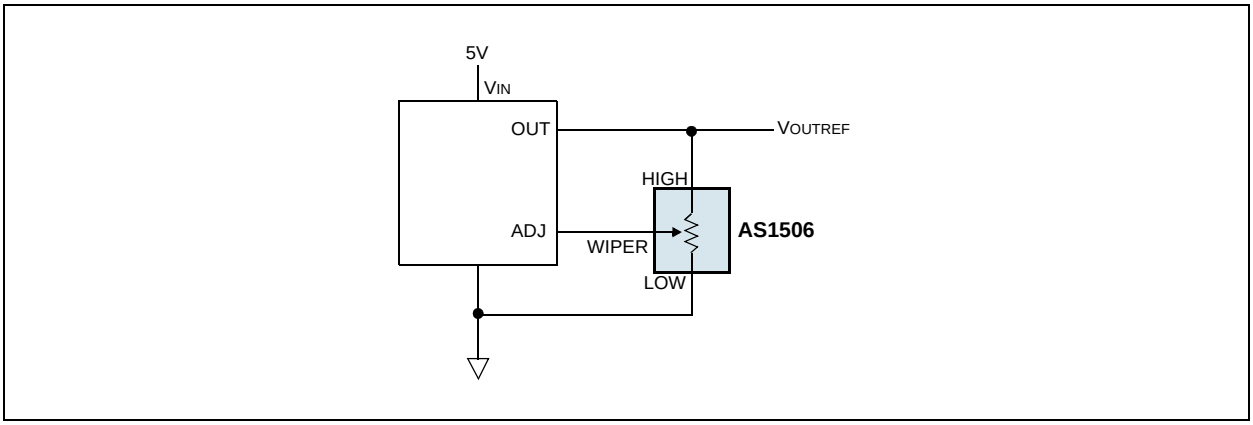
Figure 27. Positive LCD Bias Control using a Variable Resistor



Adjustable Voltage Reference

Figure 28 shows the device used as the feedback resistor in an adjustable voltage-reference application. Output voltages of external voltage references, supervisory reset thresholds, or LED brightness control can be independently adjusted by changing the wiper position of the AS1506.

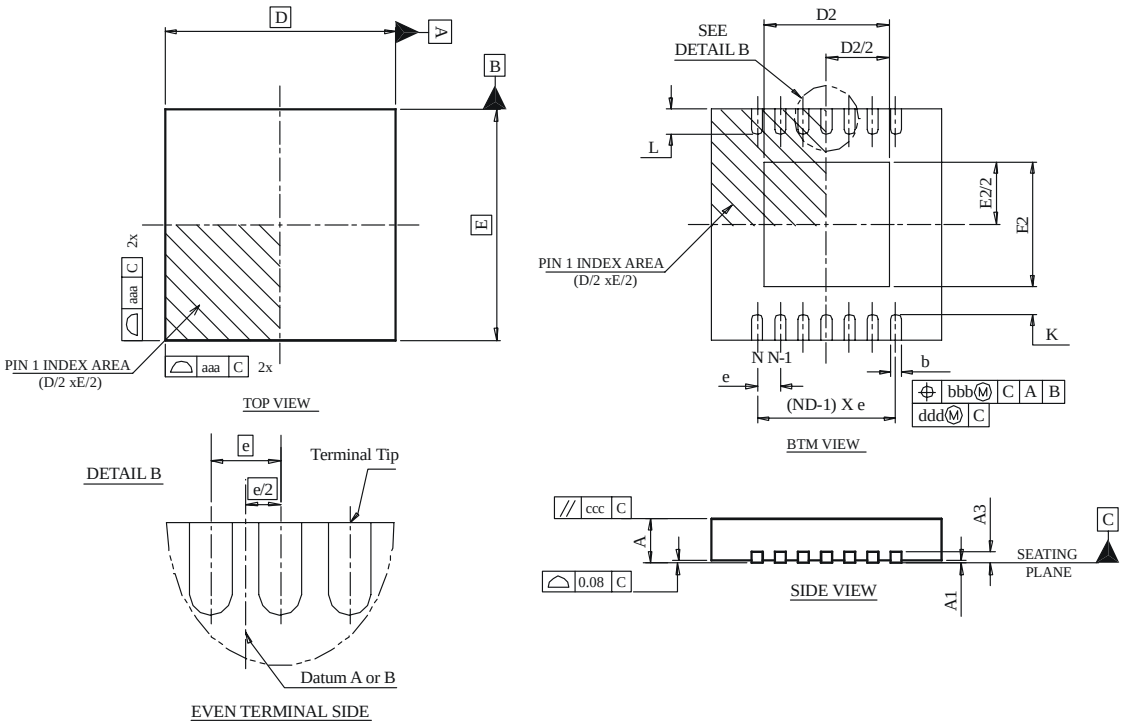
Figure 28. Adjustable Voltage Reference Circuit – V_{OUT} = 1.23V(50kΩ/R_2(kΩ)



10 Package Drawings and Markings

The device is available in an 8-pin TDFN 3x3mm package.

Figure 29. 8-pin TDFN 3x3mm Package



Symbol	Min	Typ	Max	Notes
A	0.70	0.75	0.80	1, 2
A1	0.00	0.02	0.05	1, 2
A3		0.20 REF		1, 2
L1			0.15	1, 2
L2			0.13	1, 2
aaa		0.15		1, 2
bbb		0.10		1, 2
ccc		0.10		1, 2
ddd		0.05		1, 2
eee		0.08		1, 2
ggg		0.10		1, 2

Symbol	Min	Typ	Max	Notes
D BSC		3.00		1, 2
E BSC		3.00		1, 2
D2	1.60		2.50	1, 2
E2	1.35		1.75	1, 2
L	0.30	0.40	0.50	1, 2
θ	0º		14º	1, 2
K	0.20			1, 2
b	0.25	0.30	0.35	1, 2, 5
e		0.65		
N		8		1, 2
ND		4		1, 2, 5

Notes:

1. Figure 29 is shown for illustration only.
2. All dimensions are in millimeters; angles in degrees.
3. Dimensioning and tolerancing conform to *ASME Y14.5 M-1994*.
4. N is the total number of terminals.
5. The terminal #1 identifier and terminal numbering convention shall conform to *JEDEC 95-1, SPP-012*. Details of terminal #1 identifier are optional, but must be located within the zone indicated. The terminal #1 identifier may be either a mold or marked feature.
6. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
7. ND refers to the maximum number of terminals on side D.
8. Unilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals

11 Ordering Information

The device is available as the standard products shown in Table 7.

Table 7. Ordering Information

Ordering Code	Marking	Description	End-to-End Resistance	Delivery Form	Package
AS1506-BTDT-10	ASMO	256-Tap, Non-Volatile, SPI Digital Potentiometer	10kΩ	Tape and Reel	8-pin TDFN 3x3mm
AS1506-BTDT-50	ASMN	256-Tap, Non-Volatile, SPI Digital Potentiometer	50kΩ	Tape and Reel	8-pin TDFN 3x3mm
AS1506-BTDT-100	ASMM	256-Tap, Non-Volatile, SPI Digital Potentiometer	100kΩ	Tape and Reel	8-pin TDFN 3x3mm

Note: All products are RoHS compliant and Pb-free.
Buy our products or get free samples online at ICdirect: http://www.austriamicrosystems.com/ICdirect

For further information and requests, please contact us mailto:sales@austriamicrosystems.com
or find your local distributor at http://www.austriamicrosystems.com/distributor

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