Si5344H, Si5342H Family Revision C and D Reference Manual

High-Frequency, Ultra-Low Jitter Attenuator Clock with Digitally Controlled Oscillator

This Family Reference Manual is intended to provide system, PCB design, signal integrity, and software engineers the necessary technical information to successfully use the Si5344H/42H devices in end applications. The official device specifications can be found in the Si5344H/42H data sheets.

Related Documents:

- Si5344H/42H Data Sheet
- Si5344H-EVB User Guide

KEY FEATURES

- Status monitoring (LOS, OOF, LOL)
- Hitless input clock switching: automatic or manual
- Automatic free-run and holdover modes
- Glitchless on the fly output frequency changes
- Locks to gapped clock inputs
- DCO mode: as low as 0.001 ppb steps.
- Core voltage
  - V_{DD}: 1.8 V ±5%
  - V_{DDA}: 3.3 V ±5%
- Independent output supply pins: 3.3 V, 2.5 V, or 1.8 V
- Serial interface: I^2C or SPI
- In-circuit programmable with non-volatile OTP memory
- ClockBuilder ProTM software simplifies device configuratio
- Si5342H: 2 input, 2 output, QFN44
- Si5344H, 2 input, 4 output, QFN44
- Temperature range: –40 to +85 °C
- Pb-free, RoHS-6 compliant

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1. Overview

The Si5344H/42H jitter attenuating clock multipliers combine 4th generation DSPLL and MultiSynth™ technologies to enable any-frequency clock generation for applications that require the highest level of jitter performance. These devices are programmable via a serial interface with in-circuit programmable non-volatile memory (NVM) ensuring power up with a known frequency configuration. Free-run, synchronous, and holdover modes of operation are supported offering both automatic and manual input clock switching. The loop filter is fully integrated on-chip eliminating the risk of potential noise coupling associated with discrete solutions. Further, the jitter attenuation bandwidth is digitally programmable providing jitter performance optimization at the application level.

These devices are capable of generating any combination of output frequency from any input frequency within the specified input and output range.

1.1 Workflow Expectations with ClockBuilder Pro™ and the Register Map

This reference manual is to be used to describe all the functions and features of the parts in the product family with register map details on how to implement them. It is important to understand that the intent is for customers to use the ClockBuilder Pro software to provide the initial configuration for the device. Although the register map is documented, all the details of the algorithms to implement a valid frequency plan are fairly complex and are beyond the scope of this document. Real-time changes to the frequency plan and other operating settings are supported by the devices. However, describing all the possible changes is not a primary purpose of this document. Refer to Applications Notes and Knowledge Base article links within the ClockBuilder Pro GUI for information on how to implement the most common, real-time frequency plan changes.

The primary purpose of the software is that it saves having to understand all the complexities of the device. The software abstracts the details from the user to allow focus on the high level input and output configuration, making it intuitive to understand and configure for the end application. The software walks the user through each step, with explanations about each configuration step in the process to explain the different options available. The software will restrict the user from entering an invalid combination of selections. The final configuration settings can be saved, written to an EVB and a custom part number can be created for customers who prefer to order a factory preprogrammed device. The final register maps can be exported to text files, and comparisons can be done by viewing the settings in the register map described in this document.

1.2 Family Product Comparison

The table below lists a comparison of the different family members.

Table 1.1. Product Selection Guide

Part Number	Number of Inputs	Number of MultiSynths	Number of Outputs	Package Type
Si5342H	2	2	2	44-QFN
Si5344H	2	4	4	44-QFN

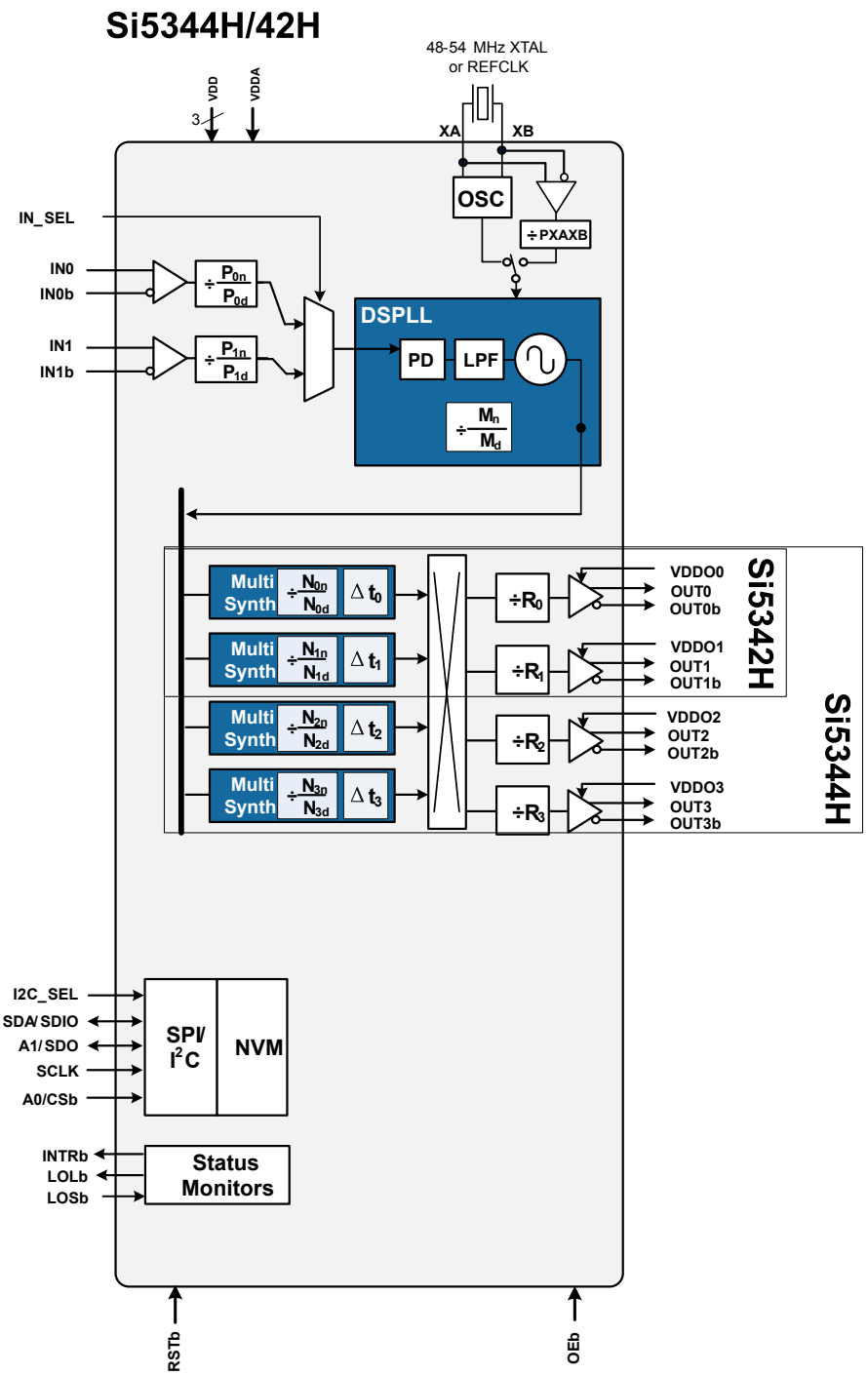


Figure 1.1. Block Diagram Si5344H/42H

1.3 Available Software Tools and Support

ClockBuilder Pro is a software tool that is used for the Si5344H/42H family and other product families, capable of configuring the timing chip in an intuitive, easy-to-use, step-by-step process. The software abstracts the details from the user to allow focus on the high level input and output configuration, making it intuitive to understand and configure for the end application. The software walks the user through each step, with explanations about each configuration step in the process to explain the different options available. The software will restrict the user from entering an invalid combination of selections. The final configuration settings can be saved, written to a device or written to the EVB and a custom part number can be created. This is all done with one software tool. ClockBuilder Pro integrates all the data sheets, application notes and information that might be helpful in one environment. It is intended that customers will use the software tool for the proper configuration of the device. Register map descriptions given in the document should not be the only source of information for programming the device. The complexity of the algorithms is embedded in the software tool.

2. DSPLL and MultiSynth

The DSPLL is responsible for input frequency translation, jitter attenuation and wander filtering. Fractional input dividers (Pxn/Pxd) allow the DSPLL to perform hitless switching between input clocks (INx) that are fractionally related. Input switching is controlled manually or automatically using an internal state machine. The oscillator circuit (OSC) provides a frequency reference which determines output frequency stability and accuracy while the device is in free-run or holdover mode. Note that a XTAL (or suitable XO reference on XA/XB) is always required and is the jitter reference for the device. The high-performance MultiSynth dividers (Nxn/Nxd) generate integer or fractionally related output frequencies for the output stage. A crosspoint switch connects any of the MultiSynth generated frequencies to any of the outputs. A single MultiSynth output can connect to two or more output drivers. Additional integer division (R) determines the final output frequency as shown in the figure below.

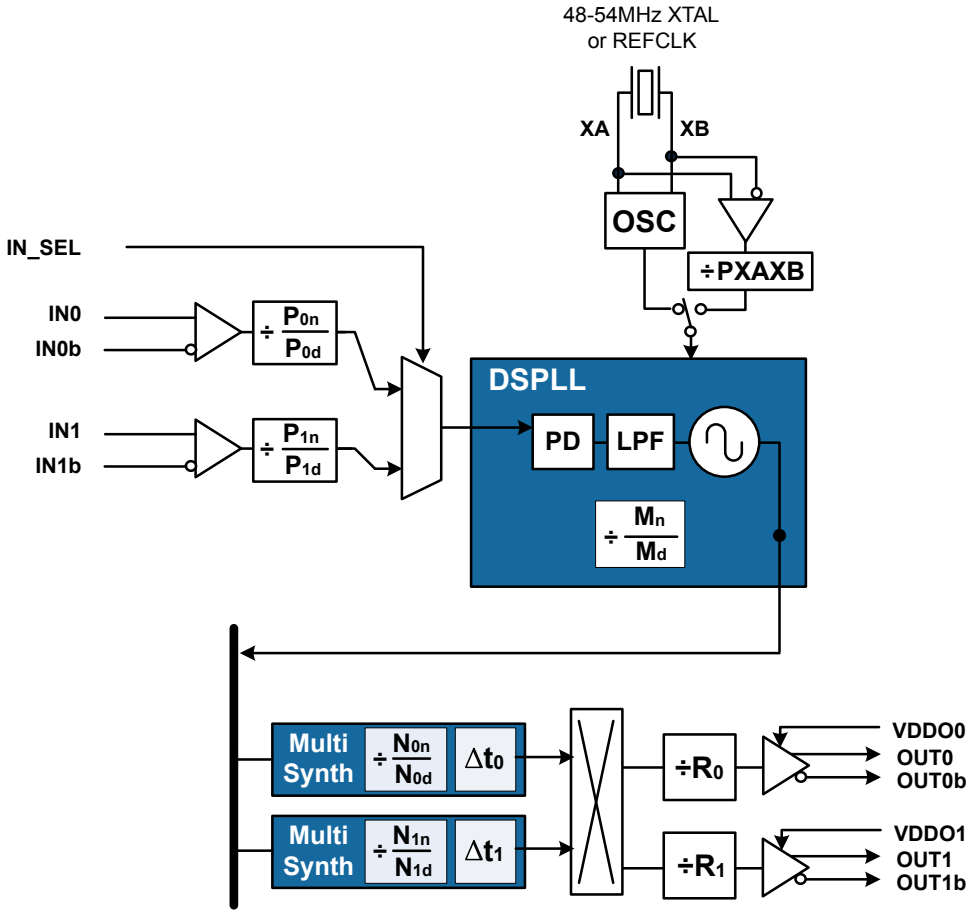


Figure 2.1. Si5342H DSPLL and Multisynth System Flow Diagram

The frequency configuration of the DSPLL is programmable through the SPI or I^2C serial interface and can also be stored in non-volatile memory or RAM. The combination of fractional input dividers (Pn/Pd), fractional frequency multiplication (Mn/Md), fractional output MultiSynth division (Nn/Nd), and integer output division (Rn) allows the generation of virtually any output frequency on any of the outputs. All divider values for a specific frequency plan are easily determined using the ClockBuilder Pro software.

2.1 Dividers

There are five divider classes within the Si5344H/42H. See Figure Figure 1.1 Block Diagram Si5344H/42H on page 6 for a block diagram that shows all of these dividers.

- Wide range input dividers P1, P0
  - MultiSynth divider
  - 48 bit numerator, 32 bit denominator
  - Min value is 1
  - Practical range limited by phase detector and VCO range
  - Each divider has an update bit that must be written to cause a newly written divider value to take effect.
- Narrow range input divider Pxaxb
  - Only divides by 1, 2, 4, 8
- Feedback M divider
  - MultiSynth divider
  - Integer or fractional divide values
  - 56 bit numerator, 32 bit denominator
  - Practical range limited by phase detector and VCO range
  - Each divider has an update bit that must be written to cause a newly written divider value to take effect.
- Output N divider
  - MultiSynth divider
  - Integer or fractional divide values
  - 44 bit numerator, 32 bit denominator
  - Each divider has an update bit that must be written to cause a newly written divider value to take effect.
  - Fractional divide values > 10 are supported. Integer divider values of 6, 7, 8, 9, and 10 are also supported.
- Output R divider
  - Only even integer divide values
  - Min value is 2. R divider is bypassed for high-frequency outputs.
  - Maximum value is $2^{25} – 2$

2.2 DSPLL Loop Bandwidth

The DSPLL loop bandwidth determines the amount of input clock jitter attenuation and wander filtering. Register configurable DSPLL loop bandwidth settings in the range of 0.1 Hz to 4 kHz are available for selection. Since the loop bandwidth is controlled digitally, the DSPLL will always remain stable with less than 0.1 dB of peaking regardless of the loop bandwidth selection. The DSPLL loop bandwidth is set in registers 0x0508-0x050D and are determined using ClockBuilder Pro.

Table 2.1. PLL_BW Registers

Register Name	Hex Address [Bit Field]		Function
	Si5344H	Si5342H	
BW_PLL	0x0508[7:0]-0x050D[7:0]	0x0508[7:0]-0x050D[7:0]	Determines the loop BW for the DSPLL.

2.2.1 Fastlock Feature

Selecting a low DSPLL loop bandwidth (e.g. 0.1 Hz) will generally lengthen the lock acquisition time. The fastlock feature allows setting a temporary fastlock loop bandwidth that is used during the lock acquisition process. Higher fastlock loop bandwidth settings will enable the DSPLL to lock faster. Fastlock Loop Bandwidth settings in the range from 100 Hz to 4 kHz are available for selection. The DSPLL will revert to its normal loop bandwidth once lock acquisition has completed.

Table 2.2. Fastlock Registers

Register Name	Hex Address [Bit Field]		Function
	Si5344H	Si5342H	
FASTLOCK_AUTO_EN	0x052B[0]	0x052B[0]	Auto Fastlock Enable/Disable
FASTLOCK_MAN	0x052B[1]	0x052B[1]	0 for normal operation, 1 to force fast lock
FAST_BW_PLL	0x050E[7:0]-0x0513[7:0]	0x050E[7:0]-0x0513[7:0]	Fastlock BW selection.

The loss of lock (LOL) feature is a fault monitoring mechanism. Details of the LOL feature can be found in 4.3.3 Loss of Lock Fault Monitoring.

3. Modes of Operation

After initialization the DSPLL will operate in one of the following modes: Free-run, lock-acquisition, locked, or holdover.

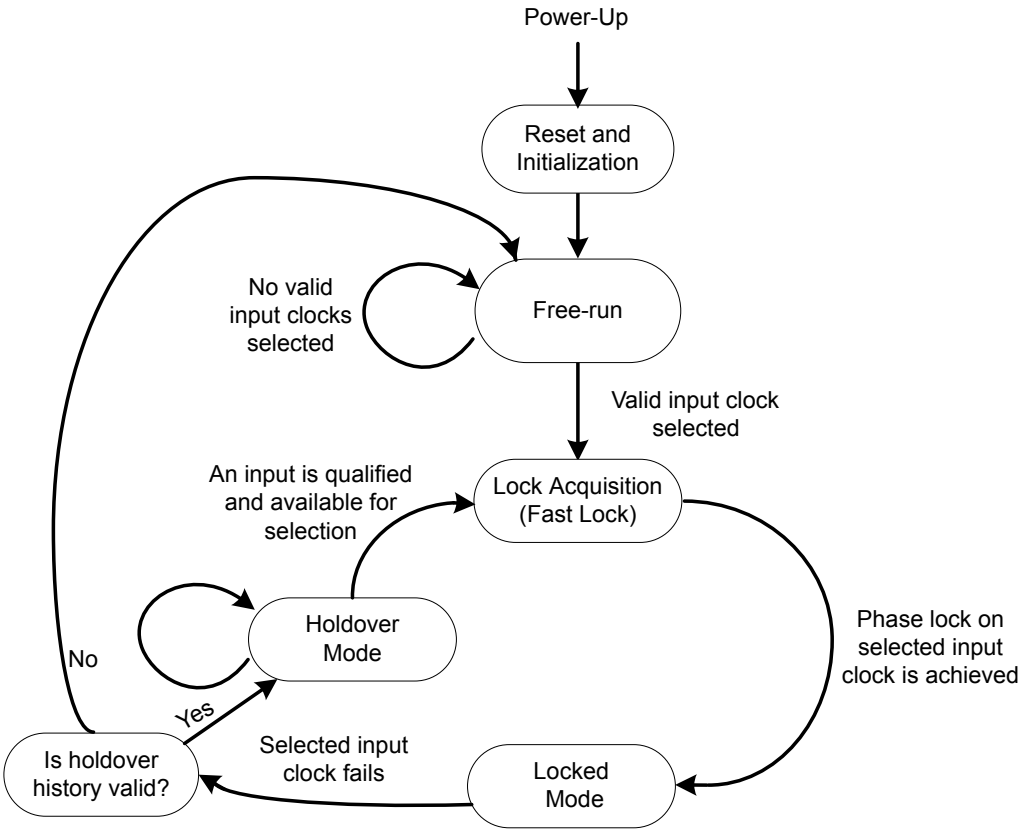


Figure 3.1. Modes of Operation

3.1 Reset and Initialization

Once power is applied, the device begins an initialization period where it downloads default register values and configuration data from NVM and performs other initialization tasks. Communicating with the device through the SPI or I^2C serial interface is possible once this initialization period is complete. No clocks will be generated until the initialization is complete. There are two types of resets available: hard reset and soft reset. A hard reset is functionally similar to a device power-up. All registers will be restored to the values stored in NVM, and all circuits including the serial interface will be restored to their initial state. A hard reset is initiated using the RST pin or by asserting the hard reset bit. A soft reset bypasses the NVM download. It is simply used to initiate register configuration changes. Table 3.1 Reset Registers on page 11 lists the reset and control registers.

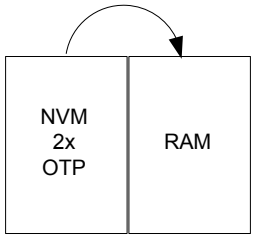


Figure 3.2. Si5344H/42H Memory Configuration

Table 3.1. Reset Registers

Register Name	Hex Address [Bit Field]		Function
	Si5344H	Si5342H	
HARD_RST	0x001E[1]	0x001E[1]	Performs the same function as power cycling the device. All registers will be restored to their default values.
SOFT_RST	0x001C[0]	0x001C[0]	Performs a soft reset. Initiates register configuration changes.

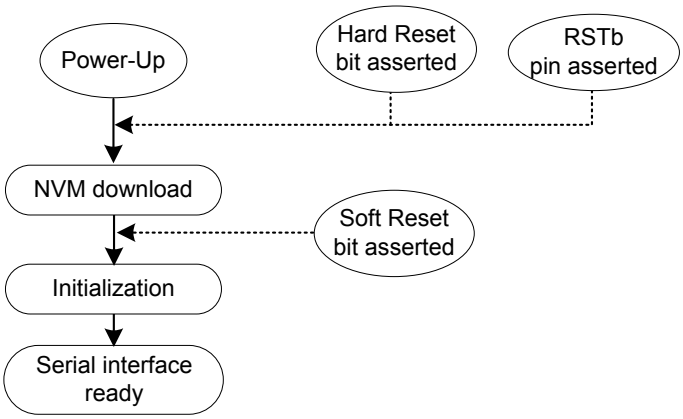


Figure 3.3. Initialization from Hard Reset and Soft Reset

The Si5344H/42H is fully configurable using the serial interface (I^2C or SPI). At power up the device downloads its default register values from internal non-volatile memory (NVM). Application specific default configurations can be written into NVM allowing the device to generate specific clock frequencies at power-up. Writing default values to NVM is in-circuit programmable with normal operating power supply voltages applied to its VDD (1.8 V) and VDDA (3.3 V) pins.

3.2 Dynamic PLL Changes

3.2.1 Revision C and D

It is possible for a PLL to become unresponsive (i.e., lose lock indefinitely) when it is dynamically reprogrammed or changed via the serial port. Reprogramming/changing the N divider does not affect the PLL. Any change that causes the VCO frequency to change by more than 250 ppm since Power-up, NVM download, or SOFT_RST requires the following special sequence of writes. Changes to the following registers require the following special sequence of writes:

- XAXB_FREQ_OFFSET
- PXAXB
- MXAXB_NUM
- MXAXB_DEN
- M_NUM
- M_DEN

1. First, the preamble

Write 0x0B24 = 0xC0

Write 0x0B25 = 0x00

Write 0x0540 = 0x01 (NOTE: for all new designs it is recommend that this register be written as part of the preamble. In some rare cases, omitting this write may result in a one-time LOL occurrence. However, if this issue has not occurred with your current frequency plan it is not likely to occur)

2. Wait 300 ms.

3. Then perform the desired register modifications

4. Write SOFT_RST - 0x001C[0] = 1

5. Write the post-amble

Write 0x0540 = 0x00 (NOTE: for all new designs it is recommend that this register be written as part of the post-amble. In some rare cases, omitting this write may result in a one-time LOL occurrence. However, if this issue has not occurred with your current frequency plan it is not likely to occur)

Write 0x0B24 = 0xC3

Write 0x0B25 = 0x02

3.3 NVM Programming

The NVM is two time writable. Because it can only be written two times, it is important to configure the registers correctly before beginning the NVM programming process. Once a new configuration has been written to NVM, the old configuration is no longer accessible.

Note: In-circuit programming is only supported over a temperature range of 0° to 80 °C.

The procedure for writing registers into NVM is as follows:

1. Write all registers as needed.
2. You may write to the user scratch space (registers 0x026B to 0x0272) to identify the content of NVM bank.
3. Write 0xC7 to NVM_WRITE register.
4. Wait until DEVICE_READY = 0x0F.
5. Set NVM_READ_BANK 0x00E4[0] = “1”.
6. Wait until DEVICE_READY = 0x0F.
7. Steps 5 and 6 can be replaced by simply powering down and then powering up the device.

Table 3.2. NVM Programming Registers

Register Name	Hex Address [Bit Field]		Function
	Si5344H	Si5342H	
ACTIVE_NVM_BANK	0x00E3[7:0]	0x00E3[7:0]	Indicates number of user bank writes carried out so far.
NVM_WRITE	0x00E3[7:0]	0x00E3[7:0]	Initiates an NVM write when written with 0xC7
NVM_READ_BANK	0x00E4[0]	0x00E4[0]	Download register values with content stored in NVM
DEVICE_READY	0x00FE[7:0]	0x00FE[7:0]	Indicates that the device serial interface is ready to accept commands.

WARNING: Any attempt to read or write any register other than DEVICE_READY before DEVICE_READY reads as 0x0F may corrupt the NVM programming. Note that this includes writes to the PAGE register.

3.4 Free Run Mode

The DSPLL will automatically enter freerun mode once power is applied to the device and initialization is complete. The frequency accuracy of the generated output clocks in freerun mode is entirely dependent on the frequency accuracy of the external crystal or reference clock on the XA/XB pins. For example, if the crystal frequency is ±100 ppm, then all the output clocks will be generated at their configured frequency ±100 ppm in freerun mode. Any drift of the crystal frequency will be tracked at the output clock frequencies. A TCXO or OCXO is recommended for applications that need better frequency accuracy and stability while in freerun or holdover modes. Because there is little or no jitter attenuation from the XAXB pins to the clock outputs, a low-jitter XAXB source will be needed for low-jitter clock outputs.

3.5 Acquisition Mode

The device monitors all inputs for a valid clock. If at least one valid clock is available for synchronization, the DSPLL will automatically start the lock acquisition process. If the fast lock feature is enabled, the DSPLL will acquire lock using the Fastlock Loop Bandwidth setting and then transition to the DSPLL Loop Bandwidth setting when lock acquisition is complete. During lock acquisition the outputs will generate a clock that follows the VCO frequency change as it pulls-in to the input clock frequency.

3.6 Locked Mode

Once locked, the DSPLL will generate output clocks that are both frequency and phase locked to its selected input clock. At this point any XTAL frequency drift will typically not affect the output frequency. A loss of lock pin (LOL) and status bit indicate when lock is achieved. See Section 4.3.3 Loss of Lock Fault Monitoring for more details on the operation of the loss of lock circuit.

3.7 Holdover Mode

The DSPLL will automatically enter holdover mode when the selected input clock becomes invalid and no other valid input clocks are available for selection. The DSPLL uses an averaged input clock frequency as its final holdover frequency to minimize the disturbance of the output clock phase and frequency when an input clock suddenly fails. The holdover circuit for the DSPLL stores up to 120 seconds of historical frequency data while locked to a valid clock input. The final averaged holdover frequency value is calculated from a programmable window within the stored historical frequency data. Both the window size and the delay are programmable as shown in Figure 3.4 Programmable Holdover Window on page 14. The window size determines the amount of holdover frequency averaging. The delay value allows ignoring frequency data that may be corrupt just before the input clock failure.

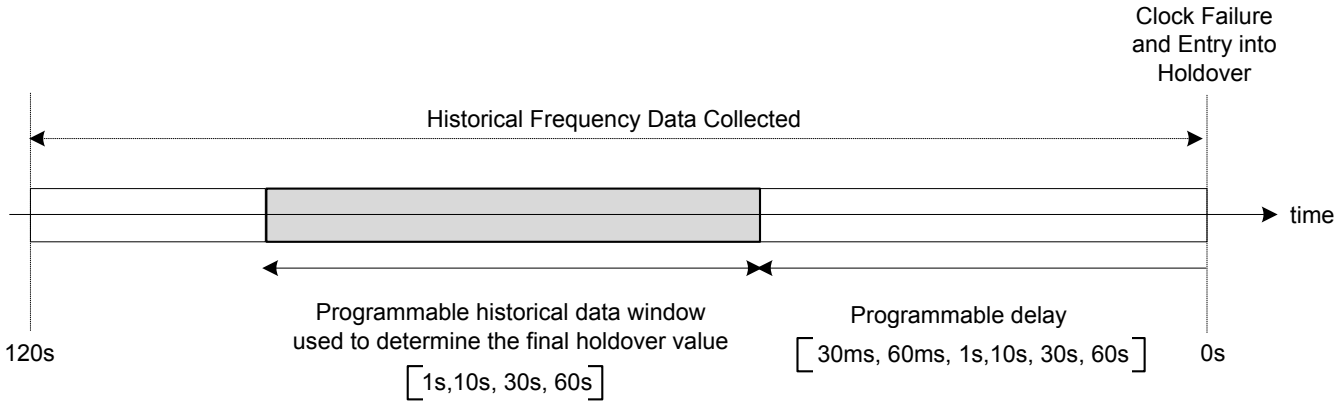


Figure 3.4. Programmable Holdover Window

When entering holdover, the DSPLL will pull its output clock frequency to the calculated averaged holdover frequency. While in holdover, the output frequency drift is entirely dependent on the external crystal or external reference clock connected to the XA/XB pins. If the clock input becomes valid, the DSPLL will automatically exit the holdover mode and re-acquire lock to the new input clock. This process involves pulling the output clock frequency to achieve frequency and phase lock with the input clock. This pull-in process is glitchless and its rate is controlled by the DSPLL bandwidth, the Fastlock bandwidth, or an artificial linear ramp rate selectable from 0.75 ppm/s up to 40 ppm/s. These options are register programmable.

Table 3.3. Holdover Mode Registers

Register Name	Hex Address [Bit Field]		Function
	Si5344H	Si5342H	
Holdover Status			
HOLD	0x000E[5]	0x000E[5]	Holdover status indicator. Indicates when the DSPLL is in holdover or free-run mode and not synchronized to an input clock on IN3, IN2, IN1, or IN0. The DSPLL is in holdover state only when the historical frequency data is valid; otherwise, the DSPLL should be considered to be in free-run mode.
HOLD_FLG	0x0013[5]	0x0013[5]	Holdover status monitor sticky bit. Sticky bits will remain asserted when an holdover event occurs until cleared. Writing a zero to a sticky bit will clear it.
HOLD_HIST_VALID	0x053F[1]	0x053F[1]	Holdover historical frequency data valid. Indicates if there is enough historical frequency data collected for valid holdover.
Holdover Control and Settings			
HOLD_HIST_LEN	0x052E[4:0]	0x052E[4:0]	Holdover historical average window. Selectable as 1 s, 10 s, 30 s, 60 s. Register values determined using ClockBuilder Pro
HOLD_HIST_DELAY	0x052F[4:0]	0x052F[4:0]	Holdover average delay window. Selectable as 30 ms, 60 ms, 1 s, 30 s, 60 s. Register values determined using ClockBuilder Pro
FORCE_HOLD	0x0535[0]	0x0535[0]	These bits allow forcing the DSPLL into holdover
HOLD_EXIT_BW_SEL	0x052C[4]	0x052C[4]	Selects the exit from holdover bandwidth. Options are: 0- exit out of holdover using the fastlock bandwidth 1- exit out of holdover using the DSPLL loop bandwidth
HOLD_RAMP_BYP	0x052C[3]	0x052C[3]	Must be set to 1 for normal operation.

4. Clock Inputs

The Si5344H/42H supports two inputs that can be used to synchronize to the internal DSPLL.

4.1 Inputs (IN0, IN1)

The inputs accept both standard format inputs and low-duty-cycle pulsed CMOS clocks. Input selection from CLK_SWITCH_MODE can be manual (pin or register controlled) or automatic with user definable priorities. Register 0x052A is used to select pin or register control, and to configure the input as shown below in Table 4.1 Input Selection Configuration on page 16.

Table 4.1. Input Selection Configuration

Register Name	Hex Address [Bit Field]		Function
	Si5344H	Si5342H	
CLK_SWITCH_MODE	0x0536[1:0]	0x0536[1:0]	Selects manual or automatic switching modes. Automatic mode can be revertive or non-revertive. Selections are the following: 00 Manual, 01 Automatic non-revertive 02 Automatic revertive, 03 Reserved
IN_SEL_REGCTRL	0x052A [0]	0x052A [0]	0 for pin controlled clock selection 1 for register controlled clock selection
IN_SEL	0x052A [1]	0x052A [1]	0 for IN0, 1 for IN1

4.1.1 Manual Input Switching

In manual mode, CLK_SWITCH_MODE=0x00.

Input switching can be done manually using the IN_SEL device pin from the package or through register 0x052A IN_SEL. Bit 0 of register 0x052A determines if the input selection is pin selectable or register selectable. The default is pin selectable. The following table describes the input selection on the pins. If there is no clock signal on the selected input, the device will automatically enter free-run or holdover mode.

Table 4.2. Manual Input Selection using IN_SEL Pin

IN_SEL DEVICE PINS	Input Clock Selected
0	IN0
1	IN1

4.1.2 Automatic Input Selection

In automatic mode CLK_SWITCH_MODE = 0x01 (non-revertive) or 0x02 (revertive)

An automatic input selection is available in addition to the above mentioned manual switching option described in 4.1.1 Manual Input Switching. In automatic mode, the selection criteria is based on input clock qualification, input priority and the revertive option. The IN_SEL pin or IN_SEL register bit is not used in automatic input selection. Also, only input clocks that are valid (i.e., with no active alarms) can be selected by the automatic clock selection. If there are no valid input clocks available the DSPLL will enter the holdover mode. With revertive switching enabled, the highest priority input with a valid input clock is always selected. If an input with a higher priority becomes valid then an automatic switchover to that input will be initiated. With non-revertive switching, the active input will always remain selected while it is valid. If it becomes invalid an automatic switchover to a valid input with the highest priority will be initiated.

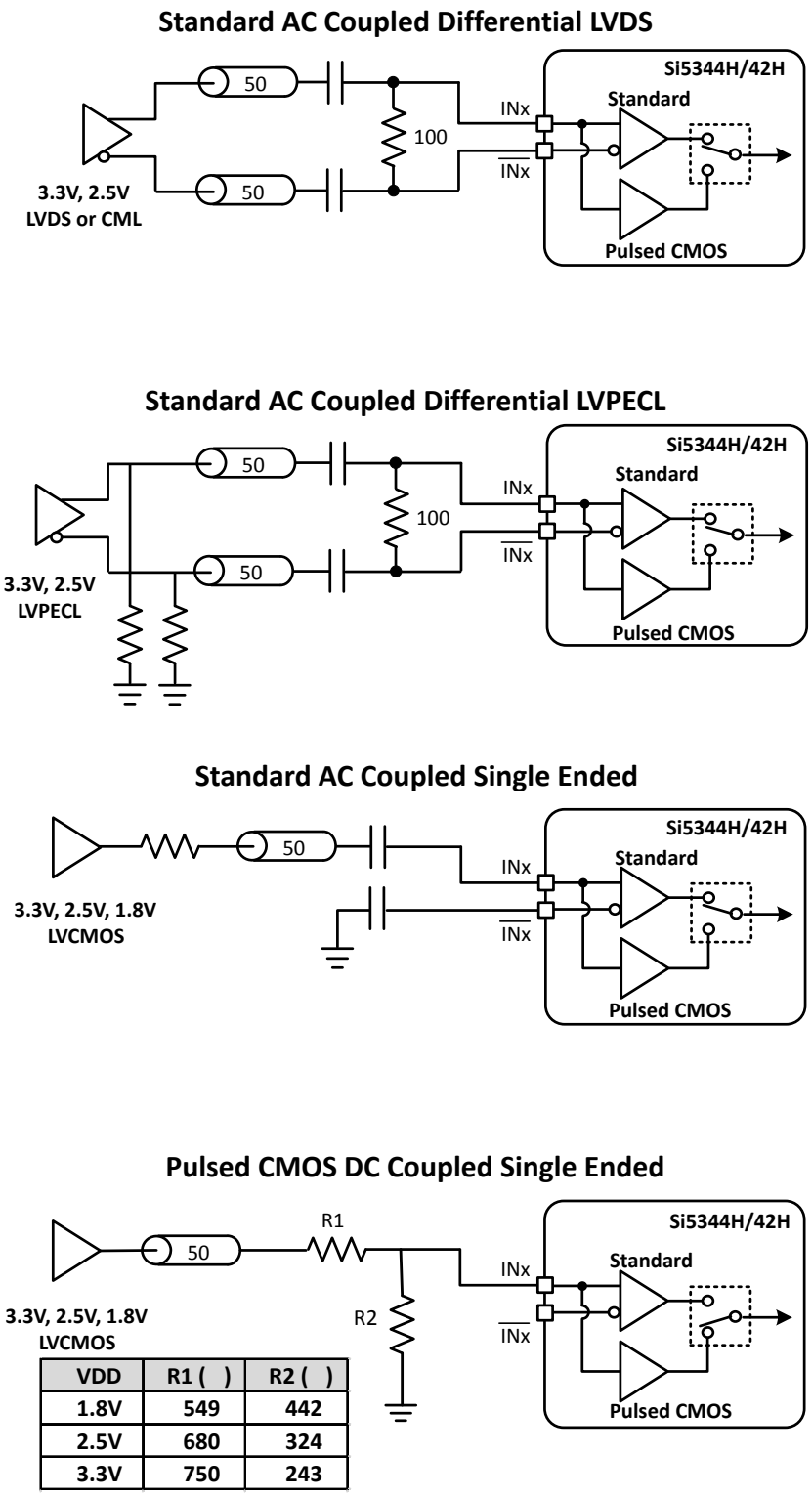
Table 4.3. Registers for Automatic Input Selection

Register Name	Hex Address [Bit Field]		Function
	Si5344H	Si5342H	
CLK_SWITCH_MODE	0x0536[1:0]	0x0536[1:0]	Selects manual or automatic switching modes. Automatic mode can be revertive or non-revertive. Selections are the following: 00 Manual, 01 Automatic non-revertive, 02 Automatic revertive, 03 Reserved
IN0_PRIORITY	0x0538[2:0]	0x0538[2:0]	IN0, IN1 priority select for the automatic selection state machine. Priority selections are 1,2, or zero for never selected.
IN1_PRIORITY	0x0538[6:4]	0x0538[6:4]	
IN_LOS_MSK	0x0537[3:0]	0x0537[3:0]	Determines the LOS status for IN1, IN0 and is used in determining a valid clock for automatic input selection. 0 to use LOS in clock selection logic, 1 to mask LOS from the clock selection logic.
IN_OOF_MSK	0x0537[7:4]	0x0537[7:4]	Determines the OOF status for IN1, IN0 and is used in determining a valid clock for the automatic input selection. 0 to use OOF in the clock selection logic, 1 to mask the OOF from the clock selection logic.

When IN_SEL_REGCTRL is low, IN_SEL register does not do anything and the clock selection is pin controlled.

4.2 Types of Inputs

Each of the inputs can be configured as standard LVDS, LVPECL, HCL, CML, and single-ended LVCMOS formats, or as a low duty cycle pulsed CMOS format. The standard format inputs have a nominal 50% duty cycle, must be AC-coupled and use the “Standard” Input Buffer selection as these pins are internally dc-biased to approximately 0.83 V. The pulsed CMOS input format allows pulse-based inputs, such as frame-sync and other synchronization signals, having a duty cycle much less than 50%. These pulsed CMOS signals are DC-coupled and use the “Pulsed CMOS” Input Buffer selection. In all cases, the inputs should be terminated near the device input pins as shown in Figure 4.1 Input Termination for Standard and Pulsed CMOS Inputs on page 19. The resistor divider values given below will work with up to 1 MHz pulsed inputs. In general, following the “Standard AC Coupled Single Ended” arrangement shown below will give superior jitter performance.



VDD	R1 ( )	R2 ( )
1.8V	549	442
2.5V	680	324
3.3V	750	243

Figure 4.1. Input Termination for Standard and Pulsed CMOS Inputs

Input clock buffers are enabled by setting the IN_EN 0x0949[1] bits appropriately for IN1 and IN0. Unused clock inputs may be powered down and left unconnected at the system level. For standard mode inputs, both input pins must be properly connected as shown in Figure 4.1 Input Termination for Standard and Pulsed CMOS Inputs on page 19 above, including the “Standard AC Coupled Single Ended” case. In Pulsed CMOS mode, it is not necessary to connect the inverting INxb input pin. To place the input buffer into Pulsed CMOS mode, the corresponding bit must be set in IN_PULSED_CMOS_EN 0x0949[5:4] for IN1 and IN0.

Table 4.4. Register 0x0949 Clock Input Control and Configuration

Register Name	Hex Address [Bit Field]		Function
	Si5344H	Si5342H	
IN_EN	0x0949[1:0]	0x0949[1:0]	Enables for the input clocks IN1, IN0. 1 to enable.
IN_PULSED_CMOS_EN	0x0949[5:4]	0x0949[5:4]	Selects CMOS or differential receiver for IN1, IN0. Defaults to differential input. Differential=0, CMOS=1

4.2.1 Unused Inputs

Unused inputs can be disabled and left unconnected when not in use. Register 0x0949[1:0] defaults the input clocks to being enabled. Clearing the unused input bits will disable them.

4.2.2 Hitless Input Switching

Hitless switching is a feature that prevents a phase transient from propagating to the output when switching between two clock inputs that have a fixed phase relationship. A hitless switch can only occur when the two input frequencies are frequency locked, which means that they have to be exactly the same frequency. When hitless switching is enabled (register 0x0536 bit 2 = 1), the DSPLL absorbs the phase difference between the current input clock and the new input clock. When disabled (register 0x0536 bit 2 = 0), the phase difference between the two inputs will propagate to the output at a rate determined by the DSPLL Loop Bandwidth. The hitless switching feature supports clock frequencies down to the minimum input frequency of 8 kHz.

Table 4.5. Hitless Switching Enable Bit

Register Name	Hex Address [Bit Field]		Function
	Si5344H	Si5342H	
HSW_EN	0x0536[2]	0x0536[2]	Hitless switching is enabled = 1, or disabled = 0.

For the Si5344H/42H to meet the hitless switching specification, there are restrictions on the clock input frequencies and the use of fractional P input dividers. When an input P divider is fractional, the associated input frequency must be 300 MHz or higher to meet the hitless switching specifications.

4.2.3 Glitchless Input Switching

The DSPLL has the ability to switch between two input clock frequencies that are up to ±500 ppm apart. The DSPLL will pull-in to the new frequency at a rate determined by the DSPLL loop bandwidth. The DSPLL loop bandwidth is set using registers 0x0508–0x050D. Note that if “Fastlock” is enabled then the DSPLL will pull-in to the new frequency using the Fastlock Loop Bandwidth. Depending on the LOL configuration settings, the loss of lock (LOL) indicator may assert while the DSPLL is pulling-in to the new clock frequency. There will never be output runt pulses generated at the output during the transition.

4.2.4 Synchronizing to Gapped Input Clocks

The DSPLL supports locking to an input clock that has missing clock periods. This is also referred to as a gapped clock. The purpose of gapped clocking is to modulate the frequency of a periodic clock by selectively removing some of its cycles. Gapping a clock severely increases its jitter so a phase-locked loop with high jitter tolerance and low loop bandwidth is required to produce a low-jitter, truly periodic clock. The resulting output will be a periodic non-gapped clock with an average frequency of the input with its missing cycles. For example, an input clock of 100 MHz with one cycle removed every 10 cycles will result in a 90 MHz periodic non-gapped output clock. A valid gapped clock input must have a minimum frequency of 10 MHz with a maximum of two missing cycles out of every eight.

When properly configured, locking to a gapped clock will not trigger the LOS, OOF, and LOL fault monitors. Clock switching between gapped clocks may violate the hitless switching specification of up to 1.5 ns for a maximum phase transient, when the switch occurs during a gap in either input clocks. The figure below shows a 100 MHz clock with one cycle removed every 10 cycles, which results in a 90 MHz periodic non-gapped output clock.

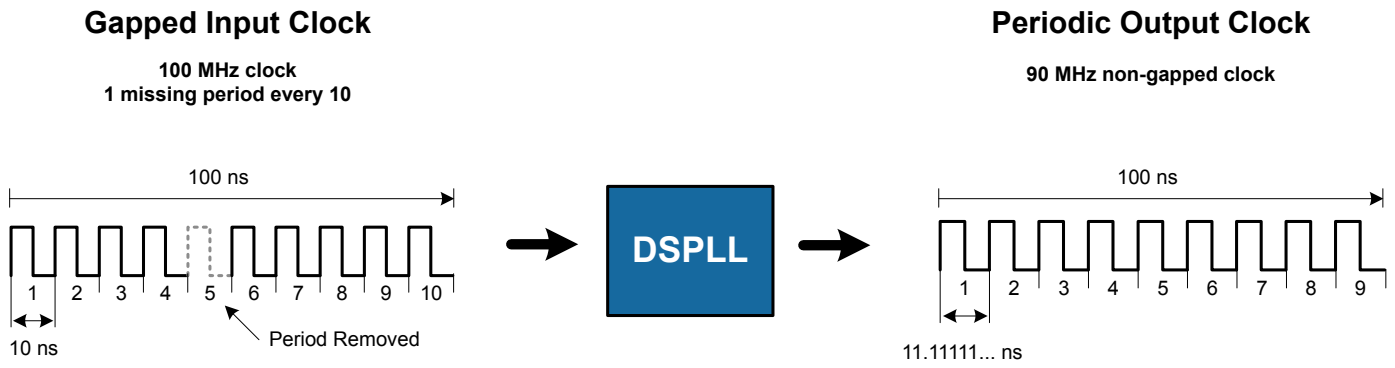


Figure 4.2. Generating an Averaged Non Gapped Output Frequency from a Gapped Input

4.3 Fault Monitoring

The input clocks (IN0, IN1) are monitored for loss of signal (LOS) and out-of-frequency (OOF). Note that the reference at the XA/XB pins is also monitored for LOS since it provides a critical reference clock for the DSPLL. There is also a Loss of Lock (LOL) indicator asserted when the DSPLL loses synchronization within the feedback loop. The figure below shows the fault monitors for each input path going into the DSPLL, which includes the crystal input as well as IN0/IN1.

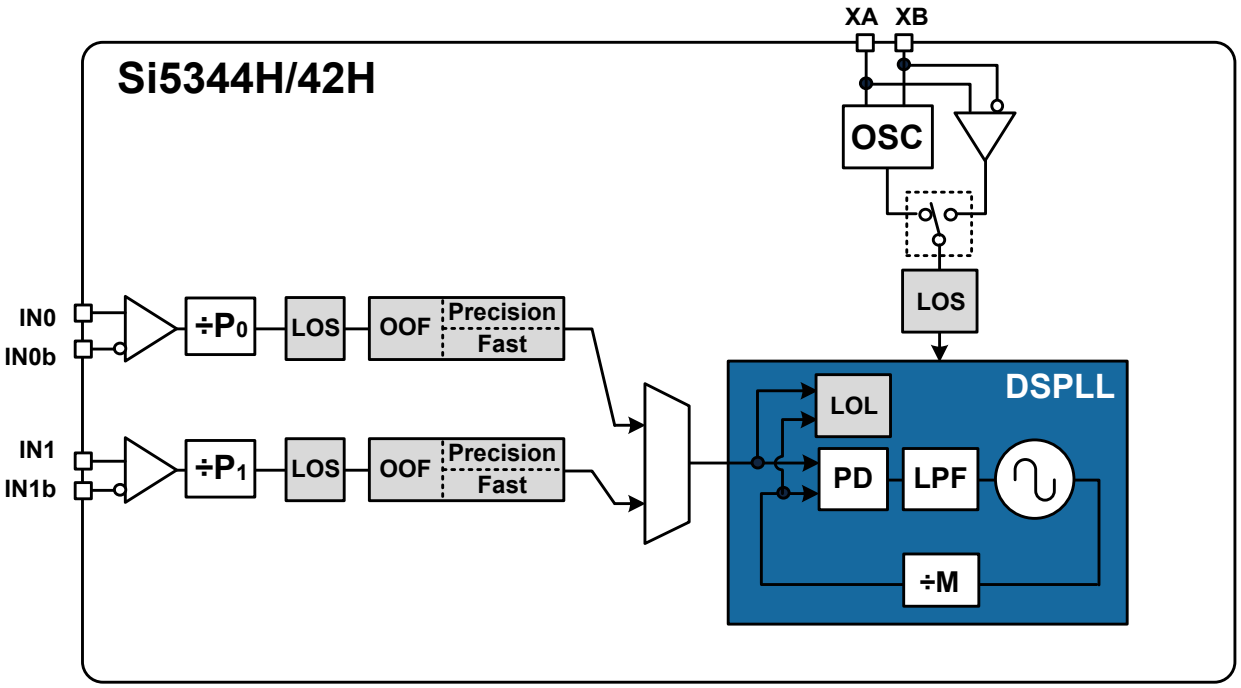


Figure 4.3. Si5344H/42H Fault Monitors

4.3.1 Input Loss of Signal (LOS) Fault Detection

The loss of signal monitor measures the period of each input clock cycle to detect phase irregularities or missing clock edges. Each of the input LOS circuits has its own programmable sensitivity which allows ignoring missing edges or intermittent errors. Loss of signal sensitivity is configurable using the ClockBuilder Pro utility. The LOS status for each of the monitors is accessible by reading a status register. The live LOS register always displays the current LOS state and a sticky register when set, always stays asserted until cleared.

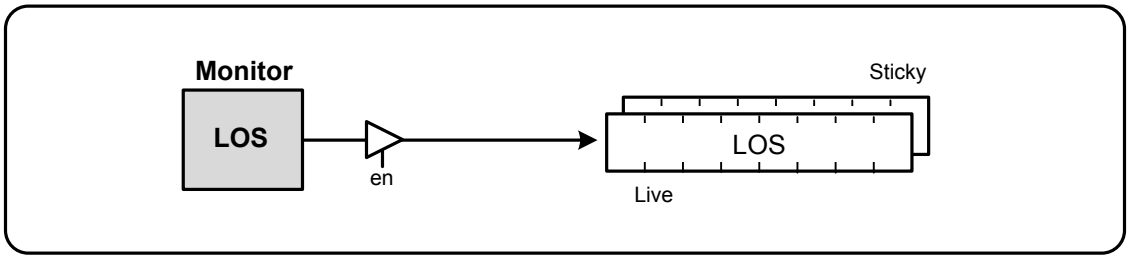


Figure 4.4. LOS Status Indicators

A LOS monitor is also available to ensure that the external crystal or reference clock is valid. By default the output clocks are disabled when LOSXAXB is detected. This feature can be disabled such that the device will continue to produce output clocks even when LOSXAXB is detected.

The table below lists the loss of signal status indicators and fault monitoring control registers.

Table 4.6. Loss of Signal Status Monitoring and Control Registers

Register Name	Hex Address [Bit Field]		Function
	Si5344H	Si5342H	
LOS	0x000D[1:0]	0x000D[1:0]	LOS status monitor for IN1(bit1), IN0 (bit0) indicates if a valid clock is detected. A set bit indicates the input is LOS.
SYSINCAL	0x000C[0]	0x000C[0]	Asserted when in calibration
LOSXAXB	0x000C[1]	0x000C[1]	LOS status monitor for the STAL or REFCLK at the XA/XB pins
LOS_FLG	0x0012[1:0]	0x0012[1:0]	LOS status monitor sticky bits for IN1, IN0. Sticky bits will remain asserted when a LOS event occurs until manually cleared. Writing zero to the bit will clear it.
SYSINCAL_FLG	0x0011[0]	0x0011[0]	SYSINCAL sticky bit. Sticky bits will remain asserted until written with a zero to clear.
LOSXAXB_FLG	0x0011[1]	0x0011[1]	LOS status monitor sticky bits for XAXB. Sticky bits will remain asserted when a LOS event occurs until cleared. Writing zero to the bit will clear it.
LOS_EN	0x002C[1:0]	0x002C[1:0]	LOS monitor enable for IN1, IN0. Allows disabling the monitor if unused.
LOS_TRIG_THR	0x002E[7:0]-0x0031[7:0]	0x002E[7:0]-0x0031[7:0]	Sets the LOS trigger threshold and clear sensitivity for IN1, IN0. These 16- bit values are determined by ClockBuilder Pro
LOS_CLR_THR	0x0036[7:0]-0x0039[7:0]	0x0036[7:0]-0x0039[7:0]	
LOS_VAL_TIME	0x002D[3:0]	0x002D[3:0]	LOS clear validation time for IN1, IN0. This sets the time that an input must have a valid clock before the LOS condition is cleared. Settings of 2ms, 100ms, 200ms, and 1 s are available.
LOS_INTR_MSK	0x0018[1:0]	0x0018[1:0]	This is the LOS interrupt mask, which can be cleared to trigger an interrupt on the INTR pin if an LOS occurs for IN1, IN0.

4.3.2 Out of Frequency (OOF) Fault Detection

Each input clock is monitored for frequency accuracy with respect to an OOF reference which it considers as its 0 ppm reference. This OOF reference can be selected as either:

- XA/XB pins
- Any input clock (IN0, IN1)

The final OOF status is determined by the combination of both a precise OOF monitor and a fast OOF monitor as shown in the figure below. An option to disable either monitor is also available. The live OOF register always displays the current OOF state and its sticky register bit stays asserted until cleared.

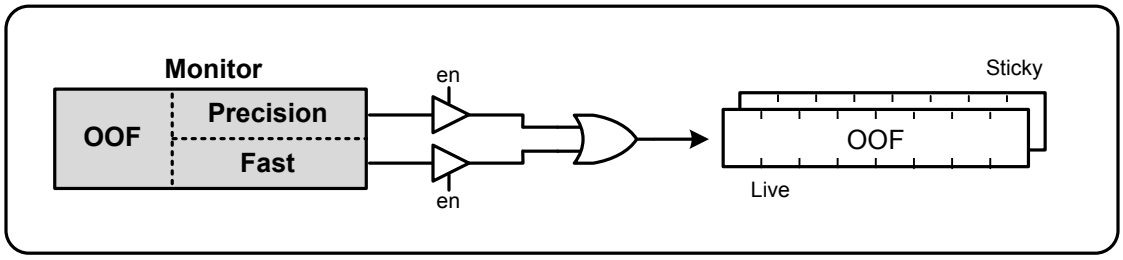


Figure 4.5. OOF Status Indicator

The precision OOF monitor circuit measures the frequency of all input clocks to within up to ±2 ppm accuracy with respect to the selected OOF frequency reference. A valid input clock frequency is one that remains within the register-programmable OOF frequency range of from ±2 ppm to ±500 ppm in steps of 2 ppm. A configurable amount of hysteresis is also available to prevent the OOF status from toggling at the failure boundary. An example is shown in the figure below. In this case, the OOF monitor is configured with a valid frequency range of ±6 ppm and with 2 ppm of hysteresis. An option to use one of the input pins (IN0–IN1) as the 0 ppm OOF reference instead of the XA/XB pins is available. This option is register configurable.

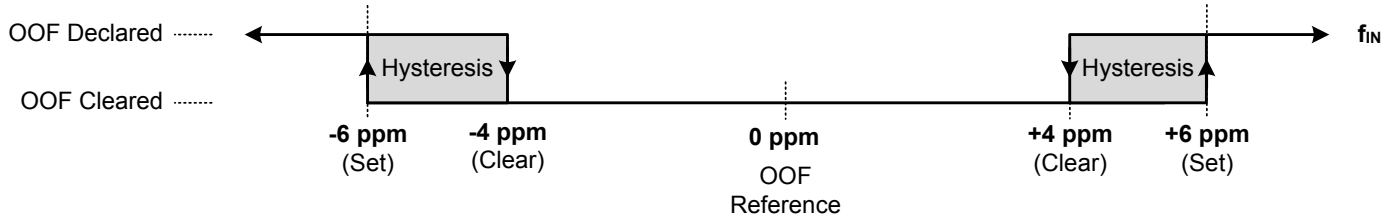


Figure 4.6. Example of Precise OOF Monitor Assertion and De-assertion Triggers

The table below lists the OOF monitoring and control registers. Because the precision OOF monitor needs to provide 1 ppm of frequency measurement accuracy, it must measure the monitored input clock frequencies over a relatively long period of time. This may be too slow to detect an input clock that is quickly ramping in frequency. An additional level of OOF monitoring called the Fast OOF monitor runs in parallel with the precision OOF monitors to quickly detect a ramping input frequency. The Fast OOF monitor asserts OOF on an input clock frequency that has changed by greater than ±4000 ppm.

Table 4.7. Out-of-Frequency Status Monitoring and Control Registers

Register Name	Hex Address [Bit Field]		Function
	Si5344H	Si5342H	
OOF	0x000D[5:4]	0x000D[5:4]	OOF status monitor for IN1, IN0. Indicates if a valid clock is detected or if a OOF condition is detected.
OOF_FLG	0x0012[5:4]	0x0012[5:4]	OOF status monitor sticky bits for IN1, IN0. Stick bits will remain asserted when an OOF event occurs until cleared. Writing zero to the bit will clear it.
OOF_REF_SEL	0x0040[2:0]	0x0040[2:0]	This selects the clock that the OOF monitors use as the 0 ppm reference. Selections are XA/XB, IN0, IN1. Default is XAXB.
OOF_EN	0x003F[1:0]	0x003F[1:0]	This allows to enable/disable the precision OOF monitor for IN1, IN0.
FAST_OOF_EN	0x003F[5:4]	0x003F[5:4]	This allows to enable/disable the fast OOF monitor for IN1, IN0.
OOF_SET_THR	0x0046[7:0]-0x0047[7:0]	0x0046[7:0]-0x0047[7:0]	Determines the OOF alarm set threshold for IN1, IN0. Range is from ±2 ppm to ±500 ppm in steps of 2 ppm.
OOF_CLR_THR	0x004A[7:0]-0x004B[7:0]	0x004A[7:0]-0x004B[7:0]	Determines the OOF alarm clear threshold for Inx. Range is from ±2 ppm to ±500 ppm in steps of 2 ppm.
FAST_OOF_SET_THR	0x0051[7:0]-0x0052[7:0]	0x0051[7:0]-0x0052[7:0]	Determines the fast OOF alarm set threshold for IN1, IN0.
FAST_OOF_CLR_THR	0x0055[7:0]-0x0056[7:0]	0x0055[7:0]-0x0056[7:0]	Determines the fast OOF alarm clear threshold for IN1, IN0.

4.3.3 Loss of Lock Fault Monitoring

The Loss of Lock (LOL) monitor asserts a LOL register bit when the DSPLL has lost synchronization with its selected input clock. There is also a dedicated loss of lock pin that reflects the loss of lock condition. The LOL monitor functions by measuring the frequency difference between the input and feedback clocks at the phase detector. There are two LOL frequency monitors, one that sets the LOL indicator (LOL Set) and another that clears the indicator (LOL Clear). An optional timer is available to delay clearing of the LOL indicator to allow additional time for the DSPLL to completely lock to the input clock. A block diagram of the LOL monitor is shown in the figure below. The live LOL register always displays the current LOL state and a sticky register always stays asserted until cleared. The LOL pin reflects the current state of the LOL monitor.

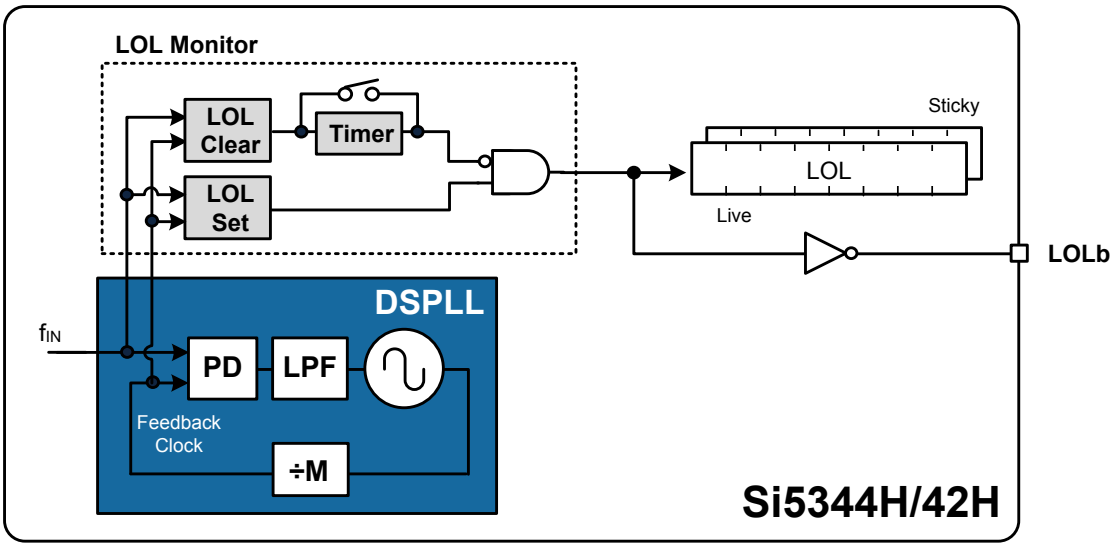


Figure 4.7. LOL Status Indicators

The LOL frequency monitors has an adjustable sensitivity which is register configurable from 0.2 ppm to 20000 ppm. Having two separate frequency monitors allows for hysteresis to help prevent chattering of LOL status. An example configuration where LOCK is indicated when there is less than 0.2 ppm frequency difference at the inputs of the phase detector and LOL is indicated when there's more than 2 ppm frequency difference is shown in the figure below.

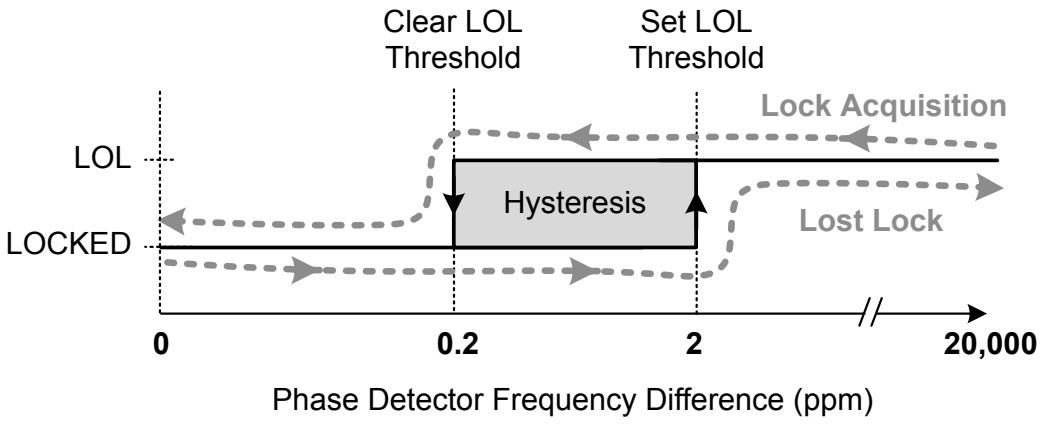


Figure 4.8. LOL Set and Clear Thresholds

Table 4.8. Loss of Lock Status Monitor and Control Registers

Register Name	Hex Address [Bit Field]		Function
	Si5344H	Si5342H	
LOL	0x000E[1]	0x000E[1]	Status bit that indicates if the DSPLL is locked to an input clock
LOL_FLG	0x0013[1]	0x0013[1]	Sticky bits for LOL register. Writing 0 to a sticky bit will clear it.
LOL_SET_THR	0x009E[7:4]	0x009E[7:4]	Configures the loss of lock set thresholds. Selectable as 0.2, 0.6, 2,6,20,60,200,600,2000,6000,20000. Values are in ppm. Default is 0.2ppm.
LOL_CLR_THR	0x00A0[7:4]	0x00A0[7:4]	Configures the loss of lock set thresholds. Selectable as 0.2, 0.6, 2,6,20,60,200,600,2000,6000,20000. Values are in ppm. Default is 2 ppm.
LOL_CLR_DELAY	0x00A8[7:0]-0x00AB[7:0]	0x00A8[7:0]-0x00AB[7:0]	This is a 35-bit register that configures the delay value for LOL Clear delay. Selectable from 0 ns to over 500 seconds.
LOL_TIMER_EN	0x00A2[1]	0x00A2[1]	Allows bypassing the LOL clear timer. 0-bypassed, 1-enabled.

The settings in the table above are handled by ClockBuilder Pro. Manual settings should be avoided.

4.4 Interrupt Configuration

There is an interrupt pin available on the device which is used to indicate a change in state of one or several of the status indicators. Any of the status indicators are maskable to prevent assertion of the interrupt pin. The state of the INTR pin is reset by clearing the status register that caused the interrupt. If an interrupt occurs the various status registers from the unmasked flags must be checked and then cleared.

Register Bit Locations

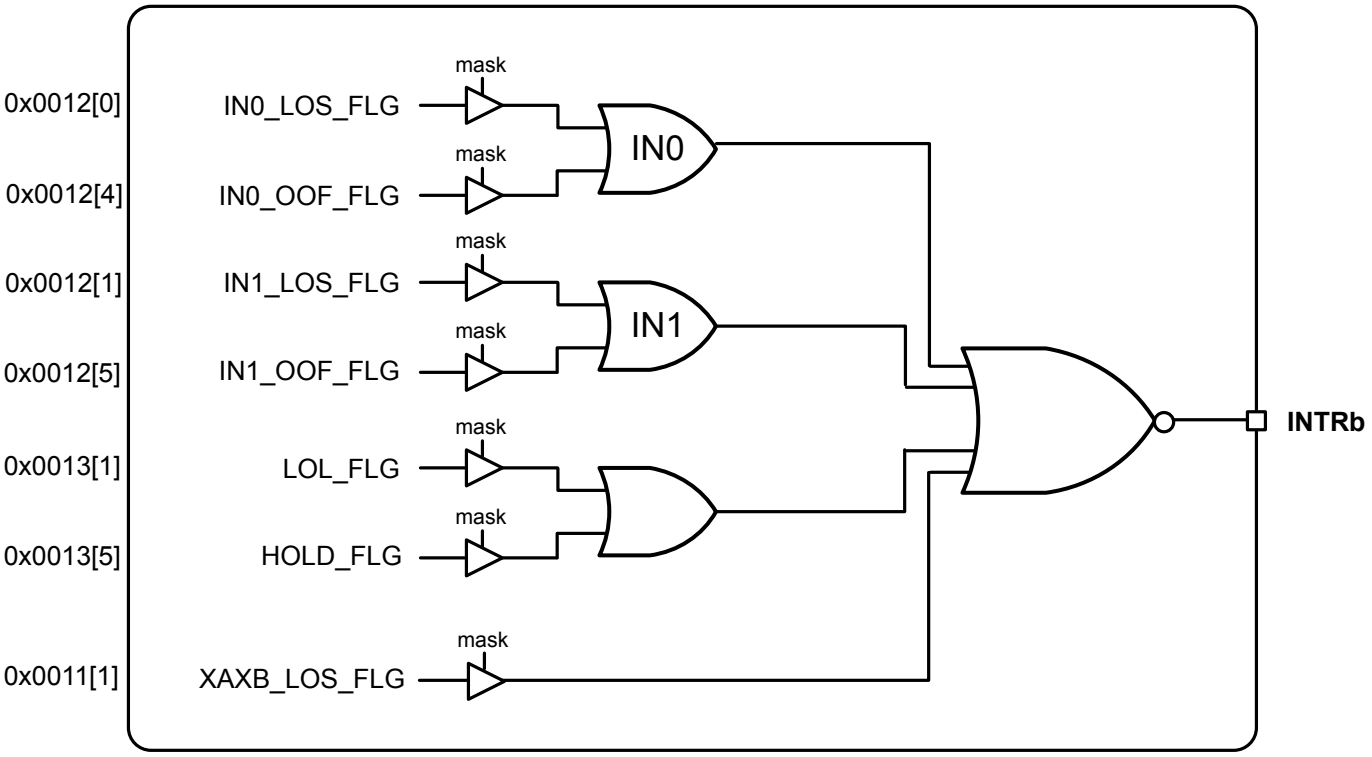


Figure 4.9. Interrupt Pin Status Flag Options

The _FLG bits are “sticky” versions of the alarm bits and will stay high until cleared. An _FLG bit can be cleared by writing a zero to the _FLG bit. When an _FLG bit is high and its corresponding alarm bit is low, the _FLG bit can be cleared.

During run time, the source of an interrupt can be determined by reading the _FLG register values and logically ANDing them with the corresponding _MSK register bits (after inverting the _MSK bit values). If the result is a logic one, then the _FLG bit will cause an interrupt.

For example, if LOS_FLG[0] is high and LOS_INTR_MSK[0] is low, then the INTR pin will be active (low) and cause an interrupt. If LOS[0] is zero and LOS_MSK[0] is one, writing a zero to LOS_MSK[0] will clear the interrupt (assuming that there are no other interrupt sources). If LOS[0] is high, then LOS_FLG[0] and the interrupt cannot be cleared.

5. Output Clocks

Each driver has a configurable voltage swing and common mode voltage covering a wide variety of differential signal formats including LVPECL, LVDS, HCSL, and CML. In addition to supporting differential signals, any of the outputs can be configured as single-ended LVCMOS (3.3, 2.5, or 1.8 V) providing up to 20 single-ended outputs or any combination of differential and single-ended outputs.

5.1 Output Crosspoint Switch

A crosspoint switch allows any of the output drivers to connect with any of the MultiSynths as shown in the figure below. The crosspoint configuration is programmable and can be stored in NVM so that the desired output configuration is ready at power up. Any MultiSynth output can connect to multiple output drivers.

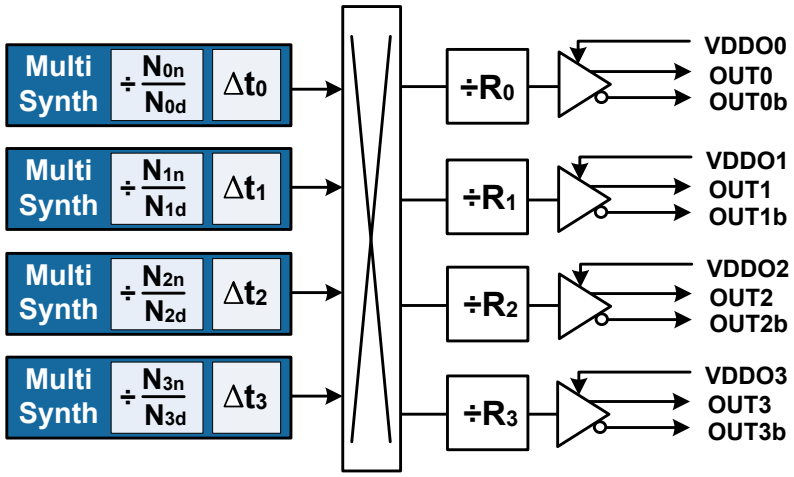


Figure 5.1. MultiSynth to Output Driver Crosspoint

The table below is used to set up the routing from the MultiSynth frequency selection to the output.

Table 5.1. Output Driver Crosspoint Configuration Registers

Register Name	Hex Address [Bit Field]		Function
	Si5344H	Si5342H	
OUT0_MUX_SEL	0x0115[2:0]	0x0115[2:0]	Connects the output drivers to one of the N dividers. Selections are N0, N1, N2, N3 for each output divider.
OUT1_MUX_SEL	0x011A[2:0]	0x011A[2:0]	
OUT2_MUX_SEL	0x0129[2:0]	—	
OUT3_MUX_SEL	0x012E[2:0]	—	

5.2 Performance Guidelines for Outputs

Whenever a number of high frequency, fast rise time, large amplitude signals are all close to one another, the laws of physics dictate that there will be some amount of crosstalk. The jitter of the Si5344H/42H is so low that crosstalk can become a significant portion of the final measured output jitter. Some of the source of the crosstalk will be the Si5344H/42H and some will be introduced by the PCB. It is difficult (and possibly irrelevant) to allocate the jitter portions between these two sources because the jitter can only be measured when a Si5344H/42H is mounted on a PCB.

For extra fine tuning and optimization in addition to following the usual PCB layout guidelines, crosstalk can be minimized by modifying the arrangements of different output clocks. For example, consider the following lineup of output clocks in Table 5.2 Example of Output Clock Frequency Sequencing Choice on page 29.

Table 5.2. Example of Output Clock Frequency Sequencing Choice

Output	Not Recommended (Frequency MHz)	Recommended (Frequency MHz)
0	155.52	155.52
1	156.25	155.52
2	155.52	622.08
3	156.25	Not used
4	200	156.25
5	100	156.25
6	622.08	625
7	625	Not used
8	Not used	200
9	Not used	100

Using this example, a few guidelines are illustrated:

Avoid adjacent frequency values that are close. A 155.52 MHz clock should not be next to a 156.25 MHz clock. If the jitter integration bandwidth goes up to 20 MHz then keep adjacent frequencies at least 20 MHz apart.

Adjacent frequency values that are integer multiples of one another are okay and these outputs should be grouped accordingly. Noting that because 155.52 × 4 = 622.08 and 156.25 × 4 = 625, it is okay to place these frequency values close to one another.

Unused outputs can be used to separate clock outputs that might otherwise interfere with one another. In this case, see OUT3 and OUT7.

If some outputs have tight jitter requirements while others are relatively loose, rearrange the clock outputs so that the critical outputs are the least susceptible to crosstalk. These guidelines typically only need to be followed by those applications that wish to achieve the highest possible levels of jitter performance. Because CMOS outputs have large pk-pk swings, are single ended, and do not present a balanced load to the VDDO supplies, CMOS outputs generate much more crosstalk than differential outputs. For this reason, CMOS outputs should be avoided whenever possible. When CMOS is unavoidable, even greater care must be taken with respect to the above guidelines. For more information on these issues, see *AN862: Optimizing Si534x Jitter Performance in Next Generation Internet Infrastructure Systems*.

5.3 Output Signal Format

The differential output swing and common mode voltage are both fully programmable covering a wide variety of signal formats including LVDS, LVPECL, HCSL. For CML applications, see 13. Appendix A—Setting the Differential Output Driver to Non-Standard Amplitudes. The differential formats can be either normal or low power. Low power format uses less power for the same amplitude but has the drawback of slower rise/fall times. The source impedance in low power format is much higher than 100 ohms. See Appendix A for register settings to implement variable amplitude differential outputs. In addition to supporting differential signals, any of the outputs can be configured as LVCMOS (3.3, 2.5, or 1.8 V) drivers providing up to 20 single-ended outputs, or any combination of differential and single-ended outputs. Note also that CMOS output can create much more crosstalk than differential outputs so extra care must be taken in their pin replacement so that other clocks that need the lowest jitter are not on nearby pins. See *AN862: Optimizing Si534x Jitter Performance in Next Generation Internet Infrastructure Systems* for additional information.

Table 5.3. Output Signal Format Control Registers

Register Name	Hex Address [Bit Field]		Function
	Si5344H	Si5342H	
OUT0_FORMAT	0x0113[2:0]	0x0113[2:0]	Selects the output signal format as differential or LVCMOS mode.
OUT1_ FORMAT	0x0118[2:0]	0x0118[2:0]	
OUT2_ FORMAT	0x0127[2:0]	—	
OUT3_ FORMAT	0x012C[2:0]	—	

5.3.1 Differential Output Terminations

The differential output drivers support both ac and dc-coupled terminations as shown in the figure below.

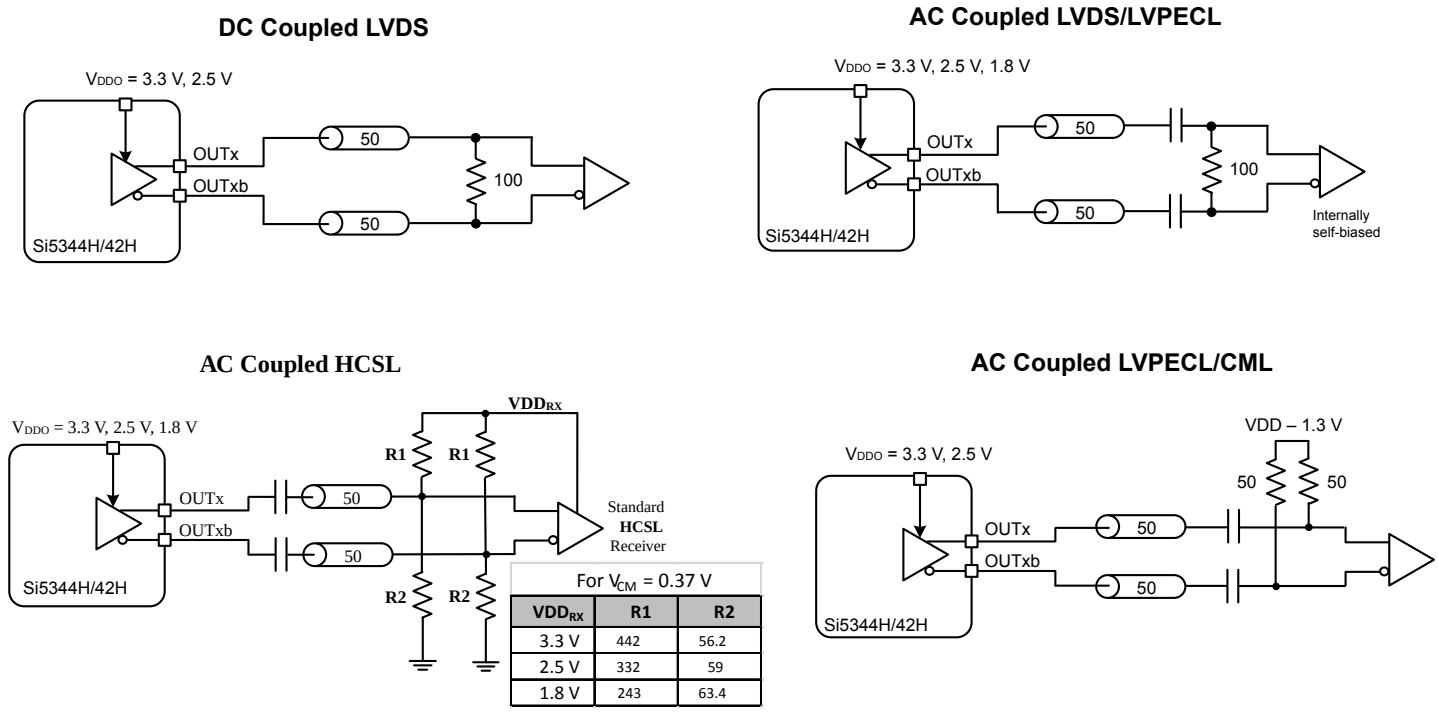


Figure 5.2. Supported Differential Output Terminations

5.3.2 Differential Output Swing Modes

There are two selectable differential output swing modes: Normal and High. Each output can support a unique mode.

- **Differential Normal Swing Mode**—This is the usual selection for differential outputs and should be used, unless there is a specific reason to do otherwise. When an output driver is configured in normal swing mode, its output swing is selectable as one of 7 settings ranging from 200 mVpp_se to 800 mVpp_se in increments of 100 mV. The table below lists the registers that control the output voltage swing. The output impedance in the Normal Swing Mode is 100 Ω differential. Any of the terminations shown in Figure 5.2 Supported Differential Output Terminations on page 30 are supported in this mode.
- **Differential High Swing Mode**—When an output driver is configured in high swing mode, its output swing is configurable as one of 7 settings ranging from 400 mVpp_se to 1600 mVpp_se in increments of 200 mV. The output driver is in high impedance mode and supports standard 50 Ω PCB traces. Any of the terminations shown in Figure 5.2 Supported Differential Output Terminations on page 30 are supported. The use of High Swing mode will result in larger pk-pk output swings that draw less power. The trade off will be slower rise and fall times.

Vpp_diff is 2 x Vpp_se, as shown in the figure below.

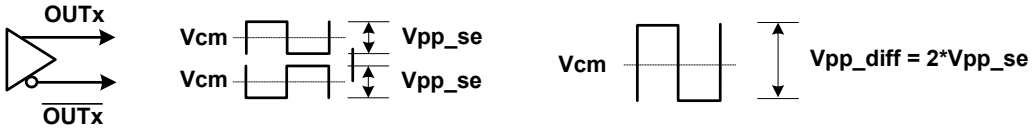


Figure 5.3. Vpp_se and Vpp_diff

Table 5.4. Differential Output Voltage Swing Control Registers

Register Name	Hex Address [Bit Field]		Function
	Si5344H	Si5342H	
OUT0_AMPL	0x0114[6:4]	0x0114[6:4]	Sets the voltage swing for the differential output drivers for both normal and high swing modes.
OUT1_ AMPL	0x0119[6:4]	0x0119[6:4]	
OUT2_ AMPL	0x0128[6:4]	—	
OUT3_ AMPL	0x012D[6:4]	—	

5.3.3 Programmable Common Mode Voltage for Differential Outputs

The common mode voltage (VCM) for the differential Normal and High Swing modes is programmable in 100 mV increments from 0.7 to 2.3 V depending on the voltage available at the output's VDDO pin. Setting the common mode voltage is useful when dc coupling the output drivers. High swing mode may also cause an increase in the rise/fall time.

Table 5.5. Differential Output Common Mode Voltage Control Registers

Register Name	Hex Address [Bit Field]		Function
	Si5344H	Si5342H	
OUT0_CM	0x0114[3:0]	0x0114[3:0]	Sets the common mode voltage for the differential output driver.
OUT1_ CM	0x0119[3:0]	0x0119[3:0]	
OUT2_ CM	0x0128[3:0]	—	
OUT3_ CM	0x012D[3:0]	—	

5.3.4 LVCMOS Output Terminations

LVCMOS outputs are dc-coupled, as shown in the figure below.

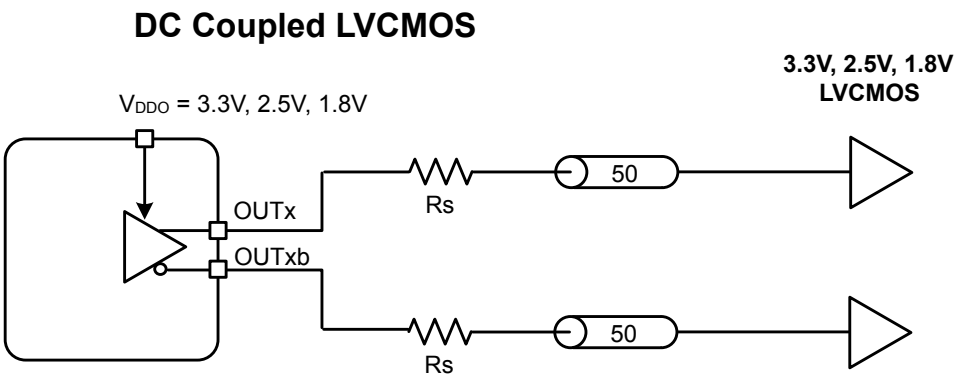


Figure 5.4. LVCMOS Output Terminations

5.3.5 LVCMOS Output Impedance and Drive Strength Selection

Each LVCMOS driver has a configurable output impedance to accommodate different trace impedances and drive strengths. A source termination resistor is recommended to help match the selected output impedance to the trace impedance. There are three programmable output impedance selections for each VDDO option, as shown in the table below. The value for the OUTx_CMOS_DRIVE bits are given.

Table 5.6. Output Impedance and Drive Strength Selections

VDDO	OUTx_CMOS_DRV	Source Impedance (Rs)	Drive Strength (Iol/Ioh)
3.3 V	0x01	38 Ω	10 mA
	0x02	30 Ω	12 mA
	0x03[1]	22 Ω	17 mA
2.5 V	0x01	43 Ω	6 mA
	0x02	35 Ω	8 mA
	0x03[1]	24 Ω	11 mA
1.8 V	0x03[1]	31 Ω	5 mA

Note:
1. Use of the lowest impedance setting is recommended for all supply voltages.

Table 5.7. LVCMOS Drive Strength Control Registers

Register Name	Hex Address [Bit Field]		Function
	Si5344H	Si5342H	
OUT0_CMOS_DRV	0x0113[7:6]	0x0113[7:6]	LVCMOS output impedance.
OUT1_ CMOS_DRV	0x0118[7:6]	0x0118[7:6]	
OUT2_ CMOS_DRV	0x0127[7:6]	—	
OUT3_ CMOS_DRV	0x012C[7:6]	—	

5.3.6 LVCMOS Output Signal Swing

The signal swing (V_{OL}/V_{OH}) of the LVCMOS output drivers is set by the voltage on the VDDO pins. Each output driver has its own VDDO pin allowing a unique output voltage swing for each of the LVCMOS drivers. Each output driver automatically detects the voltage on the VDDO pin to properly determine the correct output voltage.

5.3.7 LVCMOS Output Polarity

When a driver is configured as an LVCMOS output it generates a clock signal on both pins (OUTx and OUTxb). By default the clock on the OUTxb pin is generated with the same polarity (in phase) with the clock on the OUTx pin. The polarity of these clocks is configurable enabling complimentary clock generation and/or inverted polarity with respect to other output drivers.

Table 5.8. LVCMOS Output Polarity Control Registers

Register Name	Hex Address [Bit Field]		Function
	Si5344H	Si5342H	
OUT0_INV	0x0115[7:6]	0x0115 [7:6]	Controls the output polarity of the OUTx and OUTxb pins when in LVCMOS mode. Selections are listed in the table below.
OUT1_ INV	0x011A[7:6]	0x011A [7:6]	
OUT2_ INV	0x0129[7:6]	—	
OUT3_ INV	0x012E[7:6]	—	

Table 5.9. Output Polarity of OUTx and OUTxb Pins in LVCMOS Mode

OUTx_INV Register Settings	OUTx	OUTx	Comment
0x00	CLK	CLKb	Non-inverted
0x01	CLK	CLK	Both in phase (default)
0x02	CLKb	CLK	Inverted
0x03	CLKb	CLKb	Both out of phase

5.3.8 Output Driver Settings for LVPECL, LVDS, HCSL, and CML

Each differential output has four settings for control:

1. Normal or Low Power Format
2. Amplitude (sometimes called Swing)
3. Common Mode Voltage
4. Stop High or Stop Low

The normal Format setting has a 100 Ω internal resistor between the plus and minus output pins. The Low Power Format setting removes this 100 Ω internal resistor and then the differential output resistance will be
> 500 Ω. However as long as the termination impedance matches the differential impedance of the pcb traces the signal integrity across the termination impedance will be good. For the same output amplitude the Low Power Format will use less power than the Normal Format. The Low Power Format also has a lower rise/fall time than the Normal Format. See the Si5344H/42H data sheet for the rise/fall time specifications. For LVPECL and LVDS standards, ClockBuilder Pro does not support the Low Power Differential Format. Stop High means that when the output driver is disabled the plus output will be high and the minus output will be low. Stop Low means that when the output driver is disabled the plus output will be low and the minus output will be high.

The Format, Amplitude and Common Mode settings for the various supported standards are shown in the table below.

Table 5.10. Settings for LVDS, LVPECL, and HCSL

OUTx_FORMAT	Standard	VDDO Volts	OUTx_CM (Decimal)	OUTx_AMPL (Decimal)
001 = Normal Differential	LVPECL	3.3	11	6
001 = Normal Differential	LVPECL	2.5	11	6
002 = Low Power Differential	LVPECL	3.3	11	3
002 = Low Power Differential	LVPECL	2.5	11	3
001 = Normal Differential	LVDS	3.3	3	3
001 = Normal Differential	LVDS	2.5	11	3
001 = Normal Differential	Sub-LVDS[1]	1.8	13	3
002 = Low Power Differential	LVDS	3.3	3	1
002 = Low Power Differential	LVDS	2.5	11	1
002 = Low Power Differential	Sub-LVDS[1]	1.8	13	1
002 = Low Power Differential	HCSL[2]	3.3	11	3
002 = Low Power Differential	HCSL[2]	2.5	11	3
002 = Low Power Differential	HCSL[2]	1.8	13	3

Notes:

1. The common mode voltage produced is not compliant with LVDS standards, therefore AC coupling the driver to an LVDS receiver is highly recommended.
2. Creates HCSL compatible signal. See Figure 4.3 Si5344H/42H Fault Monitors on page 21.
3. The low-power format will cause the rise/fall time to increase by approximately a factor of two. See the Si5344H/42H data sheet for more information.

The output differential driver can produce a wide range of output amplitudes that includes CML amplitudes. See 13. Appendix A—Setting the Differential Output Driver to Non-Standard Amplitudes for additional information.

5.4 Output Enable/Disable

The OEb pin provides a convenient method of disabling or enabling the output drivers. When the OEb pin is held high all outputs will be disabled. When the pin is not driven, the device defaults to all outputs on. Outputs in the enabled state can be individually disabled through register control. If the pin is high register control is disabled and all outputs will be disabled.

Table 5.11. Output Enable/Disable Control Registers

Register Name	Hex Address [Bit Field]		Function
	Si5344H	Si5342H	
OUTALL_ DISABLE_LOW	0x0102[0]	0x0102[0]	Disables all output drivers: 0 – all outputs disabled, 1 – all outputs enabled. This bit essentially has the same function as the OEb pin if the OEb pin is held low. If the OEb pin is held high, then all outputs will be disabled regardless of the state of this register bit.
OUT0_OE	0x0112[1]	0x0112[1]	Allows enabling/disabling individual output drivers. Note that the OEb pin must be held low in order to enable an output.
OUT1_ OE	0x0117[1]	0x0117[1]	
OUT2_ OE	0x0126[1]	—	
OUT3_ OE	0x012B[1]	—	

5.4.1 Output Driver State When Disabled

The disabled state of an output driver is configurable as: disable low, disable high, or disable high-impedance.

Table 5.12. Output Driver State Control Registers

Register Name	Hex Address [Bit Field]		Function
	Si5344H	Si5342H	
OUT0_DIS_STATE	0x0113[5:4]	0x0113[5:4]	Determines the state of an output driver when disabled. Selectable as: Disable logic low Disable logic high Disable high-impedance Note that in high-impedance mode the differential driver will output the common mode voltage and no signal. The default disabled state is high-impedance.
OUT1_ DIS_STATE	0x0118[5:4]	0x0118[5:4]	
OUT2_ DIS_STATE	0x0127[5:4]	—	
OUT3_ DIS_STATE	0x012C[5:4]	—	

5.4.2 Synchronous Output Disable Feature

The output drivers provide a selectable synchronous disable feature. Output drivers with this feature turned on will wait until a clock period has completed before the driver is disabled. This prevents unwanted runt pulses from occurring when disabling an output. When this feature is turned off, the output clock will disable immediately without waiting for the period to complete. The default state is for the synchronous output to be disabled.

Table 5.13. Synchronous Disable Control Registers

Register Name	Hex Address [Bit Field]		Function
	Si5344H	Si5342H	
OUT0_SYNC_EN	0x0113[3]	0x0113[3]	Synchronous output disable. When this feature is enabled, the output clock will always finish a complete period before disabling. When this feature is disabled, the output clock will disable immediately without waiting for the period to complete. This feature is disabled by default.
OUT1_ SYNC_EN	0x0118[3]	0x0118[3]	
OUT2_ SYNC_EN	0x0127[3]	—	
OUT3_ SYNC_EN	0x012C[3]	—	

5.5 Output Skew Control (t0–t3)

The Si5344H/42H uses independent MultiSynth dividers (N0–N3) to generate up to four unique frequencies to its ten outputs through a crosspoint switch. By default all clocks are phase aligned. A delay path (t0–t3) associated with each of these dividers is available for applications that need a specific output skew configuration. This is useful for PCB trace length mismatch compensation or for applications that require quadrature clock generation. The resolution of the phase adjustment is approximately 1 ps per step definable in a range of ±8.32 ns. Phase adjustments are register configurable. An example of generating two frequencies with unique configurable path delays is shown in the figure below.

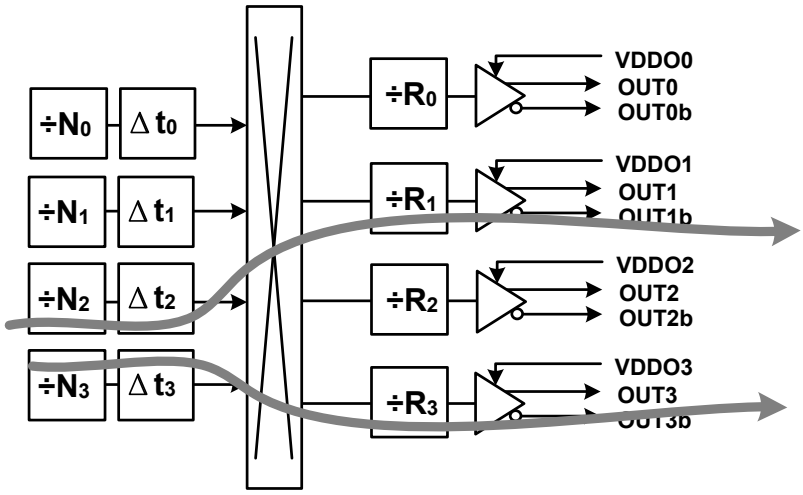


Figure 5.5. Example of Independently-Configurable Path Delays

All phase delay values are restored to their default values after power-up, hard reset, or a reset using the RST pin. Phase delay default values can be written to NVM allowing a custom phase offset configuration at power-up or after power-on reset, or after a hardware reset using the RST pin.

Table 5.14. Output Delay Registers

Register Name	Hex Address [Bit Field]		Function
	Si5344H	Si5342H	
N0_DELAY	0x0359[7:0]-0x035A[7:0]	0x0359[7:0]-0x035A[7:0]	Configures path delay values for each N divider. Each 16 bit number is 2s complement. The output delay is Nx_DELAY/(256 x Fvco) where Fvco is the frequency of the VCO in Hz and the delay is in seconds. Register values determined using ClockBuilder Pro.
N1_DELAY	0x035B [7:0]-0x035C[7:0]	0x035B [7:0]-0x035C[7:0]	
N2_DELAY	0x035D[7:0]-0x035E[7:0]	—	
N3_DELAY	0x035F[7:0]-0x0360[7:0]	—	

6. Digitally-Controlled Oscillator (DCO) Mode

The Si5344H/Si5342H supports DCO mode. In DCO mode, all outputs are controlled simultaneously. The DCO mode can be set up using the ClockBuilder Pro setup wizard.

Alternatively, DCO mode can be setup using the steps described in this section. The equations and register writes in Section 6.1 DCO Register Writes allow for modulation of outputs with three register writes—two divide value registers and one register write to update frequency. Two byte divide values allow a DCO mode range of ±150 ppm and approximately 10 ppb resolution per bit. DCO update rate is primarily limited by the SPI bus speed. Given a sufficient SPI bus rate, DCO update rate of 200 kHz or higher can be achieved.

In jitter attenuation mode, the device operates in dual-loop mode—the inner loop referenced to a crystal or XO tied to XA/XB pins and outer loop referenced to INx. In DCO mode, there is no INx input, and so the outer loop is disabled. The PLL inner loop feedback divider (M_{XAXB}) can be externally controlled to produce the desired instantaneous output frequency. Fixing the M_{XAXB} denominator and modulating only the numerator produces a linear frequency change across the full DCO range.

6.1 DCO Register Writes

To configure the device in DCO mode, you must first generate a ClockBuilder Pro configuration with nominal output frequencies.

Once the ClockBuilder Pro configuration is written to the device, the following DCO initial values must be written to the device to instantiate DCO mode.

1. Write OUTERLOOP_DIS = 1
2. Write MXAXB_NUM[43:0] = 0x000005F58000 = 99,975,168dec
3. Write MXAXB_DEN[31:0] = ROUND {99,975,168 * $F_{XTAL}/(F_{VCO})$}
4. Write MXAXB_FUPD = 1

Note: F_{VCO} is listed in the ClockBuilder Pro Frequency Plan Result Design Report.

Once instantiated, MXAXB_NUM[15:0] can be incremented or decremented in 10 ppb steps per LSB (1 / 99,975,168 per LSB). For example, to change the outputs by –1 ppm, 100 steps, write MXAXB_NUM[15:0] = 0x7F9C.

6.1.1 Other DCO Step Sizes

The previous example describes a DCO setup with 10 ppb steps. Other step sizes can be achieved by replacing MXAXB_NUM and MXAXB_DEN values with below.

As in the previous example, write the initial ClockBuilder Pro configuration into the device followed by the setup registers below to instantiate DCO mode.

1. Write OUTERLOOP_DIS = 1
2. Write MXAXB_NUM[43:0]
   a. For resolution RES set MXAXB_NUM to 1/RES rounded to the nearest 15 bits. For example, for 1.6 ppb resolution round 1/1.6E–9 to nearest 15 bits to get 624,984,064dec, or MXAXB_NUM = 0x25408000.
3. Write MXAXB_DEN[31:0] = ROUND {MXAXB_NUM * $F_{XTAL}/(F_{VCO})$}
4. Write MXAXB_FUPD = 1

Note: F_{VCO} is listed in the ClockBuilder Pro Frequency Plan Result Design Report.

As before, MXAXB_NUM[15:0] can be incremented or decremented with resolution RES per LSB.

6.2 DCO Register Descriptions

Below are descriptions of registers related to the DCO. All other register settings are generated from ClockBuilder Pro.

Table 6.1. 0x0235-0x023A – MXAXB_NUM

Reg Address	Bit Field	Type	Name	Description
0x0235	7:0	R/W	MXAXB_NUM	44-bit Integer Number Numerator portion of MXAXB Divider.
0x0236	15:8	R/W	MXAXB_NUM	
0x0237	23:16	R/W	MXAXB_NUM	
0x0238	31:24	R/W	MXAXB_NUM	
0x0239	39:32	R/W	MXAXB_NUM	
0x023A	43:40	R/W	MXAXB_NUM	

Table 6.2. 0x023B-0x023E – MXAXB_DEN

Reg Address	Bit Field	Type	Name	Description
0x023B	7:0	R/W	MXAXB_DEN	32-bit Integer Number Denominator portion of MXAXB Divider.
0x023C	15:8	R/W	MXAXB_DEN	
0x023D	23:16	R/W	MXAXB_DEN	
0x023E	31:24	R/W	MXAXB_DEN	

Table 6.3. 0x023F – MXAXB_FUPD

Reg Address	Bit Field	Type	Name	Description
0x023F	0	R/W	MXAXB_FUPD	Self-clearing bit Writing 1 to this bit applies values in MXAXB_NUM and MXAXB_DEN registers to the MXAXB Divider.
0x023F	7:1	—		Reserved. Write 0000000b.

Table 6.4. 0x0540 – OUTERLOOP_DIS

Reg Address	Bit Field	Type	Name	Description
0x0540	0	R/W	OUTERLOOP_DIS	0: Outer loop enabled (Jitter Attenuation Mode) 1: Outer loop disabled (DCO Mode)
0x0540	7:1	—		Reserved. Write 0000000b.

7. Serial Interface

Configuration and operation of the Si5344H/42H is controlled by reading and writing registers using the I²C or SPI interface. Both of these serial interfaces are based on 8-bit addressing, which means that the page byte must be written every time you need to access a different page in the register map. See the PAGE byte at register 0x0001 for more information. The I2C_SEL pin selects I²C or SPI operation. The Si5344H/42H supports communication with a 3.3 or 1.8 V host by setting the IO_VDD_SEL (0x0943[0]) configuration bit. The SPI mode supports 4-wire or 3-wire by setting the SPI_3WIRE configuration bit.

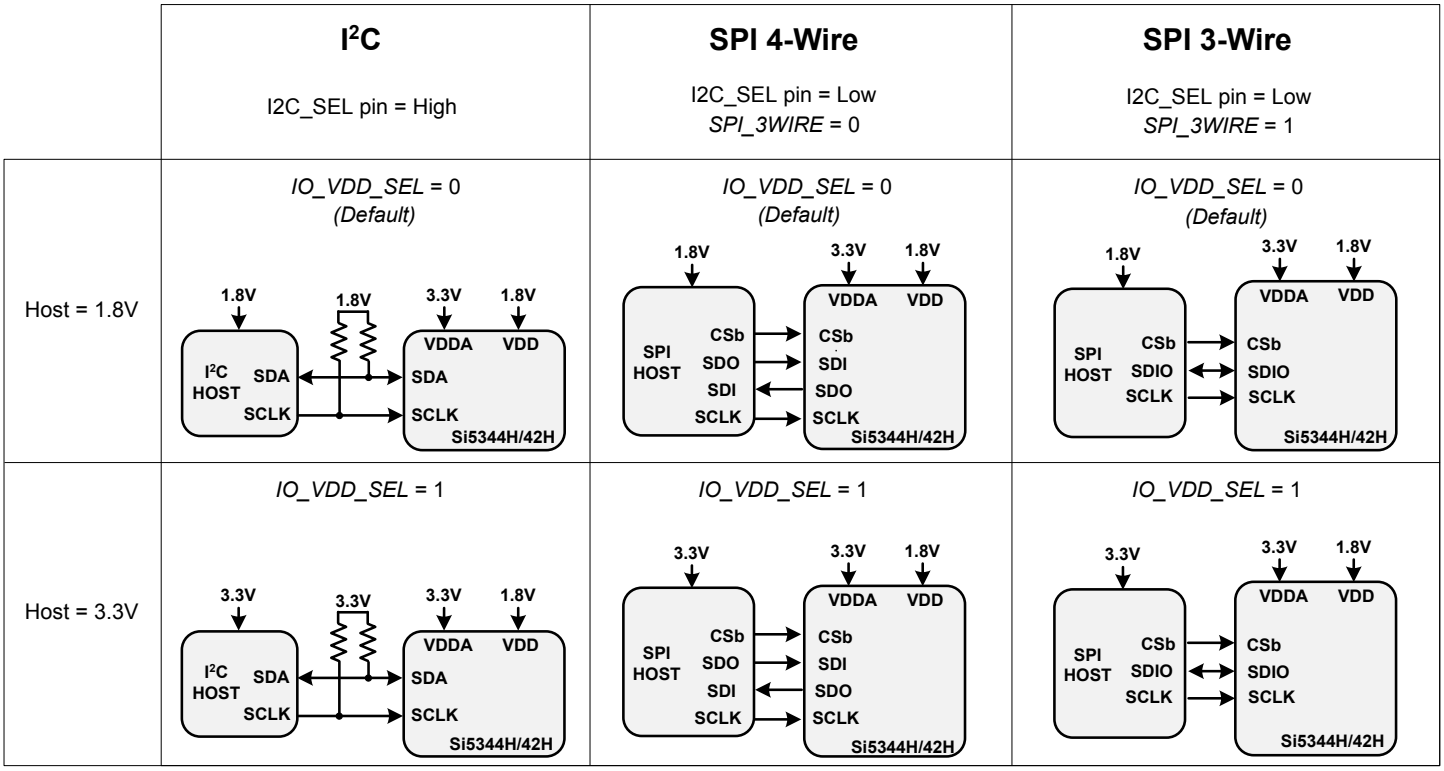


Figure 7.1. I²C/SPI Device Connectivity Configurations

The table below lists register settings of interest for the I²C/SPI.

Table 7.1. I²C/SPI Register Settings

Register Name	Hex Address [Bit Field]		Function
	Si5344H	Si5342H	
IO_VDD_SEL	0x0943[0]	0x0943[0]	The IO_VDD_SEL bit determines whether the VDD or VDDA supply voltage is used for the serial port, control pins, and status pins voltage references. See the register map description of this bit for additional details.
SPI_3WIRE	0x002B[3]	0x002B[3]	The SPI_3WIRE configuration bit selects the option of 4-wire or 3-wire SPI communication. By default, the SPI_3WIRE configuration bit is set to the 4-wire option. In this mode, the Si5344H/42H will accept write commands from a 4-wire or 3- wire SPI host allowing configuration of device registers. For full bidirectional communication in 3-wire mode, the host must write the SPI_3WIRE configuration bit to “1”.

If neither serial interface is used, leave pins I2C_SEL, A1/SDO, and A0/CS disconnected, and tie SDA/SDIO and SCLK low.

7.1 I²C Interface

When in I²C mode, the serial interface operates in slave mode with 7-bit addressing and can operate in Standard-Mode (100 kbps) or Fast-Mode (400 kbps) and supports burst data transfer with auto address increments. The I²C bus consists of a bidirectional serial data line (SDA) and a serial clock input (SCL) as shown in Figure 7.4 I²C Write Operation on page 41. Both the SDA and SCL pins must be connected to a supply via an external pull-up (4.7 kΩ) as recommended by the I²C specification as shown in Figure 7.2 I²C Configuration on page 41. Two address select bits (A0, A1) are provided allowing up to four Si5344H/42H devices to communicate on the same bus. This also allows four choices in the I²C address for systems that may have other overlapping addresses for other I²C devices.

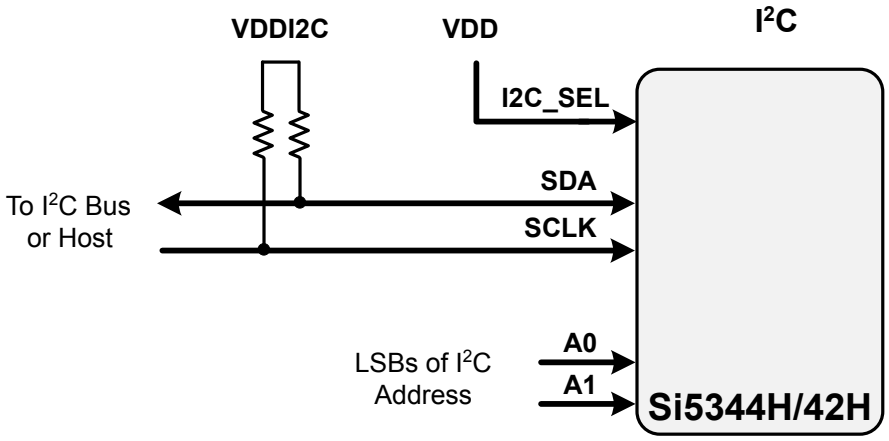


Figure 7.2. I²C Configuration

The 7-bit slave device address of the Si5344H/42H consists of a 5-bit fixed address plus 2 pins which are selectable for the last two bits, as shown in Figure 7.3 7-bit I²C Slave Address Bit-Configuration on page 41.

	6	5	4	3	2	1	0
Slave Address	1	1	0	1	0	A1	A0

Figure 7.3. 7-bit I²C Slave Address Bit-Configuration

Data is transferred MSB first in 8-bit words as specified by the I²C specification. A write command consists of a 7-bit device (slave) address + a write bit, an 8-bit register address, and 8 bits of data as shown in Figure 7.4 I²C Write Operation on page 41. A write burst operation is also shown where subsequent data words are written using to an auto-incremented address.

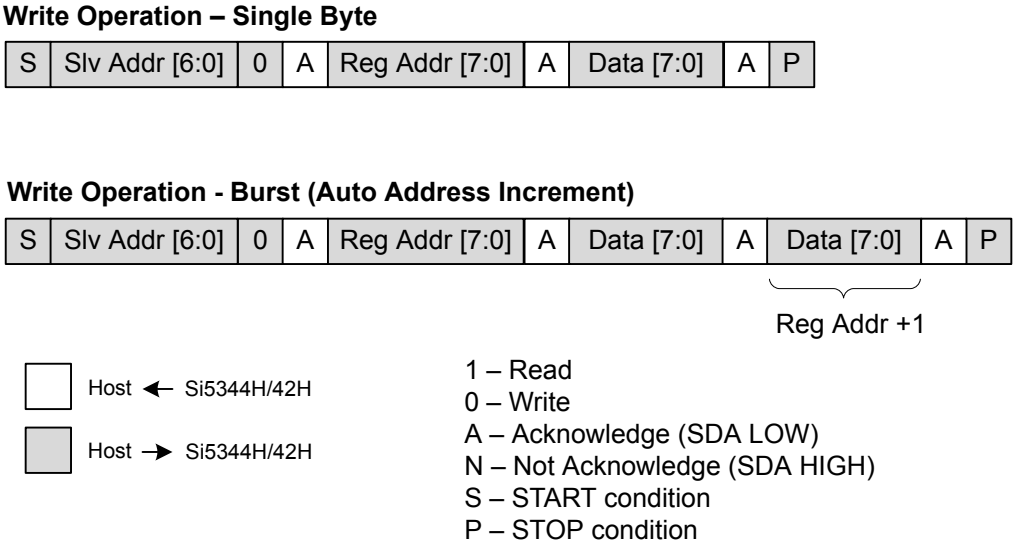


Figure 7.4. I²C Write Operation

A read operation is performed in two stages. A data write is used to set the register address, then a data read is performed to retrieve the data from the set address. A read burst operation is also supported. This is shown in the figure below.

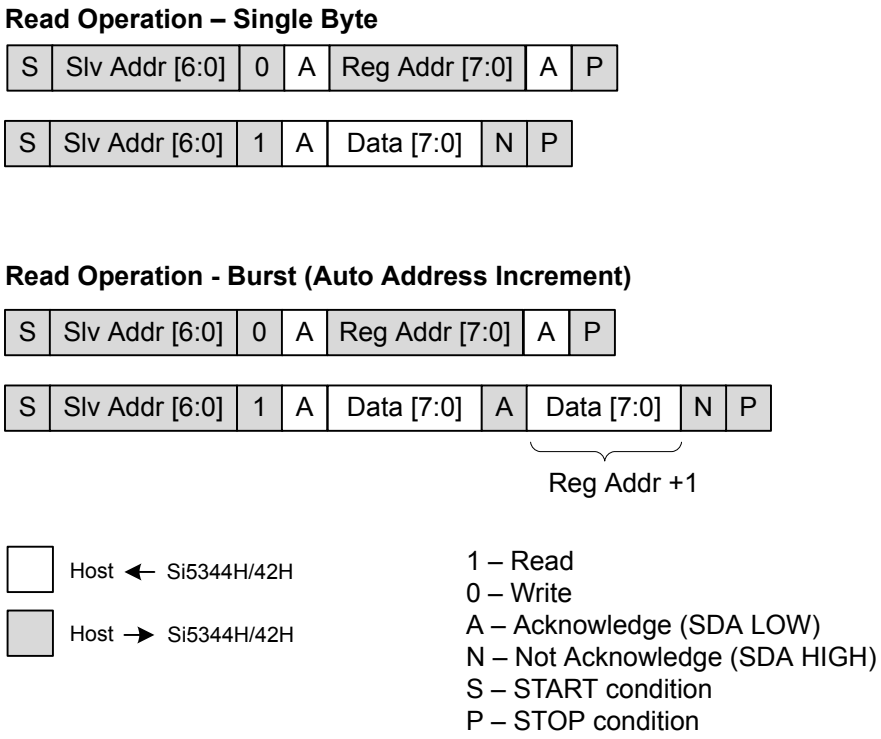


Figure 7.5. I²C Read Operation

The I²C bus supports SDA timeout for compatibility with the SMBus interfaces. The error flags are found in the registers listed in the table below.

Table 7.2. SMBus Timeout Error Bit Indicators

Register Name	Hex Address [Bit Field]		Function
	Si5344H	Si5342H	
SMBUS_TIMEOUT	0x000C[5]	0x000C[5]	1 if there is a SMBus timeout error. Contact Silicon Labs.
SMBUS_TIMEOUT_FLG	0x0011[5]	0x0011[5]	1 if there is a SMBus timeout error. Contact Silicon Labs.

7.2 SPI Interface

When in SPI mode, the serial interface operates in 4-wire or 3-wire depending on the state of the SPI_3WIRE configuration bit. The 4-wire interface consists of a clock input (SCLK), a chip select input (CS), serial data input (SDI), and serial data output (SDO). The 3-wire interface combines the SDI and SDO signals into a single bidirectional data pin (SDIO). Both 4-wire and 3-wire interface connections are shown in the figure below.

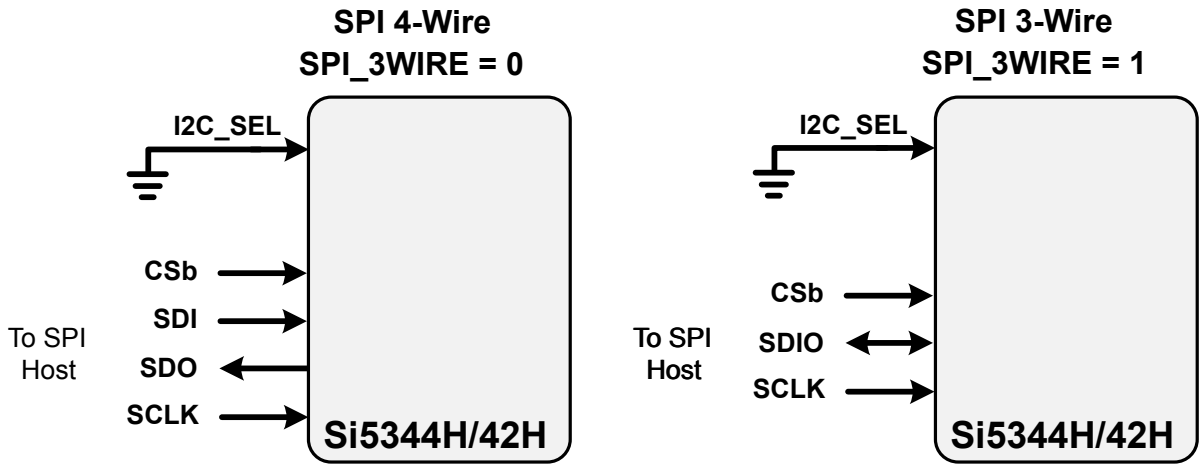


Figure 7.6. SPI Interface Connections

Table 7.3. SPI Command Format

Instruction	Ist Byte[1]	2nd Byte	3rd Byte	Nth Byte[2,3]
Set Address	000x xxxx	8-bit Address	—	—
Write Data	010x xxxx	8-bit Data	—	—
Read Data	100x xxxx	8-bit Data	—	—
Write Data + Address Increment	011x xxxx	8-bit Data	—	—
Read Data + Address Increment	101x xxxx	8-bit Data	—	—
Burst Write Data	1110 0000	8-bit Address	8-bit Data	8-bit Data

Notes:

1. X = don't care (1 or 0)
2. The Burst Write Command is terminated by de-asserting CSb (CSb = high)
3. There is no limit to the number of data bytes that follow the Burst Write Command, but the address will wrap around to zero in the byte after address 255 is written.

Writing or reading data consist of sending a "Set Address" command followed by a "Write Data" or "Read Data" command. The 'Write Data + Address Increment' or "Read Data + Address Increment" commands are available for cases where multiple byte operations in sequential address locations is necessary. The "Burst Write Data" instruction provides a compact command format for writing data since it uses a single instruction to define starting address and subsequent data bytes. Figure 7.7 Example Writing Three Data Bytes Using the Write Commands on page 44 shows an example of writing three bytes of data using the write commands. This demonstrates that the "Write Burst Data" command is the most efficient method for writing data to sequential address locations. Figure 7.8 Example of Reading Three Data Bytes Using the Read Commands on page 44 provides a similar comparison for reading data with the read commands. Note that there is no burst read, only read increment.

‘Set Address’ and ‘Write Data’

‘Set Addr’	Addr [7:0]	‘Write Data’	Data [7:0]
‘Set Addr’	Addr [7:0]	‘Write Data’	Data [7:0]
‘Set Addr’	Addr [7:0]	‘Write Data’	Data [7:0]

‘Set Address’ and ‘Write Data + Address Increment’

‘Set Addr’	Addr [7:0]	‘Write Data + Addr Inc’	Data [7:0]
‘Write Data + Addr Inc’	Data [7:0]		
‘Write Data + Addr Inc’	Data [7:0]		

‘Burst Write Data’

‘Burst Write Data’	Addr [7:0]	Data [7:0]	Data [7:0]	Data [7:0]

Figure 7.7. Example Writing Three Data Bytes Using the Write Commands

‘Set Address’ and ‘Read Data’

‘Set Addr’	Addr [7:0]	‘Read Data’	Data [7:0]
‘Set Addr’	Addr [7:0]	‘Read Data’	Data [7:0]
‘Set Addr’	Addr [7:0]	‘Read Data’	Data [7:0]

‘Set Address’ and ‘Read Data + Address Increment’

‘Set Addr’	Addr [7:0]	‘Read Data + Addr Inc’	Data [7:0]
‘Read Data + Addr Inc’	Data [7:0]		
‘Read Data + Addr Inc’	Data [7:0]		

Figure 7.8. Example of Reading Three Data Bytes Using the Read Commands

8. Field Programming

To simplify design and software development of systems using the Si5344H/42H, a field programmer is available. The ClockBuilder Pro Field Programmer supports both “in-system” programming (for devices already mounted on a PCB), as well as “in-socket” programming of Si5344H/42H sample devices. Refer to http://www.silabs.com/CBProgrammer for information about this kit.

9. XAXB External References

9.1 Performance of External References

An external standard non-pullable crystal (XTAL) is used in combination with the internal oscillator (OSC) to produce an ultra low jitter reference clock for the DSPLL and for providing a stable reference for the free-run and holdover modes. A simplified diagram is shown in Figure 9.1 Crystal Resonator and External Reference Clock Connection Options on page 46. The device includes internal XTAL loading capacitors which eliminates the need for external capacitors and also has the benefit of reduced noise coupling from external sources. Although the device includes built-in XTAL load capacitors (CL) of 8 pF, crystals with load capacitances up to 18 pF can also be accommodated. Frequency offsets due to CL mismatch can be adjusted using the frequency adjustment feature which allows frequency adjustments of ±200 ppm. The recommended crystal suppliers is provided in Table 9.1 XAXB Frequency Offset Register on page 47 with PCB layout recommendations for the crystal to ensure optimum jitter performance.

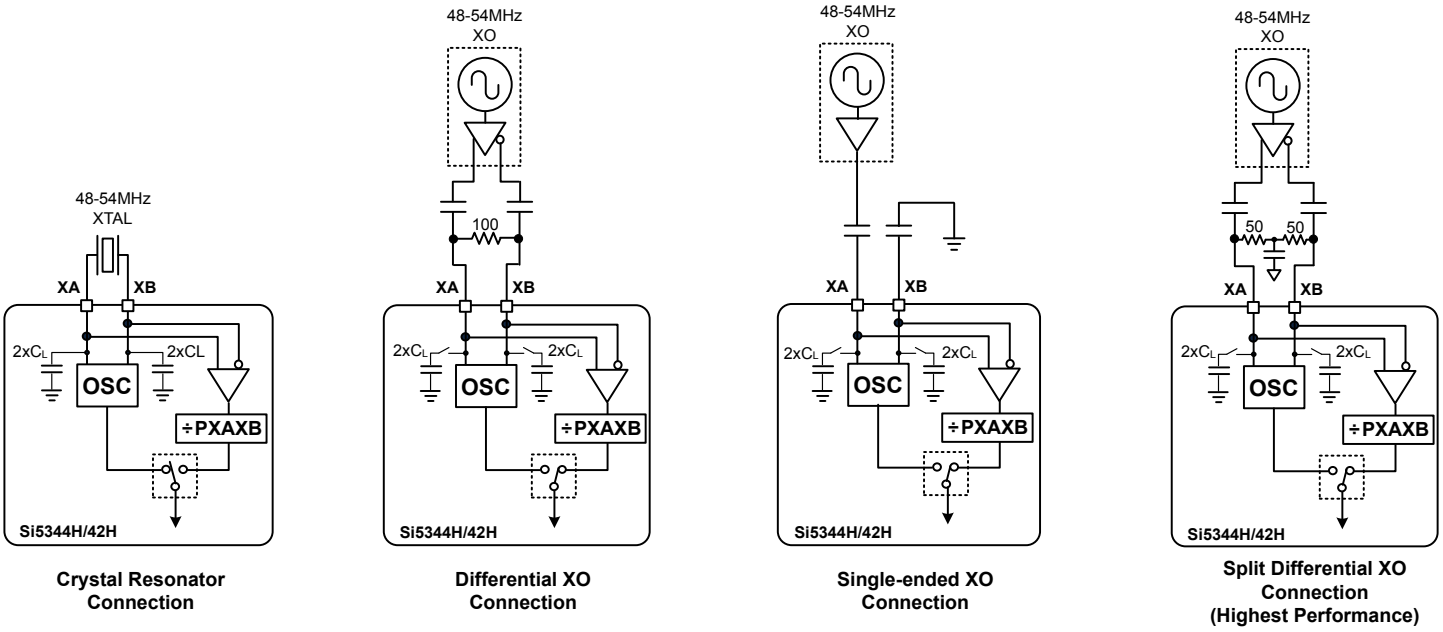


Figure 9.1. Crystal Resonator and External Reference Clock Connection Options

The Si5344H/42H accepts a clipped sine wave, CMOS, or differential reference clock on the XA/XB interface. Most clipped sine wave and CMOS TCXOs have insufficient drive strength to drive a 100 Ω or 50 Ω load. For this reason, place the TCXO as close to the Si5344H/42H as possible to minimize PCB trace length. In addition, ensure that both the Si5344H/42H and the TCXO are both connected directly to the ground plane. Figure 9.2 Clipped Sine Wave TCXO Output on page 47 shows the recommended method of connecting a clipped sine wave TCXO to the Si5344H/42H. Because the Si5344H/42H provides dc bias at the XA and XB pins, the ~800 mV peak-peak swing can be input directly into the XA interface of the Si5344H/42H once it has been ac-coupled. Because the signal is single-ended, the XB input is ac-coupled to ground. Note that when using a single-ended XO, the XO signal must be driven on XA. If XA is not driven, the device will report an LOSXAXB alarm. Figure 9.3 CMOS TCXO Output on page 47 illustrates the recommended method of connecting a CMOS rail-to-rail output to the XA/XB inputs of the Si5344H/42H. The resistor network attenuates the rail-to-rail output swing to ensure that the maximum input voltage swing at the XA pin is less than 1.6 V pk-pk. The signal is ac-coupled before connecting it to the Si5344H/42H XA input.

If an external oscillator is used as the XAXB reference, it is important to use a low jitter source because there is essentially no jitter attenuation from the XAXB pins to the outputs.

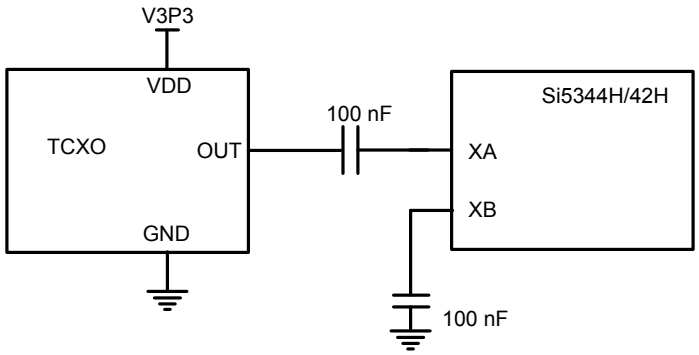


Figure 9.2. Clipped Sine Wave TCXO Output

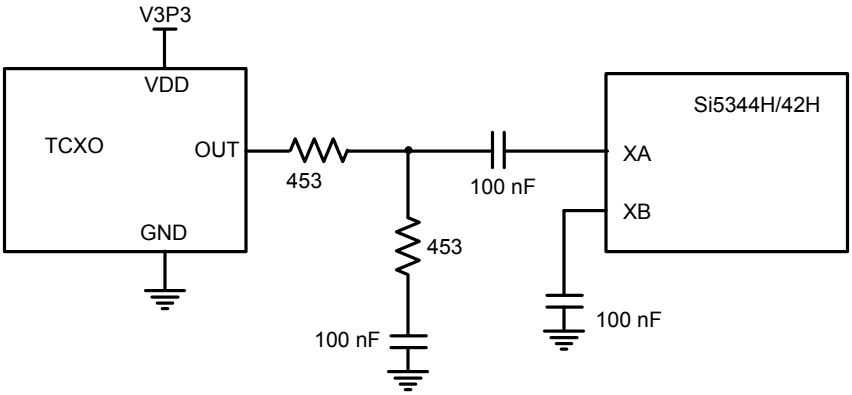


Figure 9.3. CMOS TCXO Output

The Si5344H/42H can also accommodate an external reference clock (REFCLK) instead of a crystal. Selection between the external XTAL or REFCLK is controlled by XAXB_EXTCLK_EN, the LSB of register 0x090E. The internal crystal loading capacitors (CL) are disabled when an external clock source is selected. A PXAXB prescale divider is available to accommodate external clock frequencies higher than 125 MHz as shown in Table 9.1 XAXB Frequency Offset Register on page 47. For best jitter performance, keep the REFCLK frequency above 40 MHz.

For applications with loop BW values less than 10 Hz that require low wander output clocks, using a TCXO as the XAXB reference source should be considered to avoid the wander of a crystal.

9.2 Recommended Crystals and External Oscillators

Please refer to the *Si534x/8x Jitter Attenuators Recommended Crystal, TCXO and OCXOs Reference Manual* for more information.

9.3 Register Settings to Control External XTAL Reference

The following registers can be used to control and make adjustments for the external reference source used.

9.3.1 XAXB_FREQ_OFFSET Frequency Offset Register

Table 9.1. XAXB Frequency Offset Register

Register Name	Hex Address [Bit Field]		Function
	Si5344H	Si5342H	
XAXB_FREQ_OFFSET	0202[7:0]-0205[7:0]	0202[7:0]-0205[7:0]	32-bit number which allows adjustment to the center frequency of the XTAL in the range of ±1000 ppm.

The VCO locks to the XO that is formed by the crystal or XO and the XAXB pins. XAXB_FREQ_OFFSET provides a static frequency offset to the VCO frequency. It is a 32-bit 2's complement number. This register can be used to adjust the frequency of the VCO when it is locked to the XAXB frequency. The Default value is 0.

9.3.2 XAXB_EXTCLK_EN Reference Clock Selection Register

Table 9.2. XAXB External Clock Selection Register

Register Name	Hex Address [Bit Field]		Function
	Si5344H	Si5342H	
XAXB_EXTCLK_EN	090E[0]	090E[0]	This bit selects between the XTAL or external REFCLK on the XA/XB pins. The default is XTAL = 0

This bit selects between XTAL or external REFCLK on the XA/XB pins. Set this bit to use the external REFCLK.

9.3.3 PXAXB Pre-scale Divide Ratio for Reference Clock Register

Table 9.3. Pre-Scale Divide Ratio Register

Register Name	Hex Address [Bit Field]		Function
	Si5344H	Si5342H	
PXAXB	0206[1:0]	0206[1:0]	This is a two bit value that sets the divider value.

The table below lists the input values for the two-bit field and the corresponding divider values.

Table 9.4. Pre-Scale Divide Values

Value (Decimal)	PXAXB Divider Value
0	1
1	2
2	4
3	8

10. Crystal and Device Circuit Layout Recommendations

The main layout issues that should be carefully considered include the following:

1. Number and size of the ground vias for the Epad
2. Output clock trace routing
3. Input clock trace routing
4. Control and Status signals to input or output clock trace coupling
5. Xtal signal coupling
6. Xtal layout (See 10.1.2 Si5342H/44 Crystal Guidelines for important crystal layout guidelines.)

If the application uses a crystal for the XAXB inputs a shield should be placed underneath the crystal connected to the X1 and X2 pins (4 and 7) to provide the best possible performance. The shield should not be connected to the ground plane and the planes underneath should have as little under the shield as possible. It may be difficult to do this for all the layers, but it is important to do this for the layers that are closest to the shield.

10.1 44-Pin QFN Si5344H/42 Layout Recommendations

This section details the layout recommendations for the 44-pin Si5344H and Si5342H devices using an example 6-layer PCB.

The following guidelines details images of a six layer board with the following stack:

- Layer 1: device layer, with low speed CMOS control/status signals, ground flooded
- Layer 2: crystal shield, output clocks, ground flooded
- Layer 3: ground plane
- Layer 4: power distribution, ground flooded
- Layer 5: input clocks, ground flooded
- Layer 6: low-speed CMOS control/status signals, ground flooded

This layout was designed to implement either a crystal or an external oscillator as the XAXB reference. The top layer is flooded with ground. The clock output pins go to layer 2 using vias to avoid crosstalk during transit. When the clock output signals are on layer 2 there is a ground shield above, below and on all sides for protection. Output clocks should always be routed on an internal layer with ground reference planes directly above and below. The plane that has the routing for the output clocks should have ground flooded near the clock traces to further isolate the clocks from noise and other signals.

10.1.1 Si5342H/44 Applications without a Crystal

If the application does not use a crystal, then the X1 and X2 pins should be left as “no connect” and should not be tied to ground. In addition, there is no need for a crystal shield or the voids underneath the shield. If there is a differential external clock input on XAXB there should be a termination circuit near the XA and XB pins. This termination circuit should be two 50 Ω resistors and one 0.1 µF cap connected in the same manner as on the other clock inputs (IN0, IN1 and IN2). The clock input on XAXB must be ac-coupled. Care should be taken to keep all clock inputs well isolated from each other as well as any other dynamic signal.

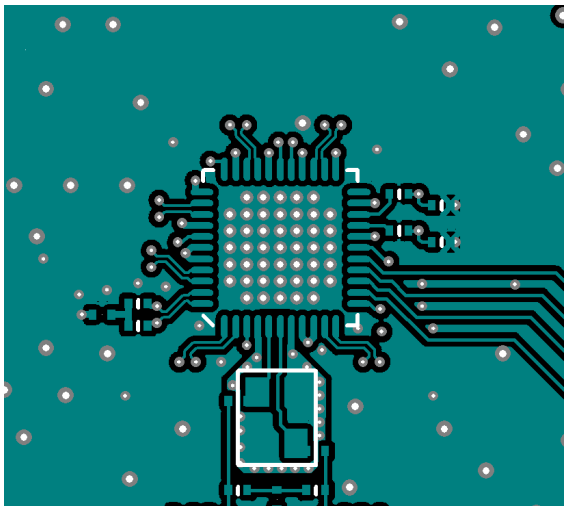


Figure 10.1. Device Layer (Layer 1)

10.1.2 Si5342H/44 Crystal Guidelines

Figure 10.2 Crystal Shield Layer 2 on page 50 is the second layer. The second layer implements the shield underneath the crystal. The shield extends underneath the entire crystal and the X1 and X2 pins. There should be no less than 12 vias to connect the X1 and X2 planes on layers 1 and 2. These vias are not shown in any other figures. All traces with signals that are not static must be kept well away from the crystal and the X1 and X2 plane.

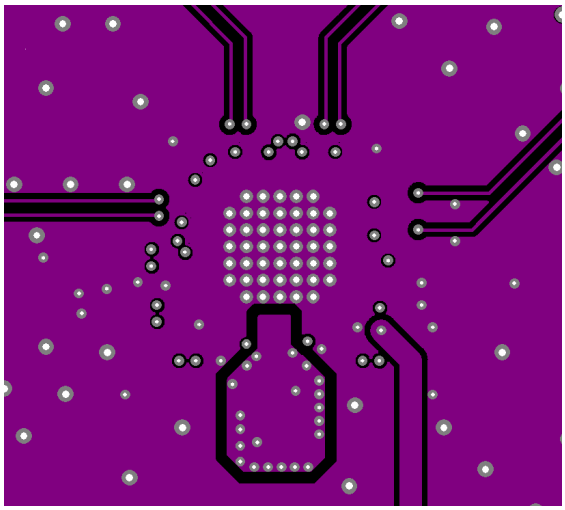


Figure 10.2. Crystal Shield Layer 2

Figure 10.3 Ground Plane (Layer 3) on page 50 is the ground plane and shows a void underneath the crystal shield.

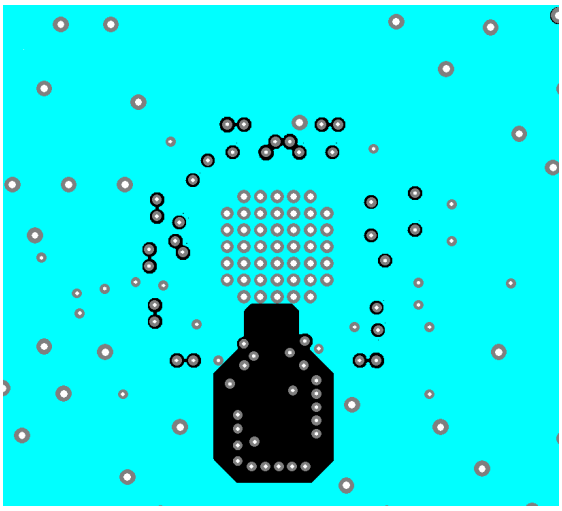


Figure 10.3. Ground Plane (Layer 3)

Figure 10.4 Power Plane and Clock Output Power Supply Traces (Layer 4) on page 51 is a power plane showing the clock output power supply traces. The void underneath the crystal shield is continued.

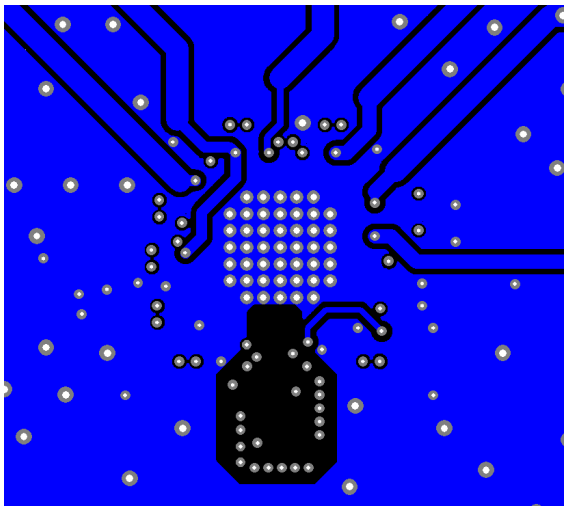


Figure 10.4. Power Plane and Clock Output Power Supply Traces (Layer 4)

Figure 10.5 Clock Input Traces (Layer 5) on page 51 shows layer 5 and the clock input traces. Similar to the clock output traces, they are routed to an inner layer and surrounded by ground to avoid crosstalk.

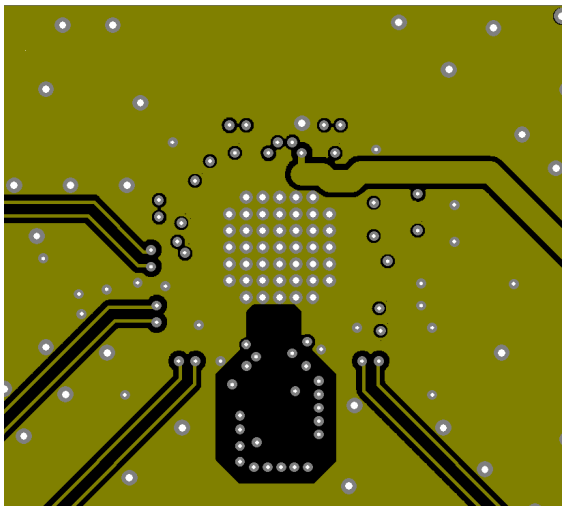


Figure 10.5. Clock Input Traces (Layer 5)

Figure 10.6 Low-Speed CMOS Control and Status Signal Layer 6 (Bottom Layer) on page 52 shows the bottom layer, which continues the void underneath the shield. Layer 6 and layer 1 are mainly used for low speed CMOS control and status signals for which crosstalk is not a significant issue. PCB ground can be placed under the XTAL Ground shield (X1/X2) as long as the PCB ground is at least 0.05 inches below it.

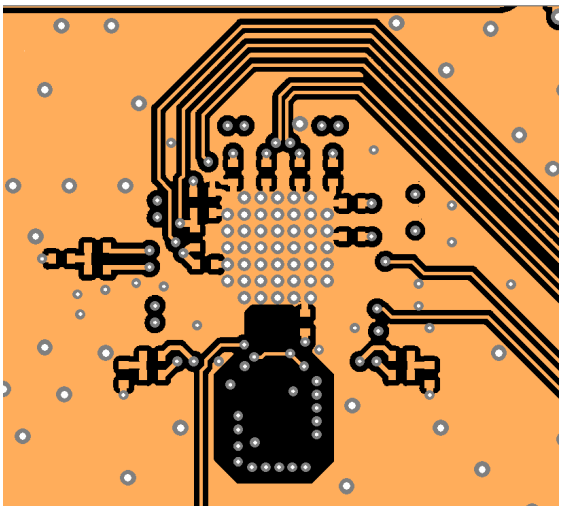


Figure 10.6. Low-Speed CMOS Control and Status Signal Layer 6 (Bottom Layer)

For any high-speed, low-jitter application, the clock signal runs should be impedance-controlled to 100 Ω differential or 50 Ω single-ended. Differential signaling is preferred because of its increased immunity to common-mode noise. All clock I/O runs should be properly terminated.

11. Power Management

11.1 Power Management Features

Several unused functions can be powered down to minimize power consumption. The registers listed in the table below are used for powering down different features.

Table 11.1. Power-Down Registers

Register Name	Hex Address [Bit Field]		Function
	Si5344H	Si5342H	
PDN	0x001E[0]	0x001E[0]	This bit allows the device to be powered down. The serial interface remains powered.
OUT0_PDN	0x0112[0]	0x0112[0]	Powers down all unused clock outputs.
OUT1_PDN	0x0117[0]	0x0117[0]	
OUT2_PDN	0x0126[0]		
OUT3_PDN	0x012B[0]		
OUT_PDN_ALL	0x0145[0]	0x0145[0]	Power down all outputs
XAXB_EXTCLK_EN	0x090E[1]	0x090E[1]	0 to use a crystal at the XAXB pins, 1 to use an external clock source at the XAXB pins

11.2 Power Supply Recommendations

The power supply filtering generally is important for optimal timing performance. The Si5344H/42H devices have multiple stages of on-chip regulation to minimize the impact of board level noise on clock jitter. Following conventional power supply filtering and layout techniques will further minimize signal degradation from the power supply.

It is recommended to use a 0402 1 µF ceramic capacitor on each power supply pin for optimal performance. If the supply voltage is extremely noisy, it might be necessary to use a ferrite bead in series between the supply voltage and the power supply pin.

11.3 Power Supply Sequencing

Four classes of supply voltages exist on the Si5344H/42H:

1. VDD = 1.8 V (Core digital supply)
2. VDDA = 3.3 V (Analog supply)
3. VDDOx = 1.8/2.5/3.3 V ± 5% (Clock output supply)
4. VDDS = 1.8/3.3 V ± 5% (Digital I/O supply)

There is no requirement for power supply sequencing unless the output clocks are required to be phase aligned with each other. In this case, the VDDO of each clock which needs to be aligned must be powered up before VDD and VDDA. VDDS has no effect on output clock alignment.

If output-to-output alignment is required for applications where it is not possible to properly sequence the power supplies, then the output clocks can be aligned by asserting the SOFT_RST 0x001C[0] or Hard Reset 0x001E[1] register bits or driving the RSTB pin. Note that using a hard reset will reload the register with the contents of the NVM and any unsaved changes will be lost.

11.4 Grounding Vias

The pad on the bottom of the device functions as both the sole electrical ground and primary heat transfer path. Hence it is important to minimize the inductance and maximize the heat transfer from this pad to the internal ground plane of the PCB. Use no fewer than 25 vias from the center pad to a ground plane under the device. In general, more vias will perform better. Having the ground plane near the top layer will also help to minimize the via inductance from the device to ground and maximize the heat transfer away from the device.

12. Register Map

12.1 Base vs. Factory Preprogrammed Devices

The Si5344H/42H devices can be ordered as “base” or “factory-preprogrammed” (also known as “custom OPN”) versions.

12.1.1 “Base” Devices (a.k.a. “Blank” Devices)

- Example “base” orderable part numbers (OPNs) are of the form “Si5344H-C-GM”.
- Base devices are available for applications where volatile reads and writes are used to program and configure the device for a particular application.
- Base devices do not power up in a usable state (all output clocks are disabled).
- Base devices are, however, configured by default to use a 48 MHz crystal on the XAXB reference and a 1.8 V compatible I/O voltage setting for the host I^2C/SPI interface.
- Additional programming of a base device is mandatory to achieve a usable configuration.
- See the on-line lookup utility at: http://www.silabs.com/products/clocksoscillators/clock-generator/Pages/clockbuilder-lookup.aspx to access the default configuration plan and register settings for any base OPN.

12.1.2 “Factory Preprogrammed” (Custom OPN) Devices

- Factory preprogammed devices use a “custom OPN”, such as Si5344H-Cxxxxx-GM, where xxxxx is a sequence of characters assigned by Silicon Labs for each customer-specific configuration. These characters are referred to as the “OPN ID”. Customers must initiate custom OPN creation using the ClockBuilder Pro software.
- Many customers prefer to order devices which are factory preprogrammed for a particular application that includes specifying the XAXB reference frequency/type, the clock input frequencies, the clock output frequencies, as well as the other options, such as automatic clock selection, loop BW, etc. The ClockBuilder software is required to select among all of these options and to produce a project file which Silicon Labs uses to preprogram all devices with custom orderable part number (“custom OPN”).
- Custom OPN devices contain all of the initialization information in their non-volatile memory (NVM) so that it powers up fully configured and ready to go.
- Because preprogrammed device applications are inherently quite different from one another, the default power up values of the register settings can be determined using the custom OPN utility at: http://www.silabs.com/products/clocksoscillators/clock-generator/Pages/clockbuilder-lookup.aspx.
- Custom OPN devices include a device top mark which includes the unique OPN ID. Refer to the device data sheet's Ordering Guide and Top Mark sections for more details.

Both “base” and “factory preprogrammed” devices can have their operating configurations changed at any time using volatile reads and writes to the registers. Both types of devices can also have their current register configuration written to the NVM by executing an NVM bank burn sequence (see 3.3 NVM Programming.)

12.2 Register Map Overview and Default Settings Values

The Si5344H/42H family has a large register map and is divided into separate pages. Each page contains a total of 256 registers, although all 256 registers are not used. Register 1 on each page is reserved to indicate the page and register 0x00FE is reserved for the device ready status. The following is a summary of the content that can be found on each of the pages. Note any page that is not listed is not used for the device. Do not attempt to write to registers that have not been described in this document, even if they are accessible. Note that the default value will depend on the values loaded into NVM, which is determined by the part number.

Where not provided in the register map information below, you can get the default values of the regiister map settings by accessing the part number lookup utility at: http://www.silabs.com/products/clocksoscillators/clock-generator/Pages/clockbuilder-lookup.aspx
. Register map settings values are listed in the datasheet addendum, which can also be accessed by using the link above.The register maps are broken out for the Si5344H and Si5342H separately.

Table 12.1. Register Map Paging Descriptions

Page	Start Address (Hex)	Start Address (Decimal)	Contents
Page 0	0000h	0	Alarms, interrupts, reset, other configuration
Page 1	0100h	256	Clock output configuration
Page 2	0200h	512	P,R dividers, scratch area
Page 3	0300h	768	Output N dividers, N divider Finc/Fdec
Page 5	0500h	1280	M divider, BW, holdover, input switch, FINC/DEC
Page 9	0900h	2304	Control IO configuration

R = Read Only

R/W = Read Write

S = Self Clearing

Registers that are sticky are cleared by writing “0” to the bits that have been set in hardware. A self-clearing bit will clear on its own when the state has changed.

12.3 Si5344H Register Definitions

12.3.1 Page 0 Registers Si5344H

Table 12.2. 0x0000 Die Rev

Reg Address	Bit Field	Type	Name	Description
0x0000	3:0	R	DIE_REV	4- bit Die Revision Number

Table 12.3. 0x0001 Page

Reg Address	Bit Field	Type	Name	Description
0x0001	7:0	R/W	PAGE	Selects one of 256 possible pages.

There is the “Page Register” which is located at address 0x01 on every page. When read, it will indicate the current page. When written, it will change the page to the value entered. There is a page register at address 0x0001, 0x0101, 0x0201, 0x0301, … etc.

Table 12.4. 0x0002–0x0003 Base Part Number

Reg Address	Bit Field	Type	Name	Value	Description
0x0002	7:0	R	PN_BASE	0x44	Four-digit “base” part number, one nibble per digit Example: Si5344H-C-GM. The base part number (OPN) is 5344, which is stored in this register
0x0003	15:8	R	PN_BASE	0x53	

Table 12.5. 0x0004 Device Grade

Reg Address	Bit Field	Type	Name	Description
0x0004	7:0	R	GRADE	One ASCII character indicating the device speed/ synthesis mode 0 = A 1 = B 2 = C 3 = D 7 = H

Refer to the device data sheet Ordering Guide section for more information about device grades.

Table 12.6. 0x0005 Device Revision

Reg Address	Bit Field	Type	Name	Description
0x0005	7:0	R	DEVICE_REV	One ASCII character indicating the device revision level. 0 = A; 1 = B, 2 = C, etc. Example Si5344H-C12345-GM, the device revision is “C” and stored as 2.

Table 12.7. 0x0006–0x0008 TOOL_VERSION

Reg Address	Bit Field	Type	Name	Description
0x0006	3:0	R/W	TOOL_VERSION[3:0]	Special
0x0006	7:4	R/W	TOOL_VERSION[7:4]	Revision
0x0007	7:0	R/W	TOOL_VERSION[15:8]	Minor[7:0]
0x0008	0	R/W	TOOL_VERSION[15:8]	Minor[8]
0x0008	4:1	R/W	TOOL_VERSION[16]	Major
0x0008	7:5	R/W	TOOL_VERSION[13:17]	Tool. 0 for ClockBuilder Pro

The software tool version that created the register values that are downloaded at power up is represented by TOOL_VERSION.

Table 12.8. 0x0009 Temperature Grade

Reg Address	Bit Field	Type	Name	Description
0x0009	7:0		TEMP_GRADE	Device temperature grading 0 = Industrial (-40° C to 85° C) ambient conditions

Table 12.9. 0x000A Package ID

Reg Address	Bit Field	Type	Name	Description
0x000A	7:0		PKG_ID	Package ID 1 = 7x7 mm 44 QFN

Part numbers are of the form:

Si<Part Num Base><Grade>-<Device Revision><OPN ID>-<Temp Grade><Package ID>

Examples:

Si5344H-C12345-GM.

Applies to a “base” or “blank” OPN (Ordering Part Number) device. These devices are factory pre-programmed with the frequency plan and all other operating characteristics defined by the user’s ClockBuilder Pro project file.

Si5344H-C-GM.

Applies to a “base” or “non-custom” OPN device. Base devices are factory pre-programmed to a specific base part type (e.g., Si5344H but exclude any user-defined frequency plan or other user-defined operating characteristics selected in ClockBuilder Pro.

Table 12.10. 0x000B I2C Address

Reg Address	Bit Field	Type	Name	Description
0x000B	6:2	R/W	I2C_ADDR	The upper 5 bits of the 7 bit I^2C address. The lower 2 bits are controlled by the A1 and A0 pins.

Table 12.11. 0x000C Internal Status Bits

Reg Address	Bit Field	Type	Name	Description
0x000C	0	R	SYSINCAL	1 if the device is calibrating.
0x000C	1	R	LOSXAXB	1 if there is no signal at the XAXB pins.
0x000C	2	R		
0x000C	3	R		
0x000C	4	R		
0x000C	5	R	SMBUS_TIMEOUT	1 if there is an SMBus timeout error.

Bit 1 is the LOS status monitor for the XTAL or REFCLK at the XA/XB pins.

Table 12.12. 0x000D Out-of-Frequency (OOF) and Loss-of Signal (LOS) Alarms

Reg Address	Bit Field	Type	Name	Description
0x000D	1:0	R	LOS	1 if the clock input is currently LOS
0x000D	5:4	R	OOF	1 if the clock input is currently OOF

Note that each bit corresponds to the input. The LOS and OOF bits are not sticky.

Input 0 (IN0) corresponds to LOS 0x000D [0], OOF 0x000D [4]

Input 1 (IN1) corresponds to LOS 0x000D [1], OOF 0x000D [5]

Table 12.13. 0x000E Holdover and LOL Status

Reg Address	Bit Field	Type	Name	Description
0x000E	1	R	LOL	1 if the DSPLL is out of lock
0x000E	5	R	HOLD	1 if the DSPLL is in holdover (or free run)

These status bits indicate if the DSPLL is in holdover and if it is in Loss of Lock. These bits are not sticky.

Table 12.14. 0x000F Calibration Status

Reg Address	Bit Field	Type	Name	Description
0x000F	5	R	CAL_PLL	1 if the DSPLL internal calibration is busy

This status bit indicates if a DSPLL is currently busy with calibration. This bit is not sticky.

Table 12.15. 0x0011 Sticky versions of Internal Status Bits

Reg Address	Bit Field	Type	Name	Description
0x0011	0	R	SYSINCAL_FLG	Sticky version of SYSINCAL
0x0011	1	R	LOSXAXB_FLG	Sticky version of LOSXAXB
0x0011	2	R		
0x0011	3	R		
0x0011	4	R		

Reg Address	Bit Field	Type	Name	Description
0x0011	5	R	SMBUS_TIMEOUT_FLG	Sticky version of SMBUS_TIMEOUT

These are sticky flag bits. They are cleared by writing zero to the bit that has been set.

Table 12.16. 0x0012 Sticky OOF and LOS Flags

Reg Address	Bit Field	Type	Name	Description
0x0012	1:0	R/W	LOS_FLG	1 if the clock input is LOS for the given input
0x0012	5:4	R/W	OOF_FLG	1 if the clock input is OOF for the given input

These are the sticky flag versions of register 0x000D. These bits are cleared by writing 0 to the bits that have been set.

Input 0 (IN0) corresponds to LOS_FLG 0x0012 [0], OOF_FLG 0x0012 [4]

Input 1 (IN1) corresponds to LOS_FLG 0x0012 [1], OOF_FLG 0x0012 [5]

Table 12.17. 0x0013 Sticky Holdover and LOL Flags

Reg Address	Bit Field	Type	Name	Description
0x0013	1	R/W	LOL_FLG	1 if the DSPLL was unlocked
0x0013	5	R/W	HOLD_FLG	1 if the DSPLL was in holdover or free run

These are the sticky flag versions of register 0x000E. These bits are cleared by writing 0 to the bits that have been set.

Table 12.18. 0x0014 Sticky PLL Calibration Flag

Reg Address	Bit Field	Type	Name	Description
0x0014	5	R/W	CAL_FLG_PLL	1 if the internal calibration is busy

This bit is the sticky flag version of 0x000F. This bit is cleared by writing 0 to bit 5.

Table 12.19. 0x0017 Status Flag Masks

Reg Address	Bit Field	Type	Name	Description
0x0017	0	R/W	SYSINCAL_INTR_MSK	1 to mask SYSINCAL_FLG from causing an interrupt
0x0017	1	R/W	LOSXAXB_FLG_MSK	1 to mask the LOSXAXB_FLG from causing an interrupt
0x0017	2	R/W		
0x0017	3	R/W		
0x0017	4	R/W		
0x0017	5	R/W	SMBUS_TIMEOUT_FLG_MSK	1 to mask SMBUS_TIMEOUT_FLG from the interrupt

These are the interrupt mask bits for the fault flags in register 0x0011. If a mask bit is set, the alarm will be blocked from causing an interrupt.

Note: Bit 1 corresponds to XAXB LOS from asserting the interrupt (INTRb) pin.

Table 12.20. 0x0018 OOF and LOS Masks

Reg Address	Bit Field	Type	Name	Description
0x0018	1:0	R/W	LOS_INTR_MSK	1 to mask the clock input LOS flag
0x0018	5:4	R/W	OOF_INTR_MSK	1 to mask the clock input OOF flag

These are the interrupt mask bits for the OOF and LOS flags in register 0x0012.

Input 0 (IN0) corresponds to LOS_INTR_MSK 0x0018 [0], OOF_INTR_MSK 0x0018 [4]

Input 1 (IN1) corresponds to LOS_INTR_MSK 0x0018 [1], OOF_INTR_MSK 0x0018 [5]

Table 12.21. 0x0019 Holdover and LOL Masks

Reg Address	Bit Field	Type	Name	Description
0x0019	1	R/W	LOL_INTR_MSK	1 to mask the clock input LOL flag
0x0019	5	R/W	HOLD_INTR_MSK	1 to mask the holdover flag

These are the interrupt mask bits for the LOL and HOLD flags in register 0x0013. If a mask bit is set the alarm will be blocked from causing an interrupt.

Table 12.22. 0x001A PLL Calibration Interrupt Mask

Reg Address	Bit Field	Type	Name	Description
0x001A	5	R/W	CAL_INTR_MSK	1 to mask the DSPLL internal calibration busy flag

The interrupt mask for this bit flag bit corresponds to register 0x0014.

the error flags in register 0x0017. If a mask bit is set, the alarm will be blocked from causing an interrupt.

Table 12.23. 0x001C Soft Reset and Calibration

Reg Address	Bit Field	Type	Name	Description
0x001C	0	S	SOFT_RST	1 Initialize and calibrates the entire device 0 No effect

These bits are of type “S”, which is self-clearing.

Table 12.24. 0x001D FINC, FDEC

Reg Address	Bit Field	Type	Name	Description
0x001D	0	S	FINC	1 a rising edge will cause the selected MultiSynth to increment the output frequency by the FstepW parameter. See registers 0x0339-0x0353
0x001D	1	S	FDEC	1 a rising edge will cause the selected MultiSynth to decrement the output frequency by the FstepW parameter. See registers 0x0339-0x0353

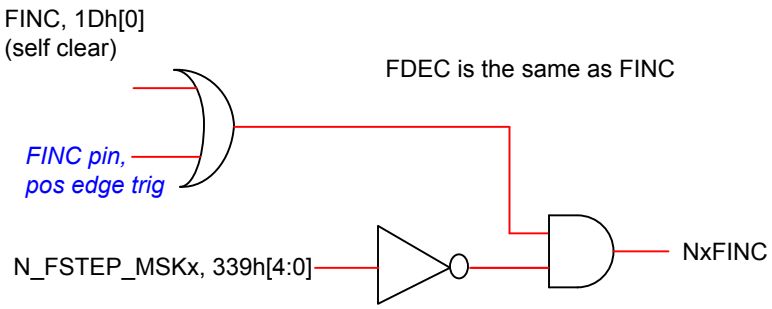


Figure 12.1. Logic Diagram of the FINC/FDEC Masks

Table 12.25. 0x001E Sync, Power Down and Hard Reset

Reg Address	Bit Field	Type	Name	Description
0x001E	0	R/W	PDN	1 to put the device into low power mode
0x001E	1	S	HARD_RST	1 causes hard reset. The same as power up except that the serial port access is not held at reset. This does not self-clear, so after setting the bit it must be cleared. 0 No reset
0x001E	2	S	SYNC	Logically equivalent to asserting the SYNC pin. Resets all R dividers to the same state.

Table 12.26. 0x002B SPI 3 vs 4 Wire

Reg Address	Bit Field	Type	Name	Description
0x002B	3	R/W	SPI_3WIRE	0 for 4-wire SPI, 1 for 3-wire SPI

Table 12.27. 0x002C LOS Enable

Reg Address	Bit Field	Type	Name	Description
0x002C	1:0	R/W	LOS_EN	1 to enable LOS for a clock input; 0 for disable

Input 0 (IN0): LOS_EN[0]

Input 1 (IN1): LOS_EN[1]

Table 12.28. 0x002D Loss of Signal Re-Qualification Value

Reg Address	Bit Field	Type	Name	Description
0x002D	1:0	R/W	LOS0_VAL_TIME	Clock Input 0 0 for 2 msec 1 for 100 msec 2 for 200 msec 3 for one second
0x002D	3:2	R/W	LOS1_VAL_TIME	Clock Input 1, same as above

When an input clock disappears (and therefore has an active LOS alarm), if the clock returns, there is a period of time that the clock must be within the acceptable range before the alarm is removed. This is the LOS_VAL_TIME.

Table 12.29. 0x002E-0x002F LOS0 Trigger Threshold

Reg Address	Bit Field	Type	Name	Description
0x002E	7:0	R/W	LOS0_TRG_THR	16-bit Threshold Value
0x002F	15:8	R/W	LOS0_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 0, given a particular frequency plan.

Table 12.30. 0x0030-0x0031 LOS1 Trigger Threshold

Reg Address	Bit Field	Type	Name	Description
0x0030	7:0	R/W	LOS1_TRG_THR	16-bit Threshold Value
0x0031	15:8	R/W	LOS1_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 1, given a particular frequency plan.

Table 12.31. 0x0036-0x0037 LOS0 Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x0036	7:0	R/W	LOS0_CLR_THR	16-bit Threshold Value
0x0037	15:8	R/W	LOS0_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 0, given a particular frequency plan.

Table 12.32. 0x0038-0x0039 LOS1 Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x0038	7:0	R/W	LOS1_CLR_THR	16-bit Threshold Value
0x0039	15:8	R/W	LOS1_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 1, given a particular frequency plan.

Table 12.33. 0x003F OOF Enable

Reg Address	Bit Field	Type	Name	Description
0x003F	1:0	R/W	OOF_EN	1 to enable, 0 to disable
0x003F	5:4	R/W	FAST_OOF_EN	1 to enable, 0 to disable

Input 0 corresponds to OOF_EN [0], FAST_OOF_EN [4]

Input 1 corresponds to OOF_EN [1], FAST_OOF_EN [5]

Table 12.34. 0x0040 OOF Reference Select

Reg Address	Bit Field	Type	Name	Description
0x0040	2:0	R/W	OOF_REF_SEL	0 for CLKIN0 1 for CLKIN1 4 for XAXB

Table 12.35. 0x0046-0x0049 Out of Frequency Set Threshold

Reg Address	Bit Field	Type	Name	Description
0x0046	7:0	R/W	OOF0_SET_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm 255 = 510 ppm
0x0047	7:0	R/W	OOF1_SET_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm 255 = 510 ppm

These registers determine the OOF alarm set threshold for IN1 and IN0. The range is from ±2 ppm up to ±510 ppm in steps of 2 ppm.

Table 12.36. 0x004A-0x004D Out of Frequency Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x004A	7:0	R/W	OOF0_CLR_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm 255 = 510 ppm
0x004B	7:0	R/W	OOF1_CLR_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm 255 = 510 ppm

These registers determine the OOF alarm clear threshold for IN1 and IN0. The range is from ±2 ppm up to ±510 ppm in steps of 2 ppm. ClockBuilder Pro is used to determine the values for these registers.

Table 12.37. 0x0051-0x0054 Fast Out of Frequency Set Threshold

Reg Address	Bit Field	Type	Name	Description
0x0051	7:0	R/W	FAST_OOF0_SET_THR	(1+ value) x 1000 ppm
0x0052	7:0	R/W	FAST_OOF1_SET_THR	(1+ value) x 1000 ppm

These registers determine the OOF alarm set threshold for IN1 and IN0 when the fast control is enabled. The value in each of the register is (1+ value) x 1000 ppm. ClockBuilder Pro is used to determine the values for these registers.

Table 12.38. 0x0055-0x0058 Fast Out of Frequency Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x0055	7:0	R/W	FAST_OOF0_CLR_THR	(1+ value) x 1000 ppm
0x0056	7:0	R/W	FAST_OOF1_CLR_THR	(1+ value) x 1000 ppm

These registers determine the OOF alarm clear threshold for IN1 and IN0 when the fast control is enabled. The value in each of the register is (1+ value)*1000 ppm. ClockBuilder Pro is used to determine the values for these registers.

OOF needs a frequency reference. ClockBuilder Pro provides the OOF register values for a particular frequency plan.

Table 12.39. 0x009A LOL Enable

Reg Address	Bit Field	Type	Name	Description
0x009A	1	R/W	LOL_SLW_EN_PLL	1 to enable LOL; 0 to disable LOL.

ClockBuilder Pro provides the LOL register values for a particular frequency plan.

Table 12.40. 0x009E LOL Set Threshold

Reg Address	Bit Field	Type	Name	Description
0x009E	7:4	R/W	LOL_SET_THR	Configures the loss of lock set thresholds. Selectable as 0.2, 0.6, 2, 6, 20, 60, 200, 600, 2000, 6000, 20000. Values are in ppm. Default is 0.2 ppm.

The following are the thresholds for the value that is placed in the top four bits of register 0x009E.

0 = 0.2 ppm (default)

1 = 0.6 ppm

2 = 2 ppm

3 = 6 ppm

4 = 20 ppm

5 = 60 ppm

6 = 200 ppm

7 = 600 ppm

8 = 2000 ppm

9 = 6000 ppm

10 = 20000 ppm

Table 12.41. 0x00A0 LOL Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x00A0	7:4	R/W	LOL_CLR_THR	Configures the loss of lock clear thresholds. Selectable as 0.2, 0.6, 2, 6, 20, 60, 200, 600, 2000, 6000, 20000. Values in ppm.

The following are the thresholds for the value that is placed in the top four bits of register 0x00A0. ClockBuilder Pro sets these values.

0 = 0.2 ppm

1 = 0.6 ppm

2 = 2 ppm (default)

3 = 6 ppm

4 = 20 ppm

5 = 60 ppm

6 = 200 ppm

7 = 600 ppm

8 = 2000 ppm

9 = 6000 ppm

10 = 20000 ppm

Table 12.42. 0x00A2 LOL Timer Enable

Reg Address	Bit Field	Type	Name	Description
0x00A2	1	R/W	LOL_TIMER_EN	0 to disable 1 to enable

LOL_TIMER_EN extends the time after LOL negates that the clock outputs can be disabled by LOL_CLR_DELAY (see below).

Table 12.43. 0x00A8-0x00AC LOL Clear Delay

Reg Address	Bit Field	Type	Name	Description
0x00A8	7:0	R/W	LOL_CLR_DELAY	35-bit value
0x00A9	15:8	R/W	LOL_CLR_DELAY	
0x00AA	23:16	R/W	LOL_CLR_DELAY	
0x00AB	31:24	R/W	LOL_CLR_DELAY	
0x00AC	34:32	R/W	LOL_CLR_DELAY	

The LOL Clear Delay value is set by ClockBuilder Pro.

Table 12.44. 0x00E2

Reg Address	Bit Field	Type	Name	Description
0x00E2	7:0	R	ACTIVE_NVM_BANK	Read-only field indicating number of user bank writes caried out so far. Value Description 0 zero 3 one 15 two 63 three

Table 12.45. 0x00E3

Reg Address	Bit Field	Type	Name	Description
0x00E3	7:0	R/W	NVM_WRITE	Write 0xC7 to initiate an NVM bank burn.

See 3.3 NVM Programming.

Table 12.46. 0x00E34

Reg Address	Bit Field	Type	Name	Description
0x00E34	0	S	NVM_READ_BANK	1 to download NVM.

When set, this bit will read the NVM down into the volatile memory.

Table 12.47. 0x00FE Device Ready

Reg Address	Bit Field	Type	Name	Description
0x00FE	7:0	R	DEVICE_READY	0x0F when device is ready 0xF3 when device is not ready

Read-only byte to indicate when the device is ready to accept serial bus writes. The user can poll this byte starting at power-on; when DEVICE_READY is 0x0F the user can safely read or write to any other register. This is only needed after power up after a hard reset using register bit 0x001E[1] or during a bank burn (register 0x0E3). The “Device Ready” register is available on every page in the device at the second last register, 0xFE. There is a device ready register at 0x00FE, 0x01FE, 0x02FE, … etc.

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Table 12.48. 0x0102 Global OE Gating for all Clock Output Drivers

Reg Address	Bit Field	Type	Name	Description
0x0102	0	R/W	OUTALL_DISABLE_LOW	1 Pass through the output enables, 0 disables all output drivers

Table 12.49. 0x0112 Clock Output Driver 0 and R-Divider 0 Configuration

Reg Address	Bit Field	Type	Name	Description
0x0112	0	R/W	OUT0_PDN	Output driver 0: 0 to power up the regulator, 1 to power down the regulator. Clock outputs will be weakly pulled-low.
0x0112	1	R/W	OUT0_OE	Output driver 0: 0 to disable the output, 1 to enable the output
0x0112	2	R/W	OUT0_RDIV_FORCE2	0 R0 divider value is set by R0_REG 1 R0 divider value is forced into divide by 2

Table 12.50. 0x0113 Output 0 Format

Reg Address	Bit Field	Type	Name	Description
0x0113	2:0	R/W	OUT0_FORMAT	0 Reserved 1 swing mode (normal swing) differential 2 swing mode (high swing) differential 3 rail to rail swing mode differential 4 LVCMOS single ended 5–7 reserved
0x0113	3	R/W	OUT0_SYNC_EN	0 disable 1 enable
0x0113	5:4	R/W	OUT0_DIS_STATE	Determines the state of an output driver when disabled, selectable as Disable low (0), Disable high (1), High impedance. (2) In high impedance mode the output common mode voltage will be the same when the output is disabled as when the output is enabled.
0x0113	7:6	R/W	OUT0_CMOS_DRV	LVCMOS output impedance. Selectable as CMOS1,CMOS2, CMOS3.

See 5.2 Performance Guidelines for Outputs.

Table 12.51. 0x0114 Output 0 Swing and Amplitude

Reg Address	Bit Field	Type	Name	Description
0x0114	3:0	R/W	OUT0_CM	Output common mode voltage adjustment Programmable swing mode with normal swing configuration: Step size = 100 mV Range = 0.9 V to 2.3 V if VDDO = 3.3 V Range = 0.6 V to 1.5V if VDDO = 2.5 V Range=0.5 V to 0.9 V if VDDO = 1.8 V Programmable swing mode with high0 swing configuration: Step size = 100 mV Range = 0.9 V to 2.3 V if VDDO = 3.3 V Range = 0.6 V to 1.5 V if VDDO = 2.5 V Range = 0.5 V to 0.9 V if VDDO = 1.8 V Rail-to-rail swing Mode configuration: No flexibility DRV0_CM = 6 if VDDO = 3.3 V (Vcm = 1.5 V) DRV0_CM = 10 if VDDO = 2.5 V (Vcm = 1.1 V) DRV0_CM = 13 if VDDO = 1.8 V (Vcm = 0.8 V) LVCMOS mode: Not supported/No effect
0x0114	6:4	R/W	OUT0_AMPL	Output swing adjustment Programmable swing mode with normal swing configuration: Step size = 100 mV Range = 100 mVpp-se to 800 mVpp-se Programmable swing mode with high swing configuration: Step size = 200 mV Range = 200 mVpp-se to 1600 mVpp-se Rail-to-rail swing mode: Not supported/No effect LVCMOS mode: Not supported/No effect

See the settings and values from Table 5.10 Settings for LVDS, LVPECL, and HCSL on page 34 for details of the settings. ClockBuilder Pro is used to select the correct settings for this register.

Table 12.52. 0x0115 R-Divider 0 Mux Selection

Reg Address	Bit Field	Type	Name	Description
0x0115	2:0	R/W	OUT0_MUX_SEL	Output driver 0 input mux select.This selects the source of the multisynth. 0: MS0 1: MS1 2: MS2 3: MS3 4: MS4 5: reserved 6: reserved 7: reserved
0x0115	7:6	R/W	OUT0_INV	CLK and CLKb not inverted CLKb inverted CLK and CLKb inverted CLK inverted

Each output can be configured to use Multisynth N0-N3 divider. The frequency for each N-divider is set in registers 0x0302-0x032C for N0 to N3. Four different frequencies can be set in the N-dividers (N0–N3) and each of the 4 outputs can be configured to any of the 4 different frequencies.

The 4 output drivers are all identical. The single set of descriptions above for output driver 0 applies to the other 3 output drivers.

Table 12.53. Registers that Follow the Same Definitions Above

Register Address	Description	(Same as) Address
0x0117	Clock Output Driver 1 Config	0x0112
0x0118	Clock Output Driver 1 Format, Sync	0x0113
0x0119	Clock Output Driver 1 Ampl, CM	0x0114
0x011A	OUT1_MUX_SEL, OUT1_INV	0x0115
0x0126	Clock Output Driver 2 Config	0x0112
0x0127	Clock Output Driver 2 Format, Sync	0x0113
0x0128	Clock Output Driver 2 Ampl, CM	0x0114
0x0129	OUT2_MUX_SEL, OUT2_INV	0x0115
0x012B	Clock Output Driver 3 Config	0x0112
0x012C	Clock Output Driver 3 Format, Sync	0x0113
0x012D	Clock Output Driver 3 Ampl, CM	0x0114
0x012E	OUT3_MUX_SEL, OUT3_INV	0x0115

Table 12.54. 0x0145 Power Down All

Reg Address	Bit Field	Type	Name	Description
0x0145	0	R/W	OUT_PDN_ALL	0- no effect 1- all drivers powered down

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Table 12.55. 0x0202–0x0205 XAXB Frequency Adjust

Reg Address	Bit Field	Type	Name	Description
0x0202	7:0	R/W	XAXB_FREQ_OFFSET	32 bit offset adjustment
0x0203	15:8	R/W	XAXB_FREQ_OFFSET	
0x0204	23:16	R/W	XAXB_FREQ_OFFSET	
0x0205	31:24	R/W	XAXB_FREQ_OFFSET	

The clock that is present on XAXB pins is used to create an internal frequency reference for the PLL. The XAXB_FREQ_OFFSET word is used to adjust this frequency reference with high resolution. ClockBuilder Pro calculates the correct values for these registers.

Table 12.56. 0x0206 Pre-scale Reference Divide Ratio

Reg Address	Bit Field	Type	Name	Description
0x0206	1:0	R/W	PXAXB	Sets the divider for the input on XAXB

0 = pre-scale value 1

1 = pre-scale value 2

2 = pre-scale value 4

3 = pre-scale value 8

This can only be used with external clock sources, not crystals.

Table 12.57. 0x0208-0x020D P0 Divider Numerator

Reg Address	Bit Field	Type	Name	Description
0x0208	7:0	R/W	P0_NUM	48-bit Integer Number
0x0209	15:8	R/W	P0_NUM	
0x020A	23:16	R/W	P0_NUM	
0x020B	31:24	R/W	P0_NUM	
0x020C	39:32	R/W	P0_NUM	
0x020D	47:40	R/W	P0_NUM	

This set of registers configure the P-dividers which are located at the two input clocks seen in Figure 2.1 Si5342H DSPLL and Multi-synth System Flow Diagram on page 7. ClockBuilder Pro calculates the correct values for the P-dividers.

Table 12.58. 0x020E-0x0211 P0 Divider Denominator

Reg Address	Bit Field	Type	Name	Description
0x020E	7:0	R/W	P0_DEN	32-bit Integer Number
0x020F	15:8	R/W	P0_DEN	
0x0210	23:16	R/W	P0_DEN	
0x0211	31:24	R/W	P0_DEN	

The P1 divider numerator and denominator follow the same format as P0 described above. ClockBuilder Pro calculates the correct values for the P-dividers.

Table 12.59. Registers that Follow the P0_NUM and P0_DEN

Register Address	Description	Size	Same as Address
0x0212-0x0217	P1 Divider Numerator	48-bit Integer Number	0x0208-0x020D
0x0218-0x021B	P1 Divider Denominator	32-bit Integer Number	0x020E-0x0211

This set of registers configure the P-dividers which are located at the two input clocks seen in Figure 2.1 Si5342H DSPLL and Multi-synth System Flow Diagram on page 7. ClockBuilder Pro calculates the correct values for the P-dividers.

Table 12.60. 0x024A-0x024C R0 Divider

Reg Address	Bit Field	Type	Name	Description
0x024A	7:0	R/W	R0_REG	A 24 bit integer divide value
0x024B	15:8	R/W	R0_REG	divide value = (R0_REG+1) x 2
0x024C	23:16	R/W	R0_REG	To set R0 = 2, set OUT0_RDIV_FORCE2 = 1 and then the R0_REG value is irrelevant.

The R dividers are at the output clocks and are purely integer division. The R1–R3 dividers follow the same format as the R0 divider described above.

Table 12.61. 0x0230 Px_UPDATE

Reg Address	Bit Field	Type	Name	Description
0x0230	0	S, R/W	P0_UPDATE	0 - No update for P-divider value
0x0230	1	S, R/W	P1_UPDATE	1 - Update P-divider value

The Px_Update bit must be asserted to update the P-Divider. The update bits are provided so that all of the divider bits can be changed at the same time. First, write all of the new values to the divider, then set the update bit.

Table 12.62. Registers that Follow the R0_REG

Register Address	Description	Size	Same as Address
0x024D-0x024F	R1_REG	24-bit Integer Number	0x024A-0x024C
0x0250-0x0252	R2_REG	24-bit Integer Number	0x024A-0x024C
0x0253-0x0255	R3_REG	24-bit Integer Number	0x024A-0x024C

Table 12.63. 0x026B-0x0272 User Scratch Pad

Reg Address	Bit Field	Type	Name	Description
0x026B	7:0	R/W	DESIGN_ID0	ASCII encoded string defined by CBPro user, with user defined space or null padding of unused characters. A user will normally include a configuration ID + revision ID. For example, “ULT.1A” with null character padding sets: DESIGN_ID0: 0x55 DESIGN_ID1: 0x4C DESIGN_ID2: 0x54 DESIGN_ID3: 0x2E DESIGN_ID4: 0x31 DESIGN_ID5: 0x41 DESIGN_ID6:0x 00 DESIGN_ID7: 0x00
0x026C	15:8	R/W	DESIGN_ID1	
0x026D	23:16	R/W	DESIGN_ID2	
0x026E	31:24	R/W	DESIGN_ID3	
0x026F	39:32	R/W	DESIGN_ID4	
0x0270	47:40	R/W	DESIGN_ID5	
0x0271	55:48	R/W	DESIGN_ID6	
0x0272	63:56	R/W	DESIGN_ID7	

Table 12.64. 0x0278-0x027C OPN Identifier

Reg Address	Bit Field	Type	Name	Description
0x0278	7:0	R/W	OPN_ID0	OPN unique identifier. ASCII encoded. For example, with OPN: Si5344H-C12345-GM, 12345 is the OPN unique identifier, which sets: OPN_ID0: 0x31 OPN_ID1: 0x32 OPN_ID2: 0x33 OPN_ID3: 0x34 OPN_ID4: 0x35
0x0279	15:8	R/W	OPN_ID1	
0x027A	23:16	R/W	OPN_ID2	
0x027B	31:24	R/W	OPN_ID3	
0x027C	39:32	R/W	OPN_ID4	

Part numbers are of the form:

Si<Part Num Base><Grade>-<Device Revision><OPN ID>-<Temp Grade><Package ID>

Examples:

Si5344H-C12345-GM.

Applies to a “custom” OPN (Ordering Part Number) device. These devices are factory pre-programmed with the frequency plan and all other operating characteristics defined by the user’s ClockBuilder Pro project file.

Si5344H-C-GM.

Applies to a “base” or “non-custom” OPN device. Base devices are factory pre-programmed to a specific base part type (e.g., Si5344H but exclude any user-defined frequency plan or other user-defined operating characteristics selected in ClockBuilder Pro.

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Table 12.65. 0x0302-0x0307 N0 Numerator

Reg Address	Bit Field	Type	Name	Description
0x0302	7:0	R/W	N0_NUM	44-bit Integer Number
0x0303	15:8	R/W	N0_NUM	The N0 value is N0_NUM/N0_DEN
0x0304	23:16	R/W	N0_NUM	
0x0305	31:24	R/W	N0_NUM	
0x0306	39:32	R/W	N0_NUM	
0x0307	43:40	R/W	N0_NUM	

The N dividers are interpolative dividers that are used as output dividers that feed into the R dividers. ClockBuilder Pro calculates the correct values for the N-dividers.

Table 12.66. 0x0308-0x030B N0 Denominator

Reg Address	Bit Field	Type	Name	Description
0x0308	7:0	R/W	N0_DEN	32-bit Integer Number
0x0309	15:8	R/W	N0_DEN	The N0 value is N0_NUM/N0_DEN
0x030A	23:16	R/W	N0_DEN	
0x030B	31:24	R/W	N0_DEN	
0x030C	0	R/W	N0_UPDATE	Set this bit to update the N0 divider.

This bit is provided so that all of the N0 divider bits can be changed at the same time. First, write all of the new values to the divider; then, set the update bit.

Table 12.67. Registers that Follow the N0_NUM and N0_DEN Definitions

Register Address	Description	Size	Same as Address
0x030D-0x0312	N1 Numerator	44-bit Integer Number	0x0302-0x0307
0x0313-0x0316	N1 Denominator	32-bit Integer Number	0x0308-0x030B
0x0317	N1_UPDATE	one bit	0x030C
0x0318-0x031D	N2 Numerator	44-bit Integer Number	0x0302-0x0307
0x031E-0x0321	N2 Denominator	32-bit Integer Number	0x0308-0x030B
0x0322	N2_UPDATE	one bit	0x030C
0x0323-0x0328	N3 Numerator	44-bit Integer Number	0x0302-0x0307
0x0329-0x032C	N3 Denominator	32-bit Integer Number	0x0308-0x030B
0x032D	N3_UPDATE	one bit	0x030C

Table 12.68. 0x0338 Global N Divider Update

Reg Address	Bit Field	Type	Name	Description
0x0338	1	R/W	N_UPDATE_ALL	Set this bit to update all five N dividers.

This bit is provided so that all of the divider bits can be changed at the same time. First, write all of the new values to the divider, then set the update bit.

Table 12.69. 0x0339 FINC/FDEC Masks

Reg Address	Bit Field	Type	Name	Description
0x0339	3:0	R/W	N_FSTEP_MSK	0 to enable FINC/FDEC updates 1 to disable FINC/FDEC updates

Bit 0 corresponds to MultiSynth N0 N_FSTEP_MSK 0x0339[0]

Bit 1 corresponds to MultiSynth N1 N_FSTEP_MSK 0x0339[1]

Bit 2 corresponds to MultiSynth N2 N_FSTEP_MSK 0x0339[2]

Bit 3 corresponds to MultiSynth N3 N_FSTEP_MSK 0x0339[3]

Table 12.70. 0x033B-0x0340 N0 Frequency Step Word

Reg Address	Bit Field	Type	Name	Description
0x033B	7:0	R/W	N0_FSTEPW	44-bit Integer Number
0x033C	15:8	R/W	N0_FSTEPW	
0x033D	23:16	R/W	N0_FSTEPW	
0x033E	31:24	R/W	N0_ FSTEPW	
0x033F	39:32	R/W	N0_ FSTEPW	
0x0340	43:40	R/W	N0_ FSTEPW	

This is a 44-bit integer value which is directly added or subtracted from the N-divider. When FINC or FDEC is set to a 1, ClockBuilder Pro calculates the correct values for the N0 Frequency Step Word. Each N divider has the ability to add or subtract up to a 44-bit value.

Table 12.71. Registers that Follow the N0_FSTEPW Definition

Register Address	Description	Size	Same as Address
0x0341-0x0346	N1 Frequency Step Word	44-bit Integer Number	0x033B-0x0340
0x0347-0x034C	N2 Frequency Step Word	44-bit Integer Number	0x033B-0x0340
0x034D-0x0352	N3 Frequency Step Word	44-bit Integer Number	0x033B-0x0340

Table 12.72. 0x0359–0x35A N0 Delay Control

Reg Address	Bit Field	Type	Name	Description
Reg Address	Bit Field	Type	Name	Description
0x0359	7:0	R/W	N0_DELAY[7:0]	Lower byte of N0_DELAY[15:0]
0x035A	7:0	R/W	N0_DELAY[15:8]	Upper byte of N0_DELAY[15:0]

Nx_DELAY[15:0] is a 2s complement number that sets the output delay of MultiSynthx.

The delay in seconds is Nx_DELAY/(256 x Fvco) where Fvco is the VCO frequency in Hz. The maximum positive and negative delay is $\pm(2^{15}-1)/(256 \times Fvco)$. ClockBuilder Pro calculates the correct value for this register. Changing any of the Nx_DELAY values requires a SOFT_RST, a HARD_RST, or a power up sequence.

Table 12.73. 0x035B-0x035C Divider N1 Delay Control

Reg Address	Bit Field	Type	Name	Description
0x35B	7:0	R/W	N1_DELAY[7:0]	Lower byte of N1_DELAY[15:0]
0x35C	7:0	R/W	N1_DELAY[15:8]	Upper byte of N1_DELAY[15:0]

Table 12.74. 0x035D-0x035E Divider N2 Delay Control

Reg Address	Bit Field	Type	Name	Description
Reg Address	Bit Field	Type	Name	Description
0x35D	7:0	R/W	N2_DELAY[7:0]	Lower byte of N2_DELAY[15:0]
0x35E	7:0	R/W	N2_DELAY[15:8]	Upper byte of N2_DELAY[15:0]

Table 12.75. 0x035F-0x0360 Divider N3 Delay Control

Reg Address	Bit Field	Type	Name	Description
Reg Address	Bit Field	Type	Name	Description
0x35F	7:0	R/W	N3_DELAY[7:0]	Lower byte of N3_DELAY[15:0]
0x360	7:0	R/W	N3_DELAY[15:8]	Upper byte of N3_DELAY[15:0]

Nx_DELAY[15:0] is a 2s complement number that sets the output delay of MultiSynthx.

The delay in seconds is Nx_DELAY/(256 x Fvco) where Fvco is the VCO frequency in Hz. The maximum positive and negative delay is $\pm(2^{15}-1)/(256 \times Fvco)$. ClockBuilder Pro calculates the correct value for this register.

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Table 12.76. 0x0507

Reg Address	Bit Field	Type	Name	Description
0x0507	7,6	R	IN_ACTV	Current input clock.

These bits indicate which input clock is currently selected. 0 for IN0, 1 for IN1, etc.

Table 12.77. 0x0508-0x050D Loop Bandwidth

Reg Address	Bit Field	Type	Name	Description
0x0508	7:0	R/W	BW0_PLL	PLL bandwidth parameter
0x0509	15:8	R/W	BW1_PLL	PLL bandwidth parameter
0x050A	23:16	R/W	BW2_PLL	PLL bandwidth parameter
0x050B	31:24	R/W	BW3_PLL	PLL bandwidth parameter
0x050C	39:32	R/W	BW4_PLL	PLL bandwidth parameter
0x050D	47:40	R/W	BW5_PLL	PLL bandwidth parameter

This group of registers determine the loop bandwidth for the DSPLL. It is selectable as 0.1 Hz, 1 Hz, 4 Hz, 10 Hz, 40 Hz, 100 Hz, 400 Hz, 1 kHz, and 4 kHz. The loop BW values are calculated by ClockBuilder Pro and are written into these registers. The BW_UPDATE_PLL bit (reg 0x0514[0]) must be set to cause the BWx_PLL parameters to take effect.

Table 12.78. 0x050E-0x0514 Fast Lock Loop Bandwidth

Reg Address	Bit Field	Type	Name	Description
0x050E	7:0	R/W	FAST_BW0_PLL	PLL fast bandwidth parameter
0x050F	15:8	R/W	FAST_BW1_PLL	PLL fast bandwidth parameter
0x0510	23:16	R/W	FAST_BW2_PLL	PLL fast bandwidth parameter
0x0511	31:24	R/W	FAST_BW3_PLL	PLL fast bandwidth parameter
0x0512	39:32	R/W	FAST_BW4_PLL	PLL fast bandwidth parameter
0x0513	47:40	R/W	FAST_BW5_PLL	PLL fast bandwidth parameter
0x0514	0	S	BW_UPDATE_PLL	Must be set to 1 to update the BWx_PLL and FAST_BWx_PLL parameters

The fast lock loop BW values are calculated by ClockBuilder Pro and used when fast lock is enabled.

Table 12.79. 0x0515-0x051B M Divider Numerator, 56-bits

Reg Address	Bit Field	Type	Name	Description
0x0515	7:0	R/W	M_NUM	56-bit Number
0x0516	15:8	R/W	M_NUM	
0x0517	23:16	R/W	M_NUM	
0x0518	31:24	R/W	M_NUM	
0x0519	39:32	R/W	M_NUM	
0x051A	47:40	R/W	M_NUM	
0x051B	55:48	R/W	M_NUM	

Table 12.80. 0x051C-0x051F M Divider Denominator, 32-bits

Reg Address	Bit Field	Type	Name	Description
0x051C	7:0	R/W	M_DEN	32-bit Number
0x051E	15:8	R/W	M_DEN	
0x051E	23:16	R/W	M_DEN	
0x051F	31:24	R/W	M_DEN	

The loop M divider values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 12.81. 0x0520 M Divider Update Bit

Reg Address	Bit Field	Type	Name	Description
0x0520	0	R/W	M_UPDATE	Set this bit to update the M divider.

Table 12.82. 0x052A Input Clock Select

Reg Address	Bit Field	Type	Name	Description
0x052A	0	R/W	IN_SEL_REGCTRL	0 for pin controlled clock selection 1 for register controlled clock selection
0x052A	1	R/W	IN_SEL	0 for IN0, 1 for IN1

Input clock selection for manual register based and pin controlled clock selection.

Note: When IN_SEL_REGCTRL is low, IN_SEL does not do anything and the clock selection is pin controlled.

Table 12.83. 0x052B Fast Lock Control

Reg Address	Bit Field	Type	Name	Description
0x052B	0	R/W	FASTLOCK_AUTO_EN	Applies only when FASTLOCK_MAN = 0 (see below): 0 to enable auto fast lock when the DSPLL is out of lock 1 to disable auto fast lock

Reg Address	Bit Field	Type	Name	Description
0x052B	1	R/W	FASTLOCK_MAN	0 for normal operation (see above) 1 to force fast lock

When in fast lock, the fast lock loop BW can be automatically used.

Table 12.84. 0x052C Holdover Exit Control

Reg Address	Bit Field	Type	Name	Description
0x052C	3	R/W	HOLD_RAMP_BYP	Must be set to 1 for normal operation.
0x052C	4	R/W	HOLD_EXIT_BW_SEL	0 to use the fastlock loop BW when exiting from holdover 1 to use the normal loop BW when exiting from holdover

Table 12.85. 0x052E Holdover History Average Length

Reg Address	Bit Field	Type	Name	Description
0x052E	4:0	R/W	HOLD_HIST_LEN	5-bit value

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency.

Table 12.86. 0x052F Holdover History Delay

Reg Address	Bit Field	Type	Name	Description
0x052F	4:0	R/W	HOLD_HIST_DELAY	

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushes back into the past, above the averaging window. The amount that the average window is delayed is the holdover history delay.

Table 12.87. 0x0535 Force Holdover

Reg Address	Bit Field	Type	Name	Description
0x0535	0	R/W	FORCE_HOLD	0 for normal operation 1 for force holdover

Table 12.88. 0x0536 Input Clock Switching Control

Reg Address	Bit Field	Type	Name	Description
0x0536	1:0	R/W	CLK_SWTCH_MODE	0 = manual 1 = automatic/non-revertive 2 = automatic/revertive 3 = reserved
0x0536	2	R/W	HSW_EN	0 glitchless switching mode (phase buildout turned off) 1 hitless switching mode (phase buildout turned on)

Table 12.89. 0x0537 Input Alarm Masks

Reg Address	Bit Field	Type	Name	Description
0x0537	1:0	R/W	IN_LOS_MSK	For each clock input LOS alarm: 0 to use LOS in the clock selection logic 1 to mask LOS from the clock selection logic
0x0537	5:4	R/W	IN_OOF_MSK	For each clock input OOF alarm: 0 to use OOF in the clock selection logic 1 to mask OOF from the clock selection logic

This register is for the input clock switch alarm masks. For each of the two clock inputs, the OOF and/or the LOS alarms can be used for the clock selection logic or they can be masked from it. Note that the clock selection logic can affect entry into holdover.

Table 12.90. 0x0538 Clock Inputs 0 and 1 Priority

Reg Address	Bit Field	Type	Name	Description
0x0538	2:0	R/W	IN0_PRIORITY	The priority for clock input 0 is: 0 for clock input not selectable 1 for priority 1 2 for priority 2 3 to 7 are reserved
0x0538	6:4	R/W	IN1_PRIORITY	The priority for clock input 1 is: 0 for clock input not selectable 1 for priority 1 2 for priority 2 3 to 7 are reserved

This register is used to assign a priority to an input clock for automatic clock input switching. The available clock with the lowest priority level will be selected. When input clocks are assigned the same priority, they will use the following default priority list: 0, 1.

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Table 12.91. 0x090E XAXB Configuration

Reg Address	Bit Field	Type	Name	Description
0x090E	0	R/W	XAXB_EXTCLK_EN	0 to use a crystal at the XAXB pins 1 to use an external clock source at the XAXB pins

Table 12.92. 0x0943 Control I/O Voltage Select

Reg Address	Bit Field	Type	Name	Description
0x0943	0	R/W	IO_VDD_SEL	0 for 1.8 V external connections 1 for 3.3 V external connections

The IO_VDD_SEL configuration bit selects the option of operating the serial interface voltage thresholds from the VDD or the VDDA pin. The serial interface pins are always 3.3 V tolerant even when the device's VDD pin is supplied from a 1.8 V source. When the I^2C or SPI host is operating at 3.3 V and the Si5344H/42H at VDD = 1.8 V, the host must write the IO_VDD_SEL configuration bit to the VDDA option. This will ensure that both the host and the serial interface are operating at the optimum voltage thresholds.

Table 12.93. 0x0949 Clock Input Control and Configuration

Reg Address	Bit Field	Type	Name	Description
0x0949	1:0	R/W	IN_EN	0: Disable and Powerdown Input Buffer. 1: Enable Input Buffer for IN1, IN0.
0x0949	5:4	R/W	IN_PULSED_CMOS_EN	0: Standard Input Format. 1: Pulsed CMOS Input Format for IN1, IN0. See 4. Clock Inputs for more information.

When a clock input is disabled, it is powered down.

Input 0 corresponds to IN_SEL 0x0949 [0], IN_PULSED_CMOS_EN 0x0949 [4]

Input 1 corresponds to IN_SEL 0x0949 [1], IN_PULSED_CMOS_EN 0x0949 [5]

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Table 12.94. 0x0A03 Output Multisynth Clock to Output Driver

Reg Address	Bit Field	Type	Name	Description
0x0A03	3:0	R/W	N_CLK_TO_OUTX_EN	Routes Multisynth outputs to output driver muxes.

Table 12.95. 0x0A04 Output Multisynth Integer Divide Mode

Reg Address	Bit Field	Type	Name	Description
0x0A04	3:0	R/W	N_PIBYP	Output Multisynth integer divide mode. Bit 0 for ID0; Bit 1 for ID1, etc. 0: Nx divider is fractional. 1: Nx divider is integer.

Table 12.96. 0x0A05 Output Multisynth Divider Power Down

Reg Address	Bit Field	Type	Name	Description
0x0A05	3:0	R/W	N_PDNB	Powers down the N dividers. Set to 0 to power down unused N dividers. Must set to 1 for all active N dividers. See also related registers 0x0A03 and 0x0B4A.

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Table 12.97. 0x0B44 Output Multisynth Clock to Output Driver

Reg Address	Bit Field	Type	Name	Description
0x0B44	3:0	R/W	PDIV_FRACN_CLK_DIS	Disable digital clocks to input P (IN0–3) fractional dividers.
0x0B44	5	R/W	FRACN_CLK_DIS_PLL	Disable digital clock to M fractional divider.

Table 12.98. 0x0B4A Divider Clock Disables

Reg Address	Bit Field	Type	Name	Description
0x0B4A	3:0	R/W	N_CLK_DIS	Disable digital clocks to N dividers. Must be set to 0 to use each N divider. See also related registers 0x0A03 and 0x0A05.

12.4 Si5342H Register Definitions

12.4.1 Page 0 Registers Si5342H

Table 12.99. 0x0000 Die Rev

Reg Address	Bit Field	Type	Name	Description
0x0000	3:0	R	DIE_REV	4- bit Die Revision Number

Table 12.100. 0x0001 Page

Reg Address	Bit Field	Type	Name	Description
0x0001	7:0	R/W	PAGE	Selects one of 256 possible pages.

There is the “Page Register” which i s located at address 0x01 on every page. When read, it will indicate the current page. When written, it will change the page to the value entered. There is a page register at address 0x0001, 0x0101, 0x0201, 0x0301, … etc.

Table 12.101. 0x0002–0x0003 Base Part Number

Reg Address	Bit Field	Type	Name	Value	Description
0x0002	7:0	R	PN_BASE	0x42	Four-digit “base” part number, one nibble per digit Example: Si5342H-C-GM. The base part number (OPN) is 5342, which is stored in this register.
0x0003	15:8	R	PN_BASE	0x53	

Table 12.102. 0x0004 Device Grade

Reg Address	Bit Field	Type	Name	Description
0x0004	7:0	R	GRADE	One ASCII character indicating the device speed/ synthesis mode 0 = A 1 = B 2 = C 3 = D 7 = H

Refer to the device data sheet Ordering Guide section for more information about device grades.

Table 12.103. 0x0005 Device Revision

Reg Address	Bit Field	Type	Name	Description
0x0005	7:0	R	DEVICE_REV	One ASCII character indicating the device revision level. 0 = A; 1 = B, 2 = C, etc. Example Si5342H-C12345-GM, the device revision is “C” and stored as 2.

Table 12.104. 0x0006–0x0008 TOOL_VERSION

Reg Address	Bit Field	Type	Name	Description
0x0006	3:0	R/W	TOOL_VERSION[3:0]	Special
0x0006	7:4	R/W	TOOL_VERSION[7:4]	Revision
0x0007	7:0	R/W	TOOL_VERSION[15:8]	Minor[7:0]
0x0008	0	R/W	TOOL_VERSION[15:8]	Minor[8]
0x0008	4:1	R/W	TOOL_VERSION[16]	Major
0x0008	7:5	R/W	TOOL_VERSION[13:17]	Tool. 0 for ClockBuilder Pro

The software tool version that created the register values that are downloaded at power up is represented by TOOL_VERSION.

Table 12.105. 0x0009 TEMPERATURE GRADE

Reg Address	Bit Field	Type	Name	Description
0x0009	7:0		TEMP_GRADE	Device temperature grading 0 = Industrial (-40° C to 85° C) ambient conditions

Table 12.106. 0x000A PACKAGE ID

Reg Address	Bit Field	Type	Name	Description
0x000A	7:0		PKG_ID	Package ID 1 = 7x7 mm 44 QFN

Part numbers are of the form:

Si<Part Num Base><Grade>-<Device Revision><OPN ID>-<Temp Grade><Package ID>

Examples:

Si5342H-C12345-GM.

Applies to a “base” or “blank” OPN (Ordering Part Number) device. These devices are factory pre-programmed with the frequency plan and all other operating characteristics defined by the user’s ClockBuilder Pro project file.

Si5342H-C-GM.

Applies to a “base” or “non-custom” OPN device. Base devices are factory pre-programmed to a specific base part type (e.g., Si5342H but exclude any user-defined frequency plan or other user-defined operating characteristics selected in ClockBuilder Pro.

Table 12.107. 0x000B I2C Address

Reg Address	Bit Field	Type	Name	Description
0x000B	6:2	R/W	I2C_ADDR	The upper 5 bits of the 7 bit I^2C address. The lower 2 bits are controlled by the A1 and A0 pins.

Table 12.108. 0x000C Internal Status Bits

Reg Address	Bit Field	Type	Name	Description
0x000C	0	R	SYSINCAL	1 if the device is calibrating.
0x000C	1	R	LOSXAXB	1 if there is no signal at the XAXB pins.
0x000C	2	R		
0x000C	3	R		
0x000C	4	R		
0x000C	5	R	SMBUS_TIMEOUT	1 if there is an SMBus timeout error.

Bit 1 is the LOS status monitor for the XTAL or REFCLK at the XA/XB pins.

Table 12.109. 0x000D Out-of-Frequency (OOF) and Loss-of Signal (LOS) Alarms

Reg Address	Bit Field	Type	Name	Description
0x000D	1:0	R	LOS	1 if the clock input is currently LOS
0x000D	5:4	R	OOF	1 if the clock input is currently OOF

Note that each bit corresponds to the input. The LOS and OOF bits are not sticky.

Input 0 (IN0) corresponds to LOS 0x000D [0], OOF 0x000D [4]

Input 1 (IN1) corresponds to LOS 0x000D [1], OOF 0x000D [5]

Table 12.110. 0x000E Holdover and LOL Status

Reg Address	Bit Field	Type	Name	Description
0x000E	1	R	LOL	1 if the DSPLL is out of lock
0x000E	5	R	HOLD	1 if the DSPLL is in holdover (or free run)

These status bits indicate if the DSPLL is in holdover and if it is in Loss of Lock. These bits are not sticky.

Table 12.111. 0x000F Calibration Status

Reg Address	Bit Field	Type	Name	Description
0x000F	5	R	CAL_PLL	1 if the DSPLL internal calibration is busy

This status bit indicates if a DSPLL is currently busy with calibration. This bit is not sticky.

Table 12.112. 0x0011 Sticky versions of Internal Status Bits

Reg Address	Bit Field	Type	Name	Description
0x0011	0	R	SYSINCAL_FLG	Sticky version of SYSINCAL
0x0011	1	R	LOSXAXB_FLG	Sticky version of LOSXAXB
0x0011	2	R		
0x0011	3	R		
0x0011	4	R		

Reg Address	Bit Field	Type	Name	Description
0x0011	5	R	SMBUS_TIMEOUT_FLG	Sticky version of SMBUS_TIMEOUT

If any of these six bits are high, there is an internal fault. Please contact Silicon Labs. These are sticky flag bits. They are cleared by writing zero to the bit that has been set.

Table 12.113. 0x0012 Sticky OOF and LOS Flags

Reg Address	Bit Field	Type	Name	Description
0x0012	1:0	R/W	LOS_FLG	1 if the clock input is LOS for the given input
0x0012	5:4	R/W	OOF_FLG	1 if the clock input is OOF for the given input

These are the sticky flag versions of register 0x000D. These bits are cleared by writing 0 to the bits that have been set.

Input 0 (IN0) corresponds to LOS_FLG 0x0012 [0], OOF_FLG 0x0012 [4]

Input 1 (IN1) corresponds to LOS_FLG 0x0012 [1], OOF_FLG 0x0012 [5]

Table 12.114. 0x0013 Sticky Holdover and LOL Flags

Reg Address	Bit Field	Type	Name	Description
0x0013	1	R/W	LOL_FLG	1 if the DSPLL was unlocked
0x0013	5	R/W	HOLD_FLG	1 if the DSPLL was in holdover or free run

These are the sticky flag versions of register 0x000E. These bits are cleared by writing 0 to the bits that have been set.

Table 12.115. 0x0014 Sticky INCAL Flag

Reg Address	Bit Field	Type	Name	Description
0x0014	5	R/W	CAL_FLG_PLL	1 if the internal calibration was busy

This bit is the sticky flag version of 0x000F. This bit is cleared by writing 0 to bit 5.

Table 12.116. 0x0017 Status Flag Masks

Reg Address	Bit Field	Type	Name	Description
0x0017	0	R/W	SYSINCAL_INTR_MSK	1 to mask SYSINCAL_FLG from causing an interrupt
0x0017	1	R/W	LOSXAXB_FLG_MSK	1 to mask the LOSXAXB_FLG from causing an interrupt
0x0017	2	R/W		
0x0017	3	R/W		
0x0017	4	R/W		
0x0017	5	R/W	FAULT5_FLG_MSK	1 to mask SMBUS_TIMEOUT_FLG from the interrupt

These are the interrupt mask bits for the fault flags in register 0x0011. If a mask bit is set, the alarm will be blocked from causing an interrupt.

Note: Bit 1 corresponds to XAXB LOS from asserting the interrupt (INTRb) pin.

Table 12.117. 0x0018 OOF and LOS Masks

Reg Address	Bit Field	Type	Name	Description
0x0018	1:0	R/W	LOS_INTR_MSK	1 to mask the clock input LOS flag
0x0018	5:4	R/W	OOF_INTR_MSK	1 to mask the clock input OOF flag

These are the interrupt mask bits for the OOF and LOS flags in register 0x0012.

Input 0 (IN0) corresponds to LOS_INTR_MSK 0x0018 [0], OOF_INTR_MSK 0x0018 [4]

Input 1 (IN1) corresponds to LOS_INTR_MSK 0x0018 [1], OOF_INTR_MSK 0x0018 [5]

Table 12.118. 0x0019 Holdover and LOL Masks

Reg Address	Bit Field	Type	Name	Description
0x0019	1	R/W	LOL_INTR_MSK	1 to mask the clock input LOL flag
0x0019	5	R/W	HOLD_INTR_MSK	1 to mask the holdover flag

These are the interrupt mask bits for the LOL and HOLD flags in register 0x0013. If a mask bit is set the alarm will be blocked from causing an interrupt.

Table 12.119. 0x001A INCAL Mask

Reg Address	Bit Field	Type	Name	Description
0x001A	5	R/W	CAL_INTR_MSK	1 to mask the DSPLL internal calibration busy flag

The interrupt mask for this bit flag bit corresponds to register 0x0014.

Table 12.120. 0x001C Soft Reset and Calibration

Reg Address	Bit Field	Type	Name	Description
0x001C	0	S	SOFT_RST	1 Initialize and calibrates the entire device 0 No effect

These bits are of type “S”, which is self-clearing.

Table 12.121. 0x001D FINC, FDEC

Reg Address	Bit Field	Type	Name	Description
0x001D	0	S	FINC	1 a rising edge will cause the selected MultiSynth to increment the output frequency by the FstepW parameter. See registers 0x0339-0x0353 0 No effect
0x001D	1	S	FDEC	1 a rising edge will cause the selected MultiSynth to decrement the output frequency by the FstepW parameter. See registers 0x0339-0x03530 No effect

The figure below shows the logic for the FINC, FDEC bits.

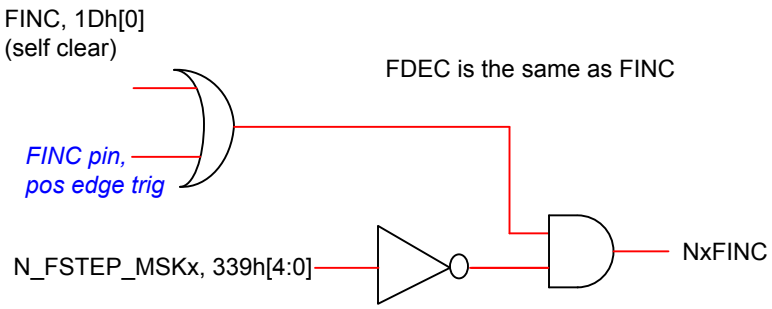

Figure 12.2. FINC, FDEC Logic Diagram

Table 12.122. 0x001E Sync, Power Down and Hard Reset

Reg Address	Bit Field	Type	Name	Description
0x001E	0	R/W	PDN	1 to put the device into low power mode
0x001E	1	S	HARD_RST	1 causes hard reset. The same as power up except that the serial port access is not held at reset. This does not self-clear, so after setting the bit it must be cleared. 0 No reset
0x001E	2	S	SYNC	Logically equivalent to asserting the SYNC pin. Resets all R dividers to the same state.

Table 12.123. 0x002B SPI 3 vs 4 Wire

Reg Address	Bit Field	Type	Name	Description
0x002B	3	R/W	SPI_3WIRE	0 for 4-wire SPI, 1 for 3-wire SPI

Table 12.124. 0x002C LOS Enable

Reg Address	Bit Field	Type	Name	Description
0x002C	1:0	R/W	LOS_EN	1 to enable LOS for a clock input; 0 for disable

Input 0 (IN0): LOS_EN[0]

Input 1 (IN1): LOS_EN[1]

Table 12.125. 0x002D Loss of Signal Re-Qualification Value

Reg Address	Bit Field	Type	Name	Description
0x002D	1:0	R/W	LOS0_VAL_TIME	Clock Input 0 0 for 2 msec 1 for 100 msec 2 for 200 msec 3 for one second
0x002D	3:2	R/W	LOS1_VAL_TIME	Clock Input 1, same as above

When an input clock disappears (and therefore has an active LOS alarm), if the clock returns, there is a period of time that the clock must be within the acceptable range before the alarm is removed. This is the LOS_VAL_TIME.

Table 12.126. 0x002E-0x002F LOS0 Trigger Threshold

Reg Address	Bit Field	Type	Name	Description
0x002E	7:0	R/W	LOS0_TRG_THR	16-bit Threshold Value
0x002F	15:8	R/W	LOS0_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 0, given a particular frequency plan.

Table 12.127. 0x0030-0x0031 LOS1 Trigger Threshold

Reg Address	Bit Field	Type	Name	Description
0x0030	7:0	R/W	LOS1_TRG_THR	16-bit Threshold Value
0x0031	15:8	R/W	LOS1_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 1, given a particular frequency plan.

Table 12.128. 0x0036-0x0037 LOS0 Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x0036	7:0	R/W	LOS0_CLR_THR	16-bit Threshold Value
0x0037	15:8	R/W	LOS0_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 0, given a particular frequency plan.

Table 12.129. 0x0038-0x0039 LOS1 Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x0038	7:0	R/W	LOS1_CLR_THR	16-bit Threshold Value
0x0039	15:8	R/W	LOS1_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 1, given a particular frequency plan.

Table 12.130. 0x003F OOF Enable

Reg Address	Bit Field	Type	Name	Description
0x003F	1:0	R/W	OOF_ENI	1 to enable, 0 to disable
0x003F	5:4	R/W	FAST_OOF_ENI	1 to enable, 0 to disable

Input 0 corresponds to OOF_ENI [0], FAST_OOF_ENI [4]

Input 1 corresponds to OOF_ENI [1], FAST_OOF_ENI [5]

Table 12.131. 0x0040 OOF Reference Select

Reg Address	Bit Field	Type	Name	Description
0x0040	2:0	R/W	OOF_REF_SEL	0 for CLKIN0 1 for CLKIN1 4 for XAXB

Table 12.132. 0x0046-0x0049 Out of Frequency Set Threshold

Reg Address	Bit Field	Type	Name	Description
0x0046	7:0	R/W	OOF0_SET_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm 255 = 510 ppm
0x0047	7:0	R/W	OOF1_SET_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm 255 = 510 ppm

These registers determine the OOF alarm set threshold for IN1 and IN0. The range is from ±2 ppm up to ±510 ppm in steps of 2 ppm.

Table 12.133. 0x004A-0x004D Out of Frequency Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x004A	7:0	R/W	OOF0_CLR_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm 255 = 510 ppm
0x004B	7:0	R/W	OOF1_CLR_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm 255 = 510 ppm

These registers determine the OOF alarm clear threshold for IN1 and IN0. The range is from ±2 ppm up to ±510 ppm in steps of 2 ppm. ClockBuilder Pro is used to determine the values for these registers.

Table 12.134. 0x0051-0x0054 Fast Out of Frequency Set Threshold

Reg Address	Bit Field	Type	Name	Description
0x0051	7:0	R/W	FAST_OOF0_SET_THR	(1+ value) x 1000 ppm
0x0052	7:0	R/W	FAST_OOF1_SET_THR	(1+ value) x 1000 ppm

These registers determine the OOF alarm set threshold for IN1 and IN0 when the fast control is enabled. The value in each of the register is (1+ value) x 1000 ppm. ClockBuilder Pro is used to determine the values for these registers.

Table 12.135. 0x0055-0x0058 Fast Out of Frequency Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x0055	7:0	R/W	FAST_OOF0_CLR_THR	(1+ value) x 1000 ppm
0x0056	7:0	R/W	FAST_OOF1_CLR_THR	(1+ value) x 1000 ppm

These registers determine the OOF alarm clear threshold for IN1 and IN0 when the fast control is enabled. The value in each of the register is (1+ value)*1000 ppm. ClockBuilder Pro is used to determine the values for these registers.

OOF needs a frequency reference. ClockBuilder Pro provides the OOF register values for a particular frequency plan.

Table 12.136. 0x009A LOL Enable

Reg Address	Bit Field	Type	Name	Description
0x009A	1	R/W	LOL_SLW_EN_PLL	1 to enable LOL; 0 to disable LOL.

ClockBuilder Pro provides the LOL register values for a particular frequency plan.

Table 12.137. 0x009E LOL Set Threshold

Reg Address	Bit Field	Type	Name	Description
0x009E	7:4	R/W	LOL_SET_THR	Configures the loss of lock set thresholds. Selectable as 0.2, 0.6, 2, 6, 20, 60, 200, 600, 2000, 6000, 20000. Values are in ppm. Default is 0.2 ppm.

The following are the thresholds for the value that is placed in the top four bits of register 0x009E.

0 = 0.2 ppm (default)

1 = 0.6 ppm

2 = 2 ppm

3 = 6 ppm

4 = 20 ppm

5 = 60 ppm

6 = 200 ppm

7 = 600 ppm

8 = 2000 ppm

9 = 6000 ppm

10 = 20000 ppm

Table 12.138. 0x00A0 LOL Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x00A0	7:4	R/W	LOL_CLR_THR	Configures the loss of lock clear thresholds. Selectable as 0.2, 0.6, 2, 6, 20, 60, 200, 600, 2000, 6000, 20000. Values in ppm. Default value is 2 ppm.

The following are the thresholds for the value that is placed in the top four bits of register 0x00A0. ClockBuilder Pro sets these values.

0 = 0.2 ppm

1 = 0.6 ppm

2 = 2 ppm

3 = 6 ppm

4 = 20 ppm

5 = 60 ppm

6 = 200 ppm

7 = 600 ppm

8 = 2000 ppm

9 = 6000 ppm

10 = 20000 ppm

Table 12.139. 0x00A2 LOL Timer Enable

Reg Address	Bit Field	Type	Name	Description
0x00A2	1	R/W	LOL_TIMER_EN	0 to disable 1 to enable

LOL_TIMER_EN extends the time after LOL negates that the clock outputs can be disabled by LOL_CLR_DELAY (see below).

Table 12.140. 0x00A8-0x00AC LOL Clear Delay

Reg Address	Bit Field	Type	Name	Description
0x00A8	7:0	R/W	LOL_CLR_DELAY	35-bit value
0x00A9	15:8	R/W	LOL_CLR_DELAY	
0x00AA	23:16	R/W	LOL_CLR_DELAY	
0x00AB	31:24	R/W	LOL_CLR_DELAY	
0x00AC	34:32	R/W	LOL_CLR_DELAY	

The LOL Clear Delay value is set by ClockBuilder Pro.

Table 12.141. 0x00E2

Reg Address	Bit Field	Type	Name	Description
0x00E2	7:0	R	ACTIVE_NVM_BANK	Read-only field indicating number of user bank writes carried out so far. Value Description 0 zero 3 one 15 two 63 three

Table 12.142. 0x00E3

Reg Address	Bit Field	Type	Name	Description
0x00E3	7:0	R/W	NVM_WRITE	Write 0xC7 to initiate an NVM bank burn.

See 3.3 NVM Programming.

Table 12.143. 0x00E34

Reg Address	Bit Field	Type	Name	Description
0x00E4	0	S	NVM_READ_BANK	1 to download NVM.

When set, this bit will read the NVM down into the volatile memory.

Table 12.144. 0x00FE Device Ready

Reg Address	Bit Field	Type	Name	Description
0x00FE	7:0	R	DEVICE_READY	0x0F when device is ready 0xF3 when device is not ready

Read-only byte to indicate when the device is ready to accept serial bus writes. The user can poll this byte starting at power-on; when DEVICE_READY is 0x0F the user can safely read or write to any other register. This is only needed after power up or after a hard reset using register bit 0x001E[1] or during a bank burn (register 0x0-E3). The “Device Ready” register is available on every page in the device at the second last register, 0xFE. There is a device ready register at 0x00FE, 0x01FE, 0x02FE, … etc.

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Table 12.145. 0x0102 Global OE Gating for all Clock Output Drivers

Reg Address	Bit Field	Type	Name	Description
0x0102	0	R/W	OUTALL_DISABLE_LOW	1 Pass through the output enables, 0 disables all output drivers

Table 12.146. 0x0112 Clock Output Driver 0 and R-Divider 0 Configuration

Reg Address	Bit Field	Type	Name	Description
0x0112	0	R/W	OUT0_PDN	Output driver 0: 0 to power up the regulator, 1 to power down the regulator. Clock outputs will be weakly pulled-low.
0x0112	1	R/W	OUT0_OE	Output driver 0: 0 to disable the output, 1 to enable the output
0x0112	2	R/W	OUT0_RDIV_FORCE2	0 R0 divider value is set by R0_REG 1 R0 divider value is forced into divide by 2

Table 12.147. 0x0113 Output 0 Format

Reg Address	Bit Field	Type	Name	Description
0x0113	2:0	R/W	OUT0_FORMAT	0 Reserved 1 swing mode (normal swing) differential 2 swing mode (high swing) differential 3 rail to rail swing mode differential 4 LVCMOS single ended 5–7 reserved
0x0113	3	R/W	OUT0_SYNC_EN	0 disable 1 enable Enable/disable synchronized (glitchless) operation. When enabled, the power down and output enables are synchronized to the output clock.
0x0113	5:4	R/W	OUT0_DIS_STATE	Determines the state of an output driver when disabled, selectable as Disable low (0), Disable high (1), High impedance. (2) In high-impedance mode the differential driver will output the common mode voltage and no signal.
0x0113	7:6	R/W	OUT0_CMOS_DRV	LVCMOS output impedance. Selectable as CMOS1,CMOS2, CMOS3.

See 5.2 Performance Guidelines for Outputs.

Table 12.148. 0x0114 Output 0 Swing and Amplitude

Reg Address	Bit Field	Type	Name	Description
0x0114	3:0	R/W	OUT0_CM	Output common mode voltage adjustment Programmable swing mode with normal swing configuration: Step size = 100 mV Range = 0.9 V to 2.3 V if VDDO = 3.3 V Range = 0.6 V to 1.5V if VDDO=2.5 V Range = 0.5 V to 0.9V if VDDO=1.8 V Programmable swing mode with high0 swing configuration: Step size = 100 mV Range = 0.9 V to 2.3 V if VDDO = 3.3 V Range = 0.6 V to 1.5 V if VDDO = 2.5 V Range = 0.5 V to 0.9 V if VDDO = 1.8 V Rail-to-rail swing Mode configuration: No flexibility DRV0_CM = 6 if VDDO = 3.3 V (Vcm = 1.5 V) DRV0_CM = 10 if VDDO = 2.5 V (Vcm = 1.1 V) DRV0_CM = 13 if VDDO = 1.8 V (Vcm = 0.8 V) LVCMOS mode: Not supported/No effect
0x0114	6:4	R/W	OUT0_AMPL	Output swing adjustment Programmable swing mode with normal swing configuration: Step size = 100 mV Range = 100 mVpp-se to 800 mVpp-se Programmable swing mode with high swing configuration: Step size = 200 mV Range = 200 mVpp-se to 1600 mVpp-se Rail-to-rail swing mode: Not supported/No effect LVCMOS mode: Not supported/No effect

See the settings and values from Table 5.10 Settings for LVDS, LVPECL, and HCSL on page 34 for details of the settings. ClockBuilder Pro is used to select the correct settings for this register.

Table 12.149. 0x0115 R-Divider 0 Mux Selection

Reg Address	Bit Field	Type	Name	Description
0x0115	1:0	R/W	OUT0_MUX_SEL	Output driver 0 input mux select.This selects the source of the multisynth. 0: N0 1: N1 2: reserved 3: reserved 4: reserved 5: reserved 6: reserved 7: reserved
0x0115	7:6	R/W	OUT0_INV	CLK and CLK not inverted CLK inverted CLK and CLK inverted CLK inverted

Each output can be configured to use Multisynth N0-N1 divider. The frequency for each N-divider is set in registers 0x0302–0x0316 for N0 to N1. Two different frequencies can be set in the N-dividers (N0–N1) and each of the 2 outputs can be configured to any of the 2 different frequencies.

The 2 output drivers are all identical. The single set of descriptions above for output driver 0 applies to the other output driver.

Table 12.150. Registers that Follow the Same Definition as Above

Register Address	Description	(Same as) Address
0x0117	Clock Output Driver 1 Config	0x0112
0x0118	Clock Output Driver 1 Format, Sync	0x0113
0x0119	Clock Output Driver 1 Ampl, CM	0x0114
0x011A	OUT1_MUX_SEL, OUT1_INV	0x0115

Table 12.151. 0x0145 Power Down All

Reg Address	Bit Field	Type	Name	Description
0x0145	0	R/W	OUT_PDN_ALL	0- no effect 1- all drivers powered down

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Table 12.152. 0x0202-0x0205 XAXB Frequency Adjust

Reg Address	Bit Field	Type	Name	Description
0x0202	7:0	R/W	XAXB_FREQ_OFFSET	32 bit offset adjustment
0x0203	15:8	R/W	XAXB_FREQ_OFFSET	
0x0204	23:16	R/W	XAXB_FREQ_OFFSET	
0x0205	31:24	R/W	XAXB_FREQ_OFFSET	

The clock that is present on XAXB pins is used to create an internal frequency reference for the PLL. The XAXB_FREQ_OFFSET word is used to adjust this frequency reference with high resolution. ClockBuilder Pro calculates the correct values for these registers.

Table 12.153. 0x0206 Pre-scale Reference Divide Ratio

Reg Address	Bit Field	Type	Name	Description
0x0206	1:0	R/W	PXAXB	Sets the prescale divider for the input clock on XAXB.

This can only be used with an external clock source, not with crystals.

0 = pre-scale value 1

1 = pre-scale value 2

2 = pre-scale value 4

3 = pre-scale value 8

Table 12.154. 0x0208-0x020D P0 Divider Numerator

Reg Address	Bit Field	Type	Name	Description
0x0208	7:0	R/W	P0_NUM	48-bit Integer Number
0x0209	15:8	R/W	P0_NUM	
0x020A	23:16	R/W	P0_NUM	
0x020B	31:24	R/W	P0_NUM	
0x020C	39:32	R/W	P0_NUM	
0x020D	47:40	R/W	P0_NUM	

This set of registers configure the P-dividers which are located at the two input clocks seen in Figure 2.1 Si5342H DSPLL and Multi-synth System Flow Diagram on page 7. ClockBuilder Pro calculates the correct values for the P-dividers.

Table 12.155. 0x020E-0x0211 P0 Divider Denominator

Reg Address	Bit Field	Type	Name	Description
0x020E	7:0	R/W	P0_DEN	32-bit Integer Number
0x020F	15:8	R/W	P0_DEN	
0x0210	23:16	R/W	P0_DEN	
0x0211	31:24	R/W	P0_DEN	

The P1 divider numerator and denominator follow the same format as P0 described above. ClockBuilder Pro calculates the correct values for the P-dividers.

Table 12.156. Registers that Follow the P0_NUM and P0_DEN Definitions

Register Address	Description	Size	Same as Address
0x0212-0x0217	P1 Divider Numerator	48-bit Integer Number	0x0208-0x020D
0x0218-0x021B	P1 Divider Denominator	32-bit Integer Number	0x020E-0x0211

This set of registers configure the P-dividers which are located at the two input clocks seen in Figure 2.1 Si5342H DSPLL and Multisynth System Flow Diagram on page 7. ClockBuilder Pro calculates the correct values for the P-dividers.

Table 12.157. 0x024A-0x024C R0 Divider

Reg Address	Bit Field	Type	Name	Description
0x024A	7:0	R/W	R0_REG	A 24 bit integer divider. Divide value = (R0_REG+1) x 2 To set R0 = 2, set OUT0_RDIV_FORCE2 = 1, and then the R0_REG value is irrelevant.
0x024B	15:8	R/W	R0_REG	
0x024C	23:16	R/W	R0_REG	

The R dividers are at the output clocks and are purely integer division. The R1divider follow the same format as the R0 divider described above.

Table 12.158. Registers that Follow the R0_REG

Register Address	Description	Size	Same as Address
0x024D-0x024F	R1 Divider	24-bit Integer Number	0x024A-0x024C

Table 12.159. 0x026B-0x0272 User Scratch Pad

Reg Address	Bit Field	Type	Name	Description
0x026B	7:0	R/W	DESIGN_ID0	ASCII encoded string defined by CBPro user, with user defined space or null padding of unused characters. A user will normally include a configuration ID + revision ID. For example, “ULT.1A” with null character padding sets: DESIGN_ID0: 0x55 DESIGN_ID1: 0x4C DESIGN_ID2: 0x54 DESIGN_ID3: 0x2E DESIGN_ID4: 0x31 DESIGN_ID5: 0x41 DESIGN_ID6:0x 00 DESIGN_ID7: 0x00
0x026C	15:8	R/W	DESIGN_ID1	
0x026D	23:16	R/W	DESIGN_ID2	
0x026E	31:24	R/W	DESIGN_ID3	
0x026F	39:32	R/W	DESIGN_ID4	
0x0270	47:40	R/W	DESIGN_ID5	
0x0271	55:48	R/W	DESIGN_ID6	
0x0272	63:56	R/W	DESIGN_ID7	

Table 12.160. 0x0278-0x027C OPN Identifier

Reg Address	Bit Field	Type	Name	Description
0x0278	7:0	R/W	OPN_ID0	OPN unique identifier. ASCII encoded. For example, with OPN: Si5342H-C12345-GM, 12345 is the OPN unique identifier, which sets: OPN_ID0: 0x31 OPN_ID1: 0x32 OPN_ID2: 0x33 OPN_ID3: 0x34 OPN_ID4: 0x35
0x0279	15:8	R/W	OPN_ID1	
0x027A	23:16	R/W	OPN_ID2	
0x027B	31:24	R/W	OPN_ID3	
0x027C	39:32	R/W	OPN_ID4	

Part numbers are of the form:

Si<Part Num Base><Grade>-<Device Revision><OPN ID>-<Temp Grade><Package ID>

Examples:

Si5342H-C12345-GM.

Applies to a “custom” OPN (Ordering Part Number) device. These devices are factory pre-programmed with the frequency plan and all other operating characteristics defined by the user’s ClockBuilder Pro project file.

Si5342H-C-GM.

Applies to a “base” or “non-custom” OPN device. Base devices are factory pre-programmed to a specific base part type (e.g., Si5342H but exclude any user-defined frequency plan or other user-defined operating characteristics selected in ClockBuilder Pro.

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Table 12.161. 0x0302-0x0307 N0 Numerator

Reg Address	Bit Field	Type	Name	Description
0x0302	7:0	R/W	N0_NUM	44-bit Integer Number
0x0303	15:8	R/W	N0_NUM	
0x0304	23:16	R/W	N0_NUM	
0x0305	31:24	R/W	N0_NUM	
0x0306	39:32	R/W	N0_NUM	
0x0307	43:40	R/W	N0_NUM	

The N dividers are interpolative dividers that are used as output dividers that feed into the R dividers. ClockBuilder Pro calculates the correct values for the N-dividers.

Table 12.162. 0x0308-0x030B N0 Denominator

Reg Address	Bit Field	Type	Name	Description
0x0308	7:0	R/W	N0_DEN	32-bit Integer Number
0x0309	15:8	R/W	N0_DEN	
0x030A	23:16	R/W	N0_DEN	
0x030B	31:24	R/W	N0_DEN	

Table 12.163. 0x0338

Reg Address	Bit Field	Type	Name	Description
0x030C	0	R/W	N0_UPDATE	Set this bit to update the N0 divider

This bit is provided so that all of the N0 divider bits can be changed at the same time. First, write all of the new values to the divider, then set the update bit.

Table 12.164. Register that Follows the N0_NUM and N0_DEN Definitions

Register Address	Description	Size	Same as Address
0x030D-0x0312	N1 Numerator	44-bit Integer Number	0x0302-0x0307
0x0313-0x0316	N1 Denominator	32-bit Integer Number	0x0308-0x030B

Table 12.165. 0x03017

Reg Address	Bit Field	Type	Name	Description
0x03017	0	R/W	N1_UPDATE	Set this bit to update the N1 divider

This bit is provided so that all of the N1 divider bits can be changed at the same time. First, write all of the new values to the divider, then set the update bit.

Table 12.166. 0x0338 Global N Divider Update

Reg Address	Bit Field	Type	Name	Description
0x0338	1	R/W	N_UPDATE_ALL	Set this bit to update both N dividers

This bit is provided so that both of the N dividers can be changed at the same time. First, write all of the new values to the divider, then set the update bit.

Table 12.167. 0x0339 FINC/FDEC Masks

Reg Address	Bit Field	Type	Name	Description
0x0339	1:0	R/W	N_FSTEP_MSK	0 to enable FINC/FDEC updates 1 to disable FINC/FDEC updates

Bit 0 corresponds to MultiSynth N0 N_FSTEP_MSK 0x0339[0]

Bit 1 corresponds to MultiSynth N1 N_FSTEP_MSK 0x0339[1]

Table 12.168. 0x033B-0x0340 N0 Frequency Step Word

Reg Address	Bit Field	Type	Name	Description
0x033B	7:0	R/W	N0_FSTEPW	44-bit Integer Number
0x033C	15:8	R/W	N0_FSTEPW	
0x033D	23:16	R/W	N0_FSTEPW	
0x033E	31:24	R/W	N0_ FSTEPW	
0x033F	39:32	R/W	N0_ FSTEPW	
0x0340	43:40	R/W	N0_ FSTEPW	

This is a 44-bit integer value which is directly added or subtracted from the N-divider. ClockBuilder Pro calculates the correct values for the N0 Frequency Step Word. Each N divider has the ability to add or subtract up to a 44-bit value. Changing any of the Nx_DELAY values requires a SOFT_RST, a HARD_RST, or a power up sequence.

Table 12.169. Registers that Follow the N0_FSTEPW Definition

Register Address	Description	Size	Same as Address
0x0341-0x0346	N1 Frequency Step Word	44-bit Integer Number	0x033B-0x0340

Table 12.170. 0x0359–0x035A N0 Delay Control

Reg Address	Bit Field	Type	Name	Description
0x0359	7:0	R/W	N0_DELAY[7:0]	8-bit Integer delay portion
0x035A	7:0	R/W	N0_DELAY[7:0]	Upper byte of N0_DELAY[15:0]

Nx_DELAY[15:0] is a 2s complement number that sets the output delay of MultiSynthx.

The delay in seconds is Nx_DELAY/(256 x Fvco) where Fvco is the VCO frequency in Hz. The maximum positive and negative delay is ±(215– 1)/(256 x Fvco). ClockBuilder Pro calculates the correct value for this register. Changing any of the Nx_DELAY values requires a SOFT_RST, a HARD_RST, or a power up sequence.

Table 12.171. Registers that Follow the N0_DELAY Definition

Register Address	Description	Size	Same as Address
0x035B	N1 Delay Integer	8-bit Integer Number	0x0359
0x035C	N1 Delay Fractional	8-bit Integer Number	0x035A

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Table 12.172. 0x0507

Reg Address	Bit Field	Type	Name	Description
0x0507	7,6	R	IN_ACTV	Current input clock.

These bits indicate which input clock is currently selected. 0 for IN0, 1 for IN1, etc.

Table 12.173. 0x0508-0x050D Loop Bandwidth

Reg Address	Bit Field	Type	Name	Description
0x0508	7:0	R/W	BW0_PLL	PLL bandwidth parameter
0x0509	15:8	R/W	BW1_PLL	PLL bandwidth parameter
0x050A	23:16	R/W	BW2_PLL	PLL bandwidth parameter
0x050B	31:24	R/W	BW3_PLL	PLL bandwidth parameter
0x050C	39:32	R/W	BW4_PLL	PLL bandwidth parameter
0x050D	47:40	R/W	BW5_PLL	PLL bandwidth parameter

This group of registers determine the loop bandwidth for the DSPLL. It is selectable as 0.1 Hz, 1 Hz, 4 Hz, 10 Hz, 40 Hz, 100 Hz, 400 Hz, 1 kHz, and 4 kHz. The loop BW values are calculated by ClockBuilder Pro and are written into these registers. The BW_UPDATE_PLL bit (reg 0x0514[0]) must be set to cause the BWx_PLL parameters to take effect.

Table 12.174. 0x050E-0x0514 Fast Lock Loop Bandwidth

Reg Address	Bit Field	Type	Name	Description
0x050E	7:0	R/W	FAST_BW0_PLL	PLL fast bandwidth parameter
0x050F	15:8	R/W	FAST_BW1_PLL	PLL fast bandwidth parameter
0x0510	23:16	R/W	FAST_BW2_PLL	PLL fast bandwidth parameter
0x0511	31:24	R/W	FAST_BW3_PLL	PLL fast bandwidth parameter
0x0512	39:32	R/W	FAST_BW4_PLL	PLL fast bandwidth parameter
0x0513	47:40	R/W	FAST_BW5_PLL	PLL fast bandwidth parameter
0x0514	0	S	BW_UPDATE_PLL	Must be set to 1 to update the BWx_PLL and FAST_BWx_PLL parameters

The fast lock loop BW values are calculated by ClockBuilder Pro and used when fast lock is enabled.

Table 12.175. 0x0515-0x051B M Divider Numerator, 56-bits

Reg Address	Bit Field	Type	Name	Description
0x0515	7:0	R/W	M_NUM	56-bit Number
0x0516	15:8	R/W	M_NUM	
0x0517	23:16	R/W	M_NUM	
0x0518	31:24	R/W	M_NUM	
0x0519	39:32	R/W	M_NUM	
0x051A	47:40	R/W	M_NUM	
0x051B	55:48	R/W	M_NUM	

Table 12.176. 0x051C-0x051F M Divider Denominator, 32-bits

Reg Address	Bit Field	Type	Name	Description
0x051C	7:0	R/W	M_DEN	32-bit Number
0x051E	15:8	R/W	M_DEN	
0x051E	23:16	R/W	M_DEN	
0x051F	31:24	R/W	M_DEN	

The loop M divider values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 12.177. 0x0520 M Divider Update Bit

Reg Address	Bit Field	Type	Name	Description
0x0520	0	R/W	M_UPDATE	Set this bit to update the M divider.

Table 12.178. 0x052A Input Clock Select

Reg Address	Bit Field	Type	Name	Description
0x052A	0	R/W	IN_SEL_REGCTRL	0 for pin controlled clock selection 1 for register controlled clock selection
0x052A	1	R/W	IN_SEL	0 for IN0, 1 for IN1

Input clock selection for manual register based and pin controlled clock selection.

Note: When IN_SEL_REGCTRL is low, IN_SEL does not do anything and the clock selection is pin controlled.

Table 12.179. 0x052B Fast Lock Control

Reg Address	Bit Field	Type	Name	Description
0x052B	0	R/W	FASTLOCK_AUTO_EN	Applies only when FASTLOCK_MAN = 0 (see below): 0 to enable auto fast lock when the DSPLL is out of lock 1 to disable auto fast lock

Reg Address	Bit Field	Type	Name	Description
0x052B	1	R/W	FASTLOCK_MAN	0 for normal operation (see above) 1 to force fast lock

When in fast lock, the fast lock loop BW can be automatically used.

Table 12.180. 0x052C Holdover Exit Control

Reg Address	Bit Field	Type	Name	Description
0x052C	3	R/W	HOLD_RAMP_BYP	Must be set to 1 for normal operation.
0x052C	4	R/W	HOLD_EXIT_BW_SEL	0 to use the fastlock loop BW when exiting from holdover 1 to use the normal loop BW when exiting from holdover

Table 12.181. 0x052E Holdover History Average Length

Reg Address	Bit Field	Type	Name	Description
0x052E	4:0	R/W	HOLD_HIST_LEN	5-bit value

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency.

Table 12.182. 0x052F Holdover History Delay

Reg Address	Bit Field	Type	Name	Description
0x052F	4:0	R/W	HOLD_HIST_DELAY	

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushes back into the past, above the averaging window. The amount that the average window is delayed is the holdover history delay.

Table 12.183. 0x0535 Force Holdover

Reg Address	Bit Field	Type	Name	Description
0x0535	0	R/W	FORCE_HOLD	0 for normal operation 1 for force holdover

Table 12.184. 0x0536 Input Clock Switching Control

Reg Address	Bit Field	Type	Name	Description
0x0536	1:0	R/W	CLK_SWTCH_MODE	0 = manual 1 = automatic/non-revertive 2 = automatic/revertive 3 = reserved
0x0536	2	R/W	HSW_EN	0 glitchless switching mode (phase buildout turned off) 1 hitless switching mode (phase buildout turned on)

Table 12.185. 0x0537 Input Alarm Masks

Reg Address	Bit Field	Type	Name	Description
0x0537	3:0	R/W	IN_LOS_MSK	For each clock input LOS alarm: 0 to use LOS in the clock selection logic 1 to mask LOS from the clock selection logic
0x0537	7:4	R/W	IN_OOF_MSK	For each clock input OOF alarm: 0 to use OOF in the clock selection logic 1 to mask OOF from the clock selection logic

This register is for the input clock switch alarm masks. For each of the two clock inputs, the OOF and/or the LOS alarms can be used for the clock selection logic or they can be masked from it. Note that the clock selection logic can affect entry into holdover.

Table 12.186. 0x0538 Clock Inputs 0 and 1 Priority

Reg Address	Bit Field	Type	Name	Description
0x0538	2:0	R/W	IN0_PRIORITY	The priority for clock input 0 is: 0 for clock input not selectable 1 for priority 1 2 for priority 2 3 to 7 are reserved
0x0538	6:4	R/W	IN1_PRIORITY	The priority for clock input 1 is: 0 for clock input not selectable 1 for priority 1 2 for priority 2 3 to 7 are reserved

This register is used to assign a priority to an input clock for automatic clock input switching. The available clock with the lowest priority level will be selected. When input clocks are assigned the same priority, they will use the following default priority list: 0, 1.

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Table 12.187. 0x090E XAXB Configuration

Reg Address	Bit Field	Type	Name	Description
0x090E	0	R/W	XAXB_EXTCLK_EN	0 to use a crystal at the XAXB pins 1 to use an external clock source at the XAXB pins

Table 12.188. 0x0943 Control I/O Voltage Select

Reg Address	Bit Field	Type	Name	Description
0x0943	0	R/W	IO_VDD_SEL	0 for 1.8 V external connections 1 for 3.3 V external connections

The IO_VDD_SEL configuration bit selects the option of operating the serial interface voltage thresholds from the VDD or the VDDA pin. The serial interface pins are always 3.3 V tolerant even when the device's VDD pin is supplied from a 1.8 V source. When the I^2C or SPI host is operating at 3.3 V and the Si5344H/42H at VDD = 1.8 V, the host must write the IO_VDD_SEL configuration bit to the VDDA option. This will ensure that both the host and the serial interface are operating at the optimum voltage thresholds.

Table 12.189. 0x0949 Clock Input Control and Configuration

Reg Address	Bit Field	Type	Name	Description
0x0949	1:0	R/W	IN_EN	0: Disable and Powerdown Input Buffer. 1: Enable Input Buffer for IN1, IN0.
0x0949	5:4	R/W	IN_PULSED_CMOS_EN	0: Standard Input Format. 1: Pulsed CMOS Input Format for IN1, IN0. See 4. Clock Inputs for more information.

When a clock input is disabled, it is powered down.

Input 0 corresponds to IN_SEL 0x0949 [0], IN_PULSED_CMOS_EN 0x0949 [4]

Input 1 corresponds to IN_SEL 0x0949 [1], IN_PULSED_CMOS_EN 0x0949 [5]

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Table 12.190. 0x0A03 Output Multisynth Clock to Output Driver

Reg Address	Bit Field	Type	Name	Description
0x0A03	1:0	R/W	N_CLK_TO_OUTX_EN	Routes Multisynth outputs to output driver muxes.

Table 12.191. 0x0A04 Output Multisynth Integer Divide Mode

Reg Address	Bit Field	Type	Name	Description
0x0A04	1:0	R/W	N_PIBYP	Output Multisynth integer divide mode. Bit 0 for ID0, Bit 1 for ID1, etc. 0: Nx divider is fractional. 1: Nx divider is integer.

Table 12.192. 0x0A05 Output Multisynth Divider Power Down

Reg Address	Bit Field	Type	Name	Description
0x0A05	1:0	R/W	N_PDNB	Powers down the N dividers. Set to 0 to power down unused N dividers. Must set to 1 for all active N dividers. See also related registers 0x0A03 and 0x0B4A.

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Table 12.193. 0x0B44 Output Multisynth Clock to Output Driver

Reg Address	Bit Field	Type	Name	Description
0x0B44	3:0	R/W	PDIV_FRACN_CLK_DIS	Disable digital clocks to input P (IN0–3) fractional dividers.
0x0B44	5	R/W	FRACN_CLK_DIS_PLL	Disable digital clock to M fractional divider.

Table 12.194. 0x0B4A Divider Clock Disables

Reg Address	Bit Field	Type	Name	Description
0x0B4A	1:0	R/W	N_CLK_DIS	Disable digital clocks to N dividers. Must be set to 0 to use each N divider. See also related registers 0x0A03 and 0x0A05.

13. Appendix A—Setting the Differential Output Driver to Non-Standard Amplitudes

In some applications it may be desirable to have larger or smaller differential amplitudes than produced by the standard LVPECL and LVDS settings, as selected by CBPro. In these cases, the following information describes how to implement these amplitudes by writing to the OUTx_CM and OUTx_AMPL setting names. Contact Silicon Labs for assistance if you want your custom configured device to be programmed for any of the settings in this appendix.

The differential output driver has a variable output amplitude capability and 2 basic formats, normal and low power format. The difference between these two formats is that the normal format has an output impedance of ~100 ohms differential and the low power format has an output impedance of > 500 ohms differential. Note that the rise/fall time is slower when using the Low Power Differential Format. See the Si5344H/42H data sheet for the rise/fall time specifications.

If the standard LVDS or LVPECL compatible output amplitudes will not work for a particular application, the variable amplitude capability can be used to achieve higher or lower amplitudes. For example, a “CML” format is sometimes desired for an application. However, CML is not a defined standard and hence the amplitude of a CML signal for one receiver may be different than that of another receiver.

When the output amplitude needs to be different than standard LVDS or LVPECL, the Common Mode Voltage settings must be set as shown in Table 13.1 Output Differential Common Mode Voltage Settings on page 109. No settings other than the ones in the table below are supported as the signal integrity could be compromised. In addition the output driver should be AC coupled to the load so that the common mode voltage of the driver is not affected by the load.

Table 13.1. Output Differential Common Mode Voltage Settings

VDDOx (Volts)	Differential Format	OUTx_FORMAT	Common Mode Voltage (Volts)	OUTx_CM
3.3	Normal	0x1	2.0	0xB
3.3	Low Power	0x2	1.6	0x7
2.5	Normal	0x1	1.3	0xC
2.5	Low Power	0x2	1.1	0xA
1.8	Normal	0x1	0.8	0xD
1.8	Low Power	0x2	0.8	0xD

The differential amplitude can be set as shown in the table below.

Table 13.2. Typical Differential Amplitudes

OUTx_AMPL	Normal Differential Format (Vpp SE mV–Typical)	Low Power Differential Format (Vpp SE mV – Typical)
0	130	200
1	230	400
2	350	620
3	450	820
4	575	1010
5	700	1200
6	810	1350[1]
7	920	1600[1]

Notes:
1. In low power mode and VDDOx=1.8V, OUTx_AMPL may not be set to 6 or 7.
2. These amplitudes are based upon a 100 Ω differential termination.

See the register map portion of this document for additional information about OUTx_FORMAT, OUTx_CM and OUTx_AMPL. Contact Silicon Labs for assistance at https://www.silabs.com/support/pages/contacttechnicalsupport.aspx if you require a factory-programmed device to be configured for any of the output driver settings in this appendix.

14. Document Change List

14.1 Revision 0.9

January 25, 2016

- Initial release.

14.2 Revision 1.0

May 24, 2017

- Updated content of Section “4.2. Dynamic PLL Changes”.
- Added a warning note after Table 5.
- Combined and replaced content in former Sections 10.2 and 10.3.

14.3 Revision 1.1

June 28, 2017

- Updated document to current style guide.

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