NETWORKING CLOCK SOURCE

ICS650-07C

Description

The ICS650-07C is a low cost, low jitter, high performance clock synthesizer for networking applications. Using analog Phase-Locked Loop (PLL) techniques, the device accepts a 12.5 MHz or 25.00 MHz clock or fundamental mode crystal input to produce multiple output clocks for networking chips, PCI devices, SDRAM, and ASICs. The ICS650-07C outputs all have 0 ppm synthesis error.

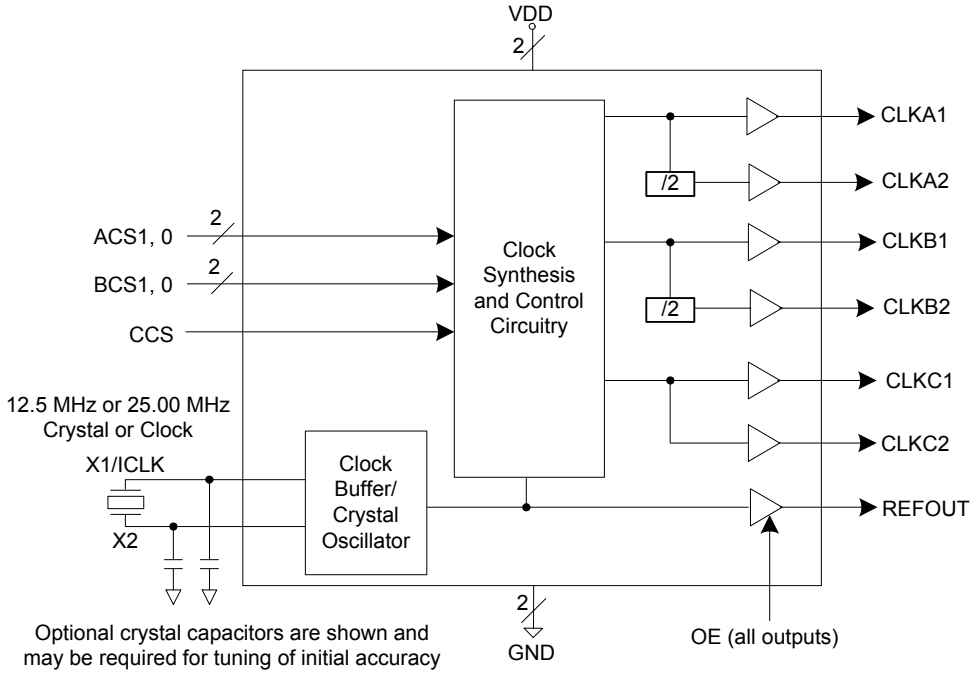
See the MK74CB214, ICS551, and ICS552-01 for non-PLL buffer devices which produce multiple low-skew copies of these output clocks.

See the ICS570, ICS9112-16/17/18 for zero delay buffers that can synchronize outputs and other needed clocks.

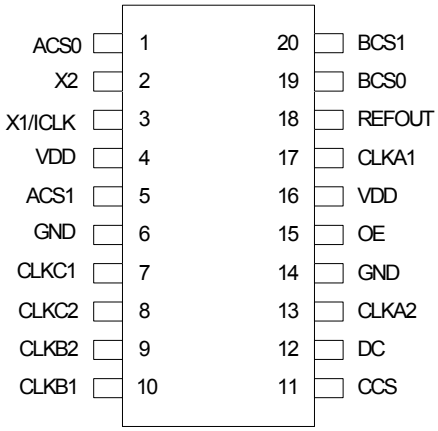
Features

- Packaged in 20-pin tiny SSOP (QSOP)
- Pb (lead) free package
- 12.5 MHz or 25.00 MHz fundamental crystal or clock input
- Six output clocks with selectable frequencies
- SDRAM frequencies of 67, 83, 100, and 133 MHz
- Buffered crystal reference output
- Zero ppm synthesis error in all clocks
- Ideal for PMC-Sierra's ATM switch chips
- Full CMOS output swing with 25 mA output drive capability at TTL levels
- Advanced, low power, sub-micron CMOS process
- 3.0 V to 5.5 V operating voltage

Block Diagram



Pin Assignment



20 pin (150 mil) SSOP

Pin Descriptions

Pin	Name	Pin Type	Description
1	ACS0	Tri-level Input	A clock select 0. Selects outputs on CLKA1 and CLKA2. See table below.
2	X2	XO	Crystal connection. Connect to a crystal or leave unconnected for clock input.
3	X1/ICLK	XI	Crystal connection. Connect to fundamental crystal or clock input.
4	VDD	Power	Connect to 3.3 V or 5 V. Must be same value as other VDD.
5	ACS1	Input	A clock select 1. Selects outputs on CLKA1 and CLKA2. Internal pull-up resistor. See table below.
6	GND	Power	Connect to ground.
7	CLKC1	Output	Clock C output 1. Depends on setting of CCS per table below.
8	CLKC2	Output	Clock C output 2. Depends on setting of CCS per table below. Same as CLKC1.
9	CLKB2	Output	Clock B output 2. Depends on setting of BCS1, 0 per table below.
10	CLKB1	Output	Clock B output 1. Depends on setting of BCS1, 0 per table below.
11	CCS	Tri-level Input	Clock C Select pin. Selects outputs on CLKC1 and CLKC2 per table below.
12	DC	—	Don't Connect. Do not connect anything to this pin.
13	CLKA2	Output	Clock A output 2. Depends on setting of ACS1, 0 per table below.
14	GND	Power	Connect to ground.
15	OE	Input	Output enable. Tri-states all outputs when low. Internal pull-up resistor.
16	VDD	Power	Connect to VDD. Must be same value as other VDD.
17	CLKA1	Output	Clock A output 1. Depends on setting of ACS1, 0 per table below.
18	REFOUT	Output	Buffered reference clock output. Same frequency as crystal or clock input.
19	BCS0	Tri-level Input	B clock select 0. Selects outputs on CLKB1 and CLKB2. See table below.
20	BCS1	Input	B clock select 1. Selects outputs on CLKB1 and CLKB2. See table below.

For a 25 MHz Fundamental Crystal or Clock Input, use the following tables:

A Clocks Select Table (MHz)

ACS1	ACS0	CLKA1	CLKA2
0	0	100	OFF (low)
0	M	TEST	TEST
0	1	75	OFF (low)
1	0	33.3333	16.6667
1	M	TEST	TEST
1	1	66.6667	33.3333

B Clocks Select Table (MHz)

BCS1	BCS0	CLKB1	CLKB2
0	0	TEST	TEST
0	M	66.6667	33.3333
0	1	100	50
1	0	83.3333	41.6667
1	M	TEST	TEST
1	1	133.3333	66.6667

REFOUT = 25 MHz

C Clocks Select Table (MHz)

CCS	CLKC1	CLKC2
0	125	125
M	TEST	TEST
1	75	75

0 = connect directly to ground

1 = connect directly to VDD

M = leave unconnected (automatically self biases to VDD/2)

For a 12.5 MHz Crystal or Clock Input, use the following tables:

A Clocks Select Table (MHz)

ACS1	ACS0	CLKA1	CLKA2
0	0	50	OFF (low)
0	M	TEST	TEST
0	1	37.5	OFF (low)
1	0	16.6667	8.3333
1	M	TEST	TEST
1	1	33.3333	16.6667

B Clocks Select Table (MHz)

BCS1	BCS0	CLKB1	CLKB2
0	0	TEST	TEST
0	M	33.3333	16.6667
0	1	50	25
1	0	41.66667	20.8333
1	M	TEST	TEST
1	1	66.6667	33.3333

REFOUT = 12.5 MHz

C Clocks Select Table (MHz)

CCS	CLKC1	CLKC2
0	62.5	62.5
M	TEST	TEST
1	37.5	37.5

0 = connect directly to ground

1 = connect directly to VDD

M = leave unconnected (automatically self biases to VDD/2)

External Components

The ICS650-07C requires a minimum number of external components for proper operation.

Decoupling Capacitor

Decoupling capacitors of 0.01µF must be connected between each VDD and GND (pins 4 and 6, pins 16 and 14), as close to the device as possible. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

Series Termination Resistor

When the PCB trace between the clock outputs and the loads are over 1 inch, series termination should be used. To series terminate a 50Ω trace (a commonly used trace impedance) place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

Crystal Information

The crystal used should be a fundamental mode (do not use third overtone), parallel resonant. Crystal capacitors should be connected from pins X1 to ground and X2 to ground to optimize the initial accuracy. The value of these capacitors is given by the following equation:

$$\text{Crystal caps (pF)} = (C_L - 6) \times 2$$

In the equation, C_L is the crystal load capacitance. So, for a crystal with a 16 pF load capacitance, two 20 pF capacitors should be used. If a clock input is used, drive it into X1 and leave X2 unconnected.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS650-07C. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature (commercial)	0 to +70° C
Ambient Operating Temperature (industrial)	-40 to +85° C
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature (20 seconds max)	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (commercial)	0		+70	° C
Ambient Operating Temperature (industrial)	-40		+85	° C
Power Supply Voltage (measured with respect to GND)	+3.0	+3.3	+5.5	V

DC Electrical Characteristics

Unless stated otherwise, **VDD = 5 V**

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0		5.5	V
Supply Current	IDD	No load		60		mA
Input High Voltage	V_{IH}	X1 pin only, Clock input	VDD/2+1	VDD/2		V
Input Low Voltage	V_{IL}	X1 pin only, Clock input		VDD/2	VDD/2-1	V
Input High Voltage	V_{IH}	All tri-level inputs	VDD-0.5			V
Input Low Voltage	V_{IL}	All tri-level inputs			0.5	V
Input High Voltage	V_{IH}	Other inputs, except tri-level	2			V
Input Low Voltage	V_{IL}	Other inputs, except tri-level			0.8	V
Output High Voltage	V_{OH}	I_{OH} = -25 mA	2.4			V
Output High Voltage	V_{OH}	I_{OH} = -8 mA	VDD-0.4			V
Output Low Voltage	V_{OL}	I_{OL} = 25 mA			0.4	V
Short Circuit Current	I_{OS}	Each output		±100		mA
Internal Pull-up Resistor		ACS1, BCS1, OE		200		kΩ

AC Electrical Characteristics

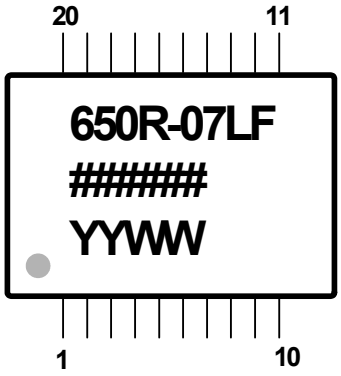
Unless stated otherwise, **VDD = 5 V**

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			10	12.5 or 25	27	MHz
Frequency Error		All clocks			0	ppm
Output Rise Time	t_{OR}	0.8 to 2.0 V			1.5	ns
Output Fall Time	t_{OF}	2.0 to 0.8 V			1.5	ns
Output Clock Duty Cycle		At VDD/2	40	50	60	%
Absolute Jitter, short term		Variation from mean		150		ps

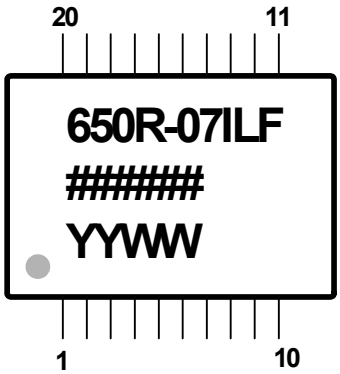
Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		135		°C/W
	θ_{JA}	1 m/s air flow		93		°C/W
	θ_{JA}	3 m/s air flow		78		°C/W
Thermal Resistance Junction to Case	θ_{JC}			60		°C/W

Marking Diagram—ICS650R-07LF



Marking Diagram—ICS650R-07ILF

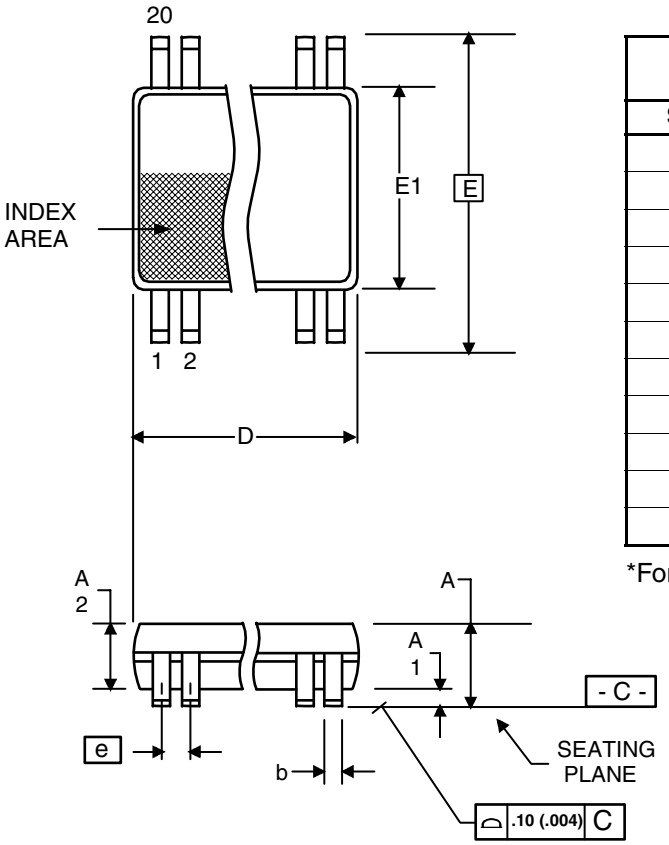


Notes:

1. ###### is the lot code.
2. YYWW is the last two digits of the year, and the week number that the part was assembled.
3. “LF” denotes Pb (lead) free package.
4. “I” denotes industrial grade device.
5. Bottom marking: (origin) = country of origin if not USA.

Package Outline and Package Dimensions (20-pin SSOP, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches*	
Symbol	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	--	1.50	--	0.059
b	0.20	0.30	0.008	0.012
c	0.18	0.25	0.007	0.010
D	8.55	8.75	0.337	0.344
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	.635 Basic		.025 Basic	
L	0.40	1.27	0.016	0.050
α	0°	8°	0°	8°

*For reference only. Controlling dimensions in mm.

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
650R-07LF	see page 7	Tubes	20-pin SSOP	0 to +70° C
650R-07LFT		Tape and Reel	20-pin SSOP	0 to +70° C
650R-07ILF		Tubes	20-pin SSOP	-40 to +85° C
650R-07ILFT		Tape and Reel	20-pin SSOP	-40 to +85° C

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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