

Low Skew Output Buffer

General Description

The **ICS9112A-16** is a high performance, low skew, low jitter clock driver. It uses a phase lock loop (PLL) technology to align, in both phase and frequency, the REF input with the CLKOUT signal. It is designed to distribute high speed clocks in PC systems operating at speeds from 25 to 133 MHz.

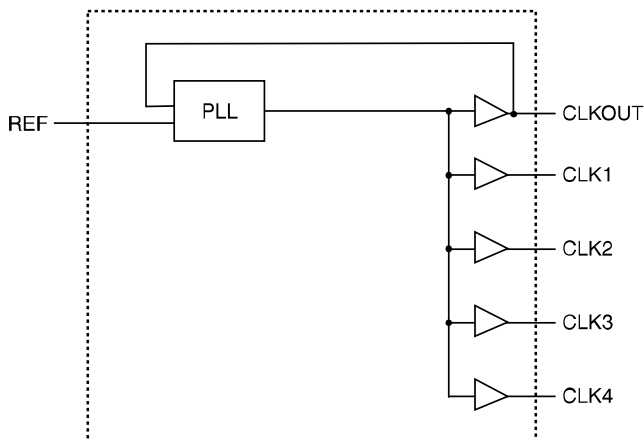
ICS9112A-16 is a zero delay buffer that provides synchronization between the input and output. The synchronization is established via CLKOUT feed back to the input of the PLL. Since the skew between the input and output is less than +/- 350 pS, the part acts as a zero delay buffer.

The **ICS9112A-16** comes in an eight pin 150 mil SOIC or 173 mil TSSOP package. It has five output clocks. In the absence of REF input, will be in the power down mode. In this mode, the PLL is turned off and the output buffers are pulled low. Power down mode provides the lowest power consumption for a standby condition.

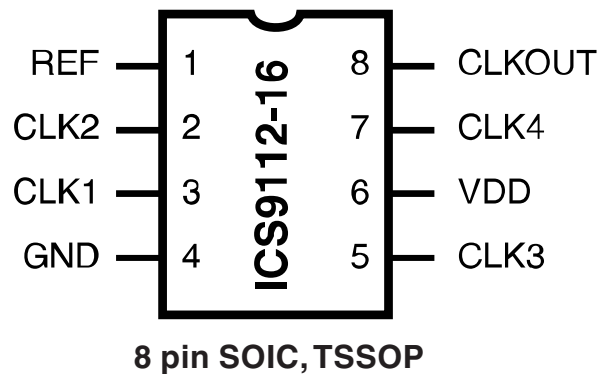
Features

- Zero input - output delay
- Frequency range 25 - 133 MHz (3.3V)
- High loop filter bandwidth ideal for Spread Spectrum applications.
- Less than 200 ps Jitter between outputs
- Skew controlled outputs
- Skew less than 250 ps between outputs
- Available in 8 pin 150 mil SOIC or 173 mil TSSOP package.
- 3.3V \pm 10% operation

Block Diagram



Pin Configuration



Pin Descriptions

| PIN NUMBER | PIN NAME | TYPE | DESCRIPTION |
|------------|---------------------|------|--|
| 1 | REF ² | IN | Input reference frequency. |
| 2 | CLK2 ³ | OUT | Buffered clock output |
| 3 | CLK1 ³ | OUT | Buffered clock output |
| 4 | GND | PWR | Ground |
| 5 | CLK3 ³ | OUT | Buffered clock output |
| 6 | VDD | PWR | Power Supply (3.3V) |
| 7 | CLK4 ³ | OUT | Buffered clock output |
| 8 | CLKOUT ³ | OUT | Buffered clock output. Internal feedback on this pin |

Notes:

1. Guaranteed by design and characterization. Not subject to 100% test.
2. Weak pull-down
3. Weak pull-down on all outputs

Absolute Maximum Ratings

| | |
|-------------------------------|--------------------------------------|
| Supply Voltage | 7.0 V |
| Logic Inputs | GND -0.5 V to V _{DD} +0.5 V |
| Ambient Operating Temperature | 0°C to +70°C |
| Storage Temperature | -65°C to +150°C |

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 3.3V

V_{DD} = 3.0 – 3.6 V, T_A = 0 – 70°C unless otherwise stated

| DC Characteristics | | | | | | |
|----------------------------------|-----------------|---|-----|------|-------|-------|
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
| Input Low Voltage | V _{IL} | | | | 0.8 | V |
| Input High Voltage | V _{IH} | | 2.0 | | | V |
| Input Low Current | I _{IL} | V _{IN} =0V | | 19 | 50.0 | μA |
| Input High Current | I _{IH} | V _{IN} =V _{DD} | | 0.10 | 100.0 | μA |
| Output Low Voltage ¹ | V _{OL} | I _{OL} = 25mA | | 0.25 | 0.4 | V |
| Output High Voltage ¹ | V _{OH} | I _{OH} = 25mA | 2.4 | 2.9 | | V |
| Power Down Supply Current | I _{DD} | REF = 0 MHz | | 0.3 | 50.0 | μA |
| Supply Current | I _{DD} | Unloaded outputs at 66.66 MHz SEL inputs at V _{DD} or GND | | 30.0 | 40.0 | mA |

Notes:

1. Guaranteed by design and characterization. Not subject to 100% test.
2. All Skew specifications are measured with a 50Ω transmission line, load terminated with 50Ω to 1.4V.
3. Duty cycle measured at 1.4V.
4. Skew measured at 1.4V on rising edges. Loading must be equal on outputs.

Switching Characteristics

| PARAMETER | SYMBOL | CONDITION | MIN | TYP | MAX | UNITS |
|--|-----------|--|---------------|-----|--------------|-------------|
| Output period | t1 | With CL=30pF | 40.00 (25) | | 7.5 (133) | ns (MHz) |
| Input period | t1 | With CL=30pF | 40.00 (25) | | 7.5 (133) | ns (MHz) |
| Duty Cycle ¹ | Dt1 | Measured at 1.4V; CL=30pF | 40.0 | 50 | 60 | % |
| Duty Cycle ¹ | Dt2 | Measured at VDD/2 Fout <66.6MHz | 45 | 50 | 55 | % |
| Rise Time ¹ | tr1 | Measured between 0.8V and 2.0V; CL=30pF | | 1.2 | 1.5 | ns |
| Fall Time ¹ | tf1 | Measured between 2.0V and 0.8V; CL=30pF | | 1.2 | 1.5 | ns |
| Rise Time ¹ | tr1 | Measured between 0.8V and 2.0V; CL=5pF | 1 | | | ns |
| Fall Time ¹ | tf1 | Measured between 2.0V and 0.8V; CL=5pF | 1 | | | ns |
| Delay, REF Rising Edge to CLKOUT Rising Edge ^{1, 2} | Dr1 | Measured at 1.4V | | 0 | ±350 | ps |
| Output to Output Skew ¹ | Tskew | All outputs equally loaded, CL=20pF | | | 250 | ps |
| Device to Device Skew ¹ | Tdsk-Tdsk | Measured at VDD/2 on the CLKOUT pins of devices | | 0 | 700 | ps |
| Cycle to Cycle Jitter ¹ | Tcyc-Tcyc | Measured at 66.66 MHz, loaded outputs | | | 200 | ps |
| PLL Lock Time ¹ | tLOCK | Stable power supply, valid clock presented on REF pin | | | 1.0 | ms |
| Jitter; Absolute Jitter ¹ | Tjabs | @ 10,000 cycles CL=30pF | -100 | 70 | 100 | ps |
| Jitter; 1 - Sigma ¹ | Tj1s | @ 10,000 cycles CL=30pF | | 14 | 30 | ps |

Notes:

1. Guaranteed by design and characterization. Not subject to 100% test.
2. REF input has a threshold voltage of 1.4V
3. All parameters expected with loaded outputs

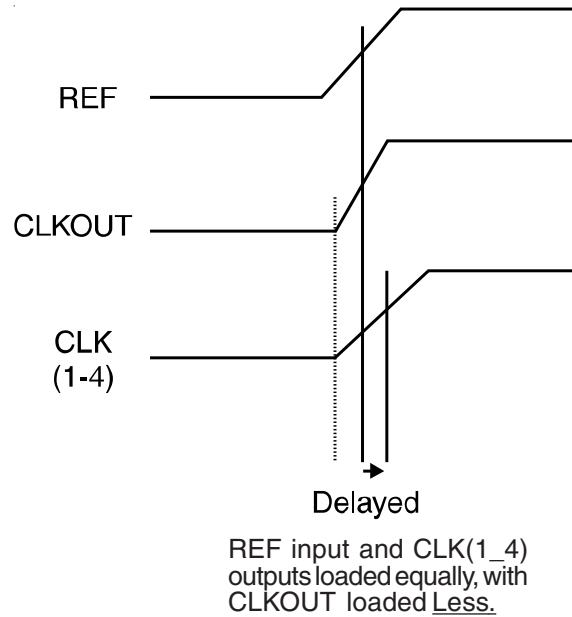
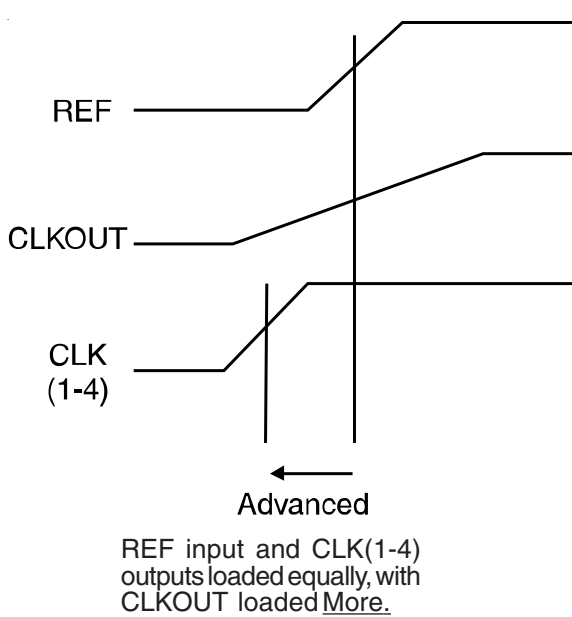
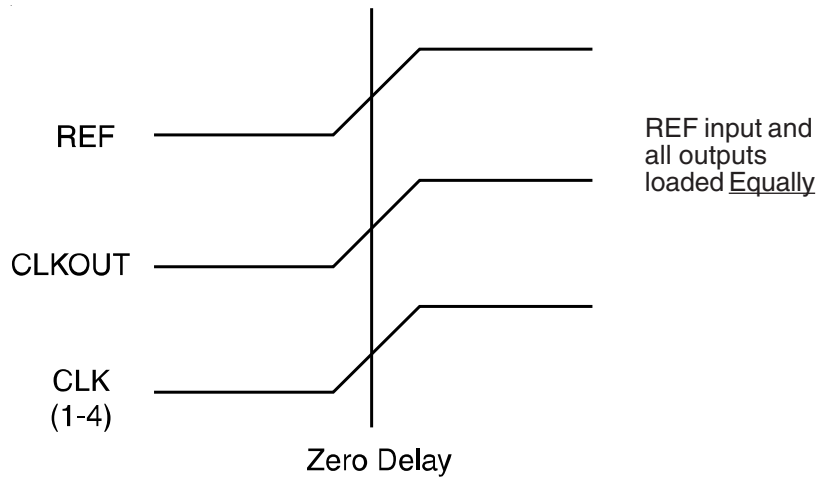
Output to Output Skew

The skew between CLKOUT and the CLK(1-4) outputs is not dynamically adjusted by the PLL. Since CLKOUT is one of the inputs to the PLL, zero phase difference is maintained from REF to CLKOUT. If all outputs are equally loaded, zero phase difference will be maintained from REF to all outputs.

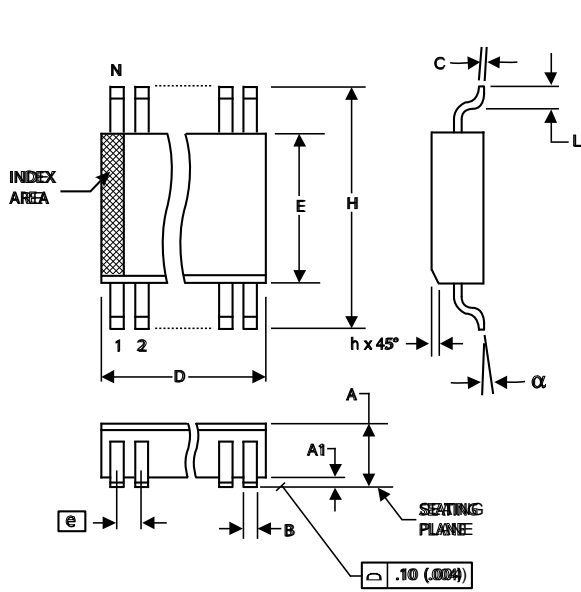
If applications requiring zero output-to-output skew, all the outputs must be equally loaded.

If the CLK(1-4) outputs are less loaded than CLKOUT, CLK(1-4) outputs will lead it; and if the CLK(1-4) is more loaded than CLKOUT, CLK(1-4) will lag the CLKOUT.

Since the CLKOUT and the CLK(1-4) outputs are identical, they all start at the same time, but different loads cause them to have different rise times and different times crossing the measurement thresholds.



Timing diagrams with different loading configurations



150 mil (Narrow Body) SOIC

150 mil (Narrow Body) SOIC

| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|--------|-------------------------------------|------|--------------------------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.75 | .0532 | .0688 |
| A1 | 0.10 | 0.25 | .0040 | .0098 |
| B | 0.33 | 0.51 | .013 | .020 |
| C | 0.19 | 0.25 | .0075 | .0098 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 3.80 | 4.00 | .1497 | .1574 |
| e | 1.27 BASIC | | 0.050 BASIC | |
| H | 5.80 | 6.20 | .2284 | .2440 |
| h | 0.25 | 0.50 | .010 | .020 |
| L | 0.40 | 1.27 | .016 | .050 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| a | 0° | 8° | 0° | 8° |

VARIATIONS

| N | D mm. | | D (inch) | |
|---|-------|------|----------|-------|
| | MIN | MAX | MIN | MAX |
| 8 | 4.80 | 5.00 | .1890 | .1968 |

Reference Doc.: JEDEC Publication 95, MS-012

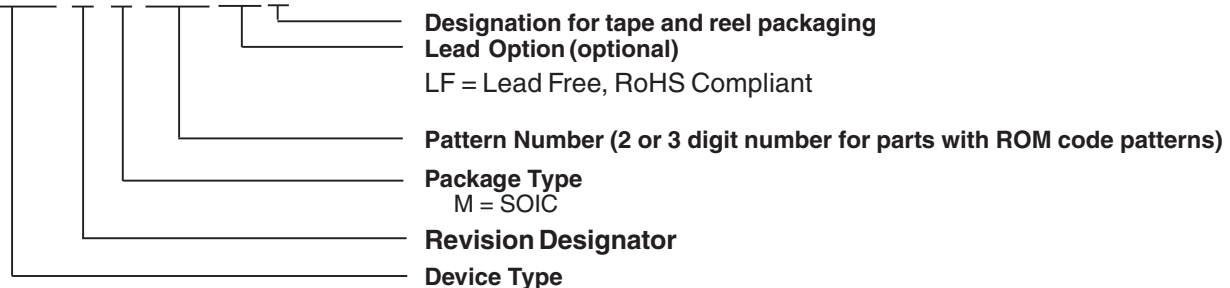
10-0030

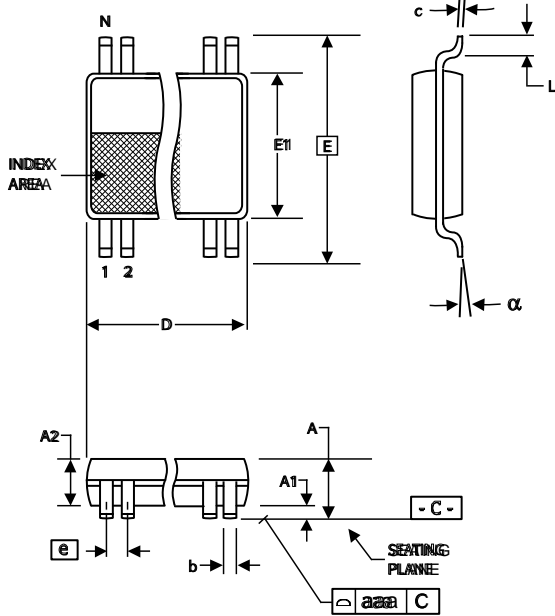
Ordering Information

9112AM-16LFT

Example:

XXXX A M PPP LFT





4.40 mm. Body, 0.65 mm. pitch TSSOP
(173 mil) (0.0256 Inch)

| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|----------|-------------------------------------|------|--------------------------------|------|
| | MIN | MAX | MIN | MAX |
| A | -- | 1.20 | -- | .047 |
| A1 | 0.05 | 0.15 | .002 | .006 |
| A2 | 0.80 | 1.05 | .032 | .041 |
| b | 0.19 | 0.30 | .007 | .012 |
| c | 0.09 | 0.20 | .0035 | .008 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 6.40 BASIC | | 0.252 BASIC | |
| E1 | 4.30 | 4.50 | .169 | .177 |
| e | 0.65 BASIC | | 0.0256 BASIC | |
| L | 0.45 | 0.75 | .018 | .030 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| α | 0° | 8° | 0° | 8° |
| aaa | -- | 0.10 | -- | .004 |

VARIATIONS

| N | D mm. | | D (inch) | |
|---|-------|------|----------|------|
| | MIN | MAX | MIN | MAX |
| 8 | 2.90 | 3.10 | .114 | .122 |

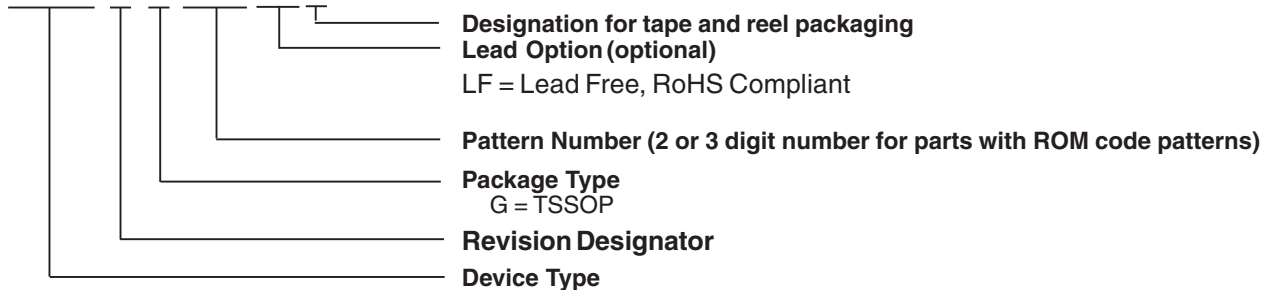
Reference Doc.: JEDEC Publication 95, MO-153
10-0035

Ordering Information

9112AG-16LF-T

Example:

XXXX A G PPP LFT



Revision History

| Rev. | Issue Date | Description | Page # |
|------|------------|---|--------|
| H | 9/1/2004 | Updated Lead Free information | 6-7 |
| I | 11/2/2004 | Added LN option | 6-7 |
| J | 4/26/2007 | Removed LN option superceded by LF. | 6-7 |
| K | 8/3/2007 | Updated Switching Characteristics Rise/Fall time. | 4 |
| L | 12/9/2008 | Removed ICS prefix from ordering information. | 6-7 |