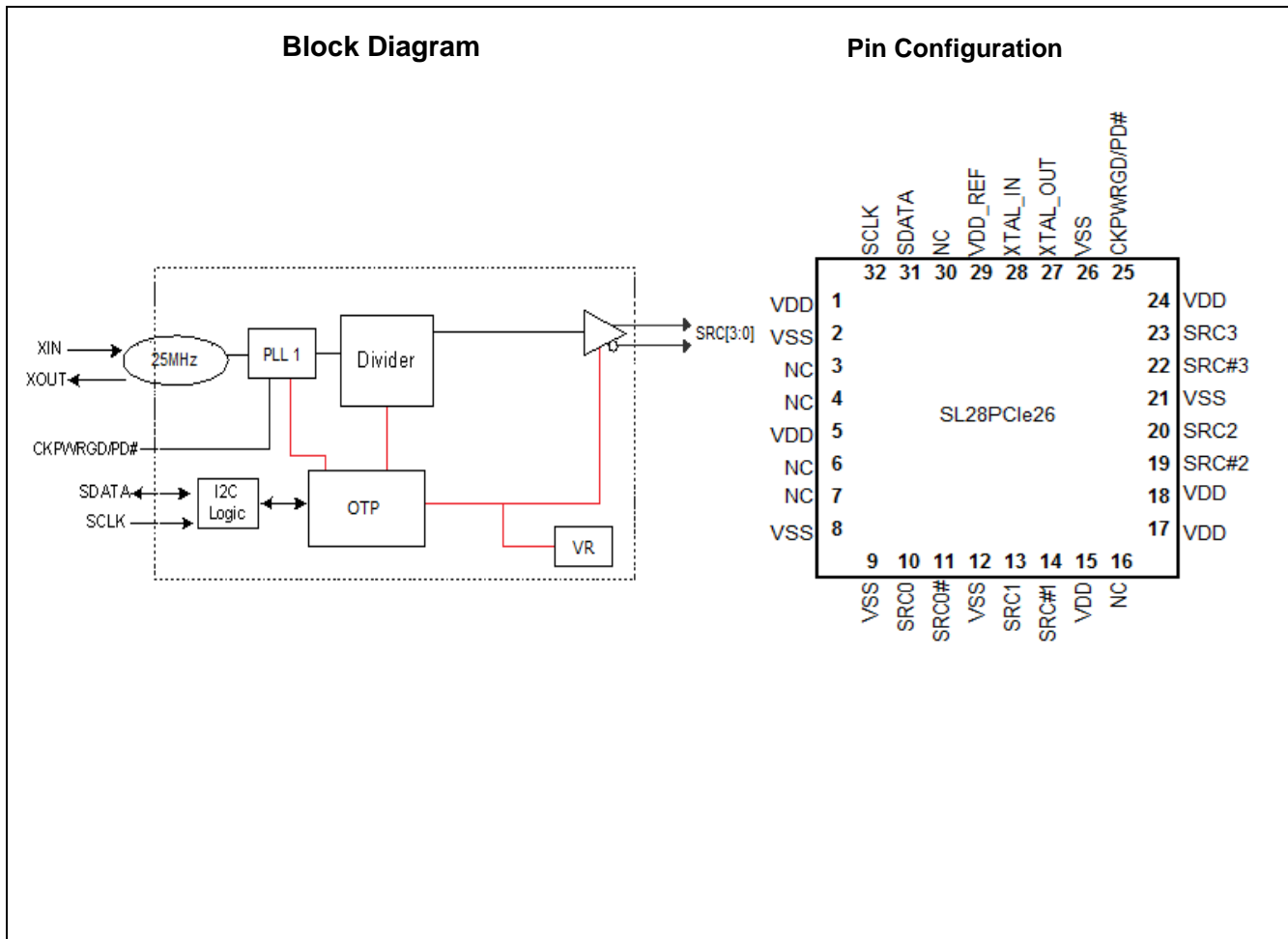


## EProClock<sup>®</sup> PCI Express Gen 2 & Gen 3 Generator

### Features

- Optimized 100 MHz Operating Frequencies to Meet the Next Generation PCI-Express Gen 2 & Gen 3
- Low power push-pull type differential output buffers
- Integrated voltage regulator
- Integrated resistors on differential clocks
- Four 100-MHz differential PCI-Express clocks
- Low jitter (<50ps)
- EProClock<sup>®</sup> Programmable Technology
- I<sup>2</sup>C support with readback capabilities
- Triangular Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction
- 25MHz Crystal Input or Clock input
- Industrial Temperature -40°C to 85°C
- 3.3V Power supply
- 32-pin QFN package



**32-QFN Pin Definitions**

Pin No.	Name	Type	Description
1	VDD	PWR	3.3V Power Supply
2	VSS	GND	Ground
3	NC	NC	No Connect.
4	NC	NC	No Connect.
5	VDD	PWR	3.3V Power Supply
6	NC	NC	No Connect.
7	NC	NC	No Connect.
8	VSS	GND	Ground
9	VSS	GND	Ground
10	SRC0	O, DIF	100MHz True differential serial reference clock
11	SRC0#	O, DIF	100MHz Complement differential serial reference clock
12	VSS	GND	Ground
13	SRC1	O, DIF	100MHz True differential serial reference clock
14	SRC1#	O, DIF	100MHz Complement differential serial reference clock
15	VDD	PWR	3.3V Power Supply
16	NC	NC	No Connect.
17	VDD	PWR	3.3V Power Supply
18	VDD	PWR	3.3V Power Supply
19	SRC2#	O, DIF	100MHz Complement differential serial reference clock
20	SRC2	O, DIF	100MHz True differential serial reference clock
21	VSS	GND	Ground
22	SRC3#	O, DIF	100MHz Complement differential serial reference clock
23	SRC3	O, DIF	100MHz True differential serial reference clock
24	VDD	PWR	3.3V Power Supply
25	CKPWRGD/PD#	I	3.3V LVTTT input pin. When PD# is asserted low, the device will power down.
26	VSS	GND	Ground
27	XOUT	O, SE	25MHz Crystal output, <i>Float XOUT if using CLKIN (Clock Input)</i>
28	XIN/CLKIN	I	25MHz Crystal input or 3.3V, 25MHz Clock Input
29	VDD	PWR	3.3V Power Supply
30	NC	NC	No Connect.
31	SDATA	I/O	SMBus compatible SDATA
32	SCLK	I	SMBus compatible SCLOCK

**EProClock® Programmable Technology**

EProClock® is the world's first non-volatile programmable clock. The EProClock® technology allows board designer to promptly achieve optimum compliance and clock signal integrity; historically, attainable typically through device and/or board redesigns.

EProClock® technology can be configured through SMBus or hard coded.

**Features:**

- > 4000 bits of configurations
- Can be configured through SMBus or hard coded
- Custom frequency sets
- Differential skew control on true or compliment or both

- Differential duty cycle control on true or compliment or both
- Differential amplitude control
- Differential slew rate control
- Program different spread profiles and modulation rates

**Serial Data Interface**

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers are individually enabled or disabled. The registers associated with the Serial Data Interface initialize to

their default setting at power-up. The use of this interface is optional. Clock device register changes are normally made at system initialization, if any are required. The interface cannot be used during system operation for power management functions.

**Data Protocol**

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For

block write/read operation, access the bytes in sequential order from lowest to highest (most significant bit first) with the ability to stop after any complete byte is transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code described in *Table 1*.

The block write and block read protocol is outlined in *Table 2* while *Table 3* outlines byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

**Table 1. Command Code Definition**

Bit	Description
7	0 = Block read or block write operation, 1 = Byte read or byte write operation
(6:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000'

**Table 2. Block Read and Block Write Protocol**

Block Write Protocol		Block Read Protocol	
Bit	Description	Bit	Description
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Byte Count–8 bits	20	Repeat start
28	Acknowledge from slave	27:21	Slave address–7 bits
36:29	Data byte 1–8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
45:38	Data byte 2–8 bits	37:30	Byte Count from slave–8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte /Slave Acknowledges	46:39	Data byte 1 from slave–8 bits
....	Data Byte N–8 bits	47	Acknowledge
....	Acknowledge from slave	55:48	Data byte 2 from slave–8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave / Acknowledge
		....	Data Byte N from slave–8 bits
		....	NOT Acknowledge
		....	Stop

**Table 3. Byte Read and Byte Write Protocol**

Byte Write Protocol		Byte Read Protocol	
Bit	Description	Bit	Description
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Data byte–8 bits	20	Repeated start

**Table 3. Byte Read and Byte Write Protocol**

28	Acknowledge from slave	27:21	Slave address—7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		37:30	Data from slave—8 bits
		38	NOT Acknowledge
		39	Stop

## Control Registers

### Byte 0: Control Register 0

Bit	@Pup	Name	Description
7	1	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	1	RESERVED	RESERVED
4	0	RESERVED	RESERVED
3	0	RESERVED	RESERVED
2	0	RESERVED	RESERVED
1	0	RESERVED	RESERVED
0	1	PD_Restore	Save configuration when PD# is asserted 0 = Config. cleared, 1 = Config. saved

### Byte 1: Control Register 1

Bit	@Pup	Name	Description
7	1	RESERVED	RESERVED
6	0	PLL1_SS_DC	Select for down or center SS 0 = -0.5% Down spread, 1 = +/-0.5% Center spread
5	0	RESERVED	RESERVED
4	0	RESERVED	RESERVED
3	0	RESERVED	RESERVED
2	1	RESERVED	RESERVED
1	0	RESERVED	RESERVED
0	1	RESERVED	RESERVED

### Byte 2: Control Register 2

Bit	@Pup	Name	Description
7	1	RESERVED	RESERVED
6	1	RESERVED	RESERVED
5	1	RESERVED	RESERVED
4	1	RESERVED	RESERVED
3	1	RESERVED	RESERVED
2	1	RESERVED	RESERVED
1	1	RESERVED	RESERVED
0	1	RESERVED	RESERVED

### Byte 3: Control Register 3

Bit	@Pup	Name	Description
-----	------	------	-------------

**Byte 3: Control Register 3**

7	1	RESERVED	RESERVED
6	1	RESERVED	RESERVED
5	1	RESERVED	RESERVED
4	1	RESERVED	RESERVED
3	1	RESERVED	RESERVED
2	1	RESERVED	RESERVED
1	1	RESERVED	RESERVED
0	1	RESERVED	RESERVED

**Byte 4: Control Register 4**

Bit	@Pup	Name	Description
7	1	RESERVED	RESERVED
6	1	SRC0_OE	Output enable for SRC0 0 = Output Disabled, 1 = Output Enabled
5	1	SRC1_OE	Output enable for SRC1 0 = Output Disabled, 1 = Output Enabled
4	0	RESERVED	RESERVED
3	1	SRC3_OE	Output enable for SRC3 0 = Output Disabled, 1 = Output Enabled
2	1	SRC2_OE	Output enable for SRC2 0 = Output Disabled, 1 = Output Enabled
1	0	PLL1_SS_EN	Enable PLL1s spread modulation, 0 = Spread Disabled, 1 = Spread Enabled
0	1	RESERVED	RESERVED

**Byte 5: Control Register 5**

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	0	RESERVED	RESERVED
4	0	RESERVED	RESERVED
3	0	RESERVED	RESERVED
2	0	RESERVED	RESERVED
1	0	RESERVED	RESERVED
0	0	RESERVED	RESERVED

**Byte 6: Control Register 6**

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	0	RESERVED	RESERVED
4	0	RESERVED	RESERVED
3	0	RESERVED	RESERVED
2	0	RESERVED	RESERVED
1	0	RESERVED	RESERVED
0	0	RESERVED	RESERVED

**Byte 7: Vendor ID**

Bit	@Pup	Name	Description
7	0	Rev Code Bit 3	Revision Code Bit 3
6	1	Rev Code Bit 2	Revision Code Bit 2
5	0	Rev Code Bit 1	Revision Code Bit 1
4	0	Rev Code Bit 0	Revision Code Bit 0
3	1	Vendor ID bit 3	Vendor ID Bit 3
2	0	Vendor ID bit 2	Vendor ID Bit 2
1	0	Vendor ID bit 1	Vendor ID Bit 1
0	0	Vendor ID bit 0	Vendor ID Bit 0

**Byte 8: Control Register 8**

Bit	@Pup	Name	Description
7	1	Device_ID3	RESERVED
6	0	Device_ID2	RESERVED
5	0	Device_ID1	RESERVED
4	0	Device_ID0	RESERVED
3	0	RESERVED	RESERVED
2	0	RESERVED	RESERVED
1	0	RESERVED	RESERVED
0	0	RESERVED	RESERVED

**Byte 9: Control Register 9**

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	1	RESERVED	RESERVED
4	0	TEST_MODE_SEL	Test mode select either REF/N or tri-state 0 = All outputs tri-state, 1 = All output REF/N
3	0	TEST_MODE_ENTRY	Allows entry into test mode 0 = Normal Operation, 1 = Enter test mode(s)
2	1	I2C_VOUT<2>	Amplitude configurations differential clocks  I2C_VOUT[2:0] 000 = 0.30V 001 = 0.40V 010 = 0.50V 011 = 0.60V 100 = 0.70V 101 = 0.80V (default) 110 = 0.90V 111 = 1.00V
1	0	I2C_VOUT<1>	
0	1	I2C_VOUT<0>	

**Byte 10: Control Register 10**

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	0	RESERVED	RESERVED
4	0	RESERVED	RESERVED
3	0	RESERVED	RESERVED

**Byte 10: Control Register 10**

Bit	@Pup	Name	Description
2	0	RESERVED	RESERVED
1	1	RESERVED	RESERVED
0	1	RESERVED	RESERVED

**Byte 11: Control Register 11**

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	0	RESERVED	RESERVED
4	0	RESERVED	RESERVED
3	0	RESERVED	RESERVED
2	1	RESERVED	RESERVED
1	1	RESERVED	RESERVED
0	1	RESERVED	RESERVED

**Byte 12: Byte Count**

Bit	@Pup	Name	Description
7	0	BC7	Byte count register for block read operation. The default value for Byte count is 15. In order to read beyond Byte 15, the user should change the byte count limit.to or beyond the byte that is desired to be read.
6	0	BC6	
5	0	BC5	
4	0	BC4	
3	1	BC3	
2	1	BC2	
1	1	BC1	
0	1	BC0	

**Byte 13: Control Register 13**

Bit	@Pup	Name	Description
7	1	RESERVED	RESERVED
6	1	RESERVED	RESERVED
5	1	RESERVED	RESERVED
4	1	RESERVED	RESERVED
3	1	RESERVED	RESERVED
2	1	RESERVED	RESERVED
1	0	RESERVED	RESERVED
0	0	RESERVED	RESERVED

**Byte 14: Control Register 14**

Bit	@Pup	Name	Description
7	1	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	1	RESERVED	RESERVED

Bit	@Pup	Name	Description
4	0	OTP_4	OTP_ID Identification for programmed device
3	0	OTP_3	
2	1	OTP_2	
1	0	OTP_1	
0	1	OTP_0	

**Table 4. Output Driver Status**

	All Differential Clocks	
	Clock	Clock#
PD# = 0 (Power down)	Low	Low

**PD# (Power down) Assertion**

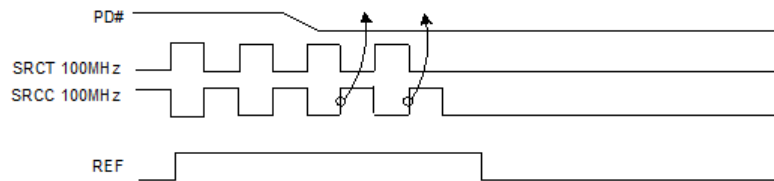
When PD is sampled HIGH by two consecutive rising edges of SRCC, differential clocks must held LOW. When PD mode is desired as the initial power on state, PD must be asserted HIGH in less than 10  $\mu$ s after asserting CKPWRGD.

**PD# (Power down) Clarification**

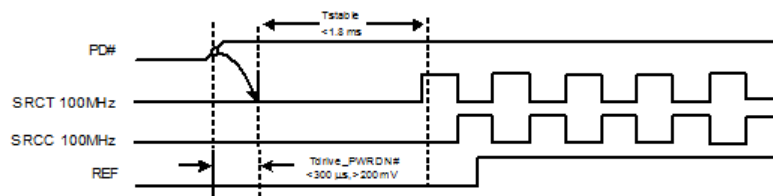
The CKPWRGD/PD# pin is a dual-function pin. During initial power up, the pin functions as CKPWRGD. Once CKPWRGD has been sampled HIGH by the clock chip, the pin assumes PD# functionality. The PD# pin is an asynchronous active LOW input used to shut off all clocks cleanly before shutting off power to the device. This signal is synchronized internally to the device before powering down the clock synthesizer. PD# is also an asynchronous input for powering up the system. When PD# is asserted LOW, clocks are driven to a LOW value and held before turning off the VCOs and the crystal oscillator.

**PD# Deassertion**

The power up latency is less than 1.8 ms. This is the time from the deassertion of the PD# pin or the ramping of the power supply until the time that stable clocks are generated from the clock chip. All differential outputs stopped in a three-state condition, resulting from power down are driven high in less than 300  $\mu$ s of PD# deassertion to a voltage greater than 200 mV. After the clock chip's internal PLL is powered up and locked, all outputs are enabled within a few clock cycles of each clock. *Figure 2* is an example showing the relationship of clocks coming up.



**Figure 1. Power down Assertion Timing Waveform**



**Figure 2. Power down Deassertion Timing Waveform**



**Absolute Maximum Conditions**

Parameter	Description	Condition	Min.	Max.	Unit
V <sub>DD_3.3V</sub>	Main Supply Voltage	Functional	–	4.6	V
V <sub>IN</sub>	Input Voltage	Relative to V <sub>SS</sub>	–0.5	4.6	V <sub>DC</sub>
T <sub>S</sub>	Temperature, Storage	Non-functional	–65	150	°C
T <sub>A</sub>	Temperature, Operating Ambient, Commercial	Functional	0	85	°C
T <sub>A</sub>	Temperature, Operating Ambient, Industrial	Functional	–40	85	°C
T <sub>J</sub>	Temperature, Junction	Functional	–	150	°C
∅ <sub>JC</sub>	Dissipation, Junction to Case	JEDEC (JESD 51)	–	20	°C/W
∅ <sub>JA</sub>	Dissipation, Junction to Ambient	JEDEC (JESD 51)	–	60	°C/W
ESD <sub>HBM</sub>	ESD Protection (Human Body Model)	JEDEC (JESD 22 - A114)	2000	–	V
UL-94	Flammability Rating	UL (Class)	V-0		

**DC Electrical Specifications**

Parameter	Description	Condition	Min.	Max.	Unit
V <sub>DD core</sub>	3.3V Operating Voltage	3.3 ± 5%	3.135	3.465	V
V <sub>IH</sub>	3.3V Input High Voltage (SE)		2.0	V <sub>DD</sub> + 0.3	V
V <sub>IL</sub>	3.3V Input Low Voltage (SE)		V <sub>SS</sub> – 0.3	0.8	V
V <sub>IHI2C</sub>	Input High Voltage	S <sub>DATA</sub> , S <sub>CLK</sub>	2.2	–	V
V <sub>ILI2C</sub>	Input Low Voltage	S <sub>DATA</sub> , S <sub>CLK</sub>	–	1.0	V
I <sub>IH</sub>	Input High Leakage Current	Except internal pull-down resistors, 0 < V <sub>IN</sub> < V <sub>DD</sub>	–	5	μA
I <sub>IL</sub>	Input Low Leakage Current	Except internal pull-up resistors, 0 < V <sub>IN</sub> < V <sub>DD</sub>	–5	–	μA
I <sub>OZ</sub>	High-impedance Output Current		–10	10	μA
C <sub>IN</sub>	Input Pin Capacitance		1.5	5	pF
C <sub>OUT</sub>	Output Pin Capacitance		–	6	pF
L <sub>IN</sub>	Pin Inductance		–	7	nH
I <sub>DD_PD</sub>	Power Down Current		–	1	mA
I <sub>DD_3.3V</sub>	Dynamic Supply Current	All outputs enabled. Differential clocks with 7” traces 2pF load.	–	50	mA

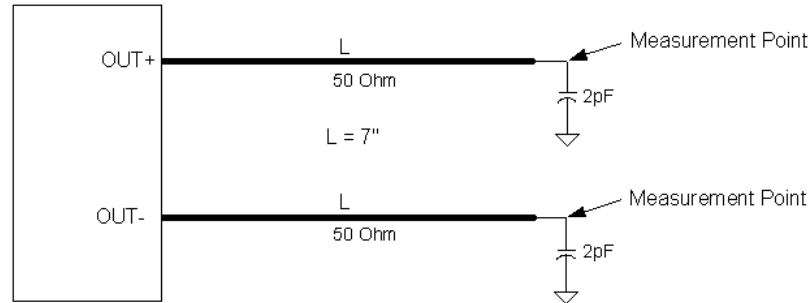
**AC Electrical Specifications**

Parameter	Description	Condition	Min.	Max.	Unit
<b>Crystal</b>					
L <sub>ACC</sub>	Long-term Accuracy	Measured at VDD/2 differential	–	250	ppm
<b>Clock Input</b>					
T <sub>DC</sub>	CLKIN Duty Cycle	Measured at VDD/2	47	53	%
T <sub>R</sub> /T <sub>F</sub>	CLKIN Rise and Fall Times	Measured between 0.2V <sub>DD</sub> and 0.8V <sub>DD</sub>	0.5	4.0	V/ns
T <sub>CCJ</sub>	CLKIN Cycle to Cycle Jitter	Measured at VDD/2	–	250	ps
T <sub>LTJ</sub>	CLKIN Long Term Jitter	Measured at VDD/2	–	350	ps
V <sub>IH</sub>	Input High Voltage	XIN / CLKIN pin	2	VDD+0.3	V
V <sub>IL</sub>	Input Low Voltage	XIN / CLKIN pin	–	0.8	V
I <sub>IH</sub>	Input High Current	XIN / CLKIN pin, VIN = VDD	–	35	uA
I <sub>IL</sub>	Input Low Current	XIN / CLKIN pin, 0 < VIN < 0.8	-35	–	uA
<b>SRC at 0.7V</b>					
T <sub>DC</sub>	Duty Cycle	Measured at 0V differential	45	55	%
T <sub>PERIOD</sub>	Period	Measured at 0V differential at 0.1s	9.99900	10.0010	ns
T <sub>PERIODSS</sub>	Period, SSC	Measured at 0V differential at 0.1s	10.02406	10.02607	ns
T <sub>PERIODAbs</sub>	Absolute Period	Measured at 0V differential at 1 clock	9.87400	10.1260	ns
T <sub>PERIODSSAbs</sub>	Absolute Period, SSC	Measured at 0V differential at 1 clock	9.87406	10.1762	ns
T <sub>CCJ</sub>	Cycle to Cycle Jitter	Measured at 0V differential	–	125	ps
RMS <sub>GEN1</sub>	Output PCIe* Gen1 REFCLK phase jitter	BER = 1E-12 (including PLL BW 8 - 16 MHz, ζ = 0.54, Td=10 ns, Ftrk=1.5 MHz)	0	108	ps
RMS <sub>GEN2</sub>	Output PCIe* Gen2 REFCLK phase jitter	Includes PLL BW 8 - 16 MHz, Jitter Peaking = 3dB, ζ = 0.54, Td=10 ns), Low Band, F < 1.5MHz	0	3.0	ps
RMS <sub>GEN2</sub>	Output PCIe* Gen2 REFCLK phase jitter	Includes PLL BW 8 - 16 MHz, Jitter Peaking = 3dB, ζ = 0.54, Td=10 ns), Low Band, F < 1.5MHz	0	3.1	ps
RMS <sub>GEN3</sub>	Output phase jitter impact – PCIe* Gen3	Includes PLL BW 2 - 4 MHz, CDR = 10MHz)	0	1.0	ps
L <sub>ACC</sub>	Long Term Accuracy	Measured at 0V differential	–	100	ppm
T <sub>R</sub> / T <sub>F</sub>	Rising/Falling Slew Rate	Measured differentially from ±150 mV	2.5	8	V/ns
V <sub>HIGH</sub>	Voltage High			1.15	V
V <sub>LOW</sub>	Voltage Low		-0.3	–	V
V <sub>OX</sub>	Crossing Point Voltage at 0.7V Swing		300	550	mV
<b>ENABLE/DISABLE and SET-UP</b>					
T <sub>STABLE</sub>	Clock Stabilization from Power-up		–	1.8	ms
T <sub>SS</sub>	Stopclock Set-up Time		10.0	–	ns

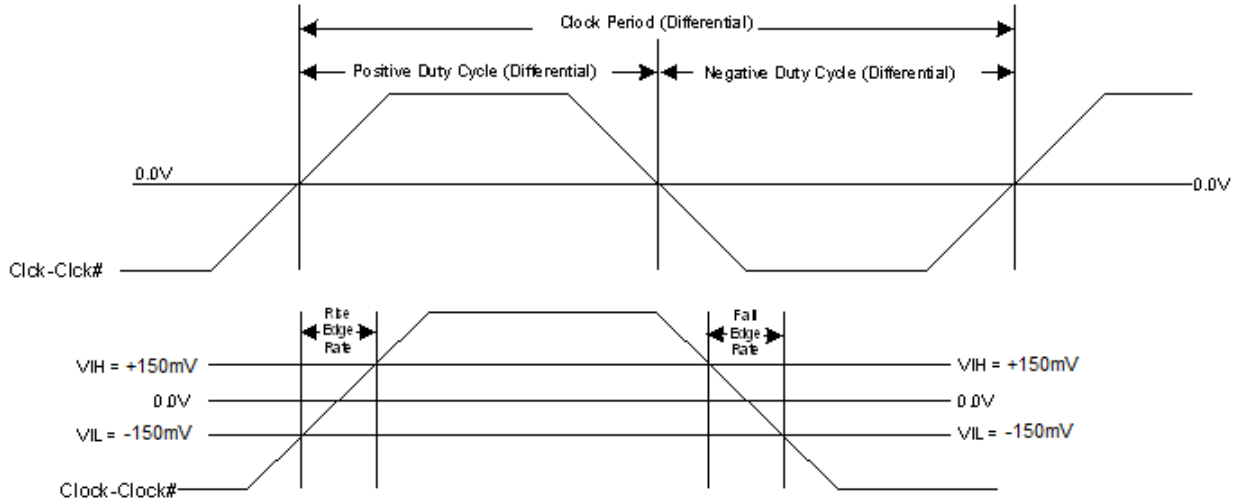
**Test and Measurement Set-up**

**For Differential Clock Signals**

This diagram shows the test load configuration for the differential clock signals



**Figure 3. 0.7V Differential Load Configuration**



**Figure 4. Differential Measurement for Differential Output Signals (for AC Parameters Measurement)**

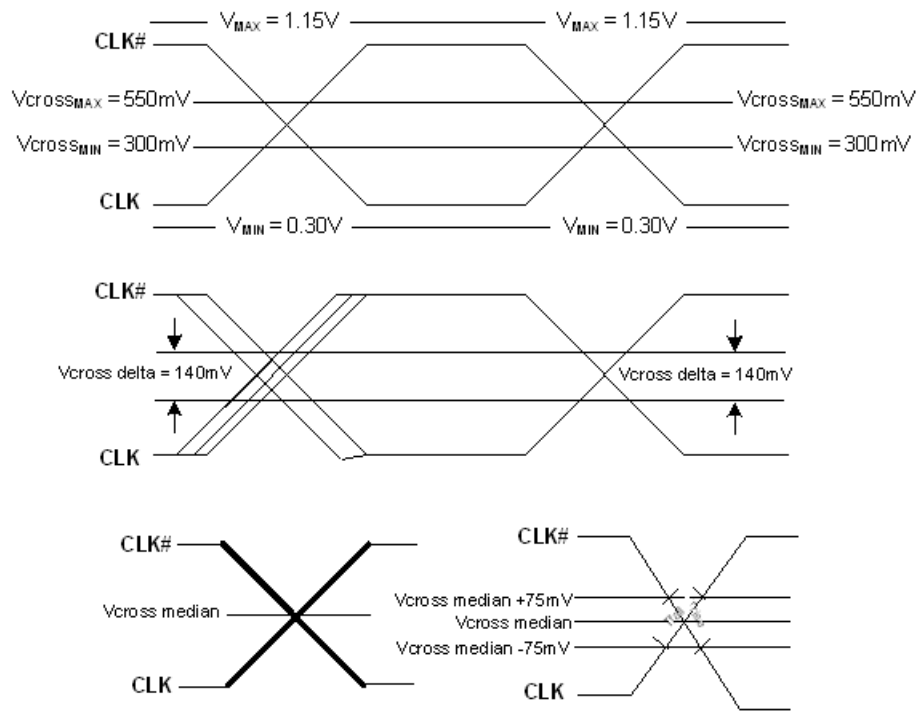


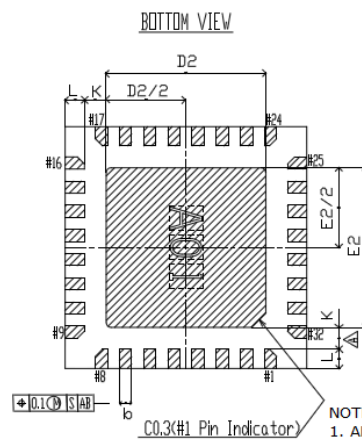
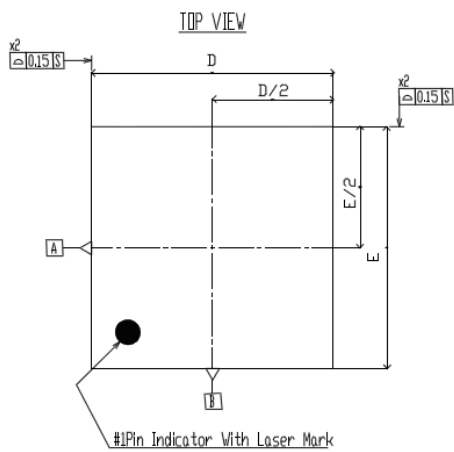
Figure 5. Single-ended Measurement for Differential Output Signals (for AC Parameters Measurement)

**Ordering Information**

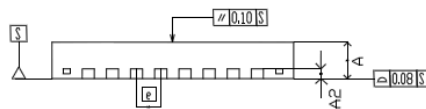
Part Number	Package Type	Product Flow
<b>Lead-free</b>		
SL28PCle26ALC	32-pin QFN	Industrial, 0° to 85°C
SL28PCle26ALCT	32-pin QFN–Tape and Reel	Industrial, 0° to 85°C
SL28PCle26ALI	32-pin QFN	Industrial, -40° to 85°C
SL28PCle26ALIT	32-pin QFN–Tape and Reel	Industrial, -40° to 85°C

**Package Diagrams**

**32-Lead QFN 5x 5mm**



- NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.
  2. DIMENSIONAL TOLERANCE UNLESS OTHERWISE SPECIFIED +/- 0.10.
  3. THE SURFACE OF THE PACKAGE SHALL BE RZ 4-8UM
  4. PROTRUSIONS AT THE PKG. OUTLINE SHALL NOT EXCEED 0.10.



\*TRACE CODE: BOTTOM SIDE HALF ETCHING(DEPTH=0.1REF.)  
 ① A,B,- JK(FRAME ROW)  
 ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨ ⑩ ⑪ ⑫ ⑬ ⑭ ⑮ ⑯ ⑰ ⑱ ⑲ ⑳ ㉑ ㉒ ㉓ ㉔ ㉕ ㉖ ㉗ ㉘ ㉙ ㉚ ㉛ ㉜ ㉝ ㉞ ㉟ ㊱ ㊲ ㊳ ㊴ ㊵ ㊶ ㊷ ㊸ ㊹ ㊺ ㊻ ㊼ ㊽ ㊾ ㊿ 01 02 03 04 05 06 07 08 09 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100 101 102 103 104 105 106 107 108 109 110 111 112 113 114 115 116 117 118 119 120 121 122 123 124 125 126 127 128 129 130 131 132 133 134 135 136 137 138 139 140 141 142 143 144 145 146 147 148 149 150 151 152 153 154 155 156 157 158 159 160 161 162 163 164 165 166 167 168 169 170 171 172 173 174 175 176 177 178 179 180 181 182 183 184 185 186 187 188 189 190 191 192 193 194 195 196 197 198 199 200 201 202 203 204 205 206 207 208 209 210 211 212 213 214 215 216 217 218 219 220 221 222 223 224 225 226 227 228 229 230 231 232 233 234 235 236 237 238 239 240 241 242 243 244 245 246 247 248 249 250 251 252 253 254 255 256 257 258 259 260 261 262 263 264 265 266 267 268 269 270 271 272 273 274 275 276 277 278 279 280 281 282 283 284 285 286 287 288 289 290 291 292 293 294 295 296 297 298 299 300 301 302 303 304 305 306 307 308 309 310 311 312 313 314 315 316 317 318 319 320 321 322 323 324 325 326 327 328 329 330 331 332 333 334 335 336 337 338 339 340 341 342 343 344 345 346 347 348 349 350 351 352 353 354 355 356 357 358 359 360 361 362 363 364 365 366 367 368 369 370 371 372 373 374 375 376 377 378 379 380 381 382 383 384 385 386 387 388 389 390 391 392 393 394 395 396 397 398 399 400 401 402 403 404 405 406 407 408 409 410 411 412 413 414 415 416 417 418 419 420 421 422 423 424 425 426 427 428 429 430 431 432 433 434 435 436 437 438 439 440 441 442 443 444 445 446 447 448 449 450 451 452 453 454 455 456 457 458 459 460 461 462 463 464 465 466 467 468 469 470 471 472 473 474 475 476 477 478 479 480 481 482 483 484 485 486 487 488 489 490 491 492 493 494 495 496 497 498 499 500 501 502 503 504 505 506 507 508 509 510 511 512 513 514 515 516 517 518 519 520 521 522 523 524 525 526 527 528 529 530 531 532 533 534 535 536 537 538 539 540 541 542 543 544 545 546 547 548 549 550 551 552 553 554 555 556 557 558 559 560 561 562 563 564 565 566 567 568 569 570 571 572 573 574 575 576 577 578 579 580 581 582 583 584 585 586 587 588 589 590 591 592 593 594 595 596 597 598 599 600 601 602 603 604 605 606 607 608 609 610 611 612 613 614 615 616 617 618 619 620 621 622 623 624 625 626 627 628 629 630 631 632 633 634 635 636 637 638 639 640 641 642 643 644 645 646 647 648 649 650 651 652 653 654 655 656 657 658 659 660 661 662 663 664 665 666 667 668 669 670 671 672 673 674 675 676 677 678 679 680 681 682 683 684 685 686 687 688 689 690 691 692 693 694 695 696 697 698 699 700 701 702 703 704 705 706 707 708 709 710 711 712 713 714 715 716 717 718 719 720 721 722 723 724 725 726 727 728 729 730 731 732 733 734 735 736 737 738 739 740 741 742 743 744 745 746 747 748 749 750 751 752 753 754 755 756 757 758 759 760 761 762 763 764 765 766 767 768 769 770 771 772 773 774 775 776 777 778 779 780 781 782 783 784 785 786 787 788 789 790 791 792 793 794 795 796 797 798 799 800 801 802 803 804 805 806 807 808 809 810 811 812 813 814 815 816 817 818 819 820 821 822 823 824 825 826 827 828 829 830 831 832 833 834 835 836 837 838 839 840 841 842 843 844 845 846 847 848 849 850 851 852 853 854 855 856 857 858 859 860 861 862 863 864 865 866 867 868 869 870 871 872 873 874 875 876 877 878 879 880 881 882 883 884 885 886 887 888 889 890 891 892 893 894 895 896 897 898 899 900 901 902 903 904 905 906 907 908 909 910 911 912 913 914 915 916 917 918 919 920 921 922 923 924 925 926 927 928 929 930 931 932 933 934 935 936 937 938 939 940 941 942 943 944 945 946 947 948 949 950 951 952 953 954 955 956 957 958 959 960 961 962 963 964 965 966 967 968 969 970 971 972 973 974 975 976 977 978 979 980 981 982 983 984 985 986 987 988 989 990 991 992 993 994 995 996 997 998 999 1000

SYMBOL	COMMON DIMENSIONS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A2	0.20 REF.		
b	0.20	0.25	0.30
D	4.90	5.00	5.10
D2	3.15	3.30	3.45
E	4.90	5.00	5.10
E2	3.15	3.30	3.45
e	0.50 BSC.		
k	0.41	—	—
L	0.30	0.40	0.50

**Document History Page**

<b>Document Title: SL28PCle26 PC EProClock® PCI Express Gen 2 &amp; Gen 3 Generator</b>			
<b>DOC#: SP-AP-0774 (Rev. 0.2)</b>			
<b>REV.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
1.0	9/17/09	JMA	Initial Release
1.1	10/13/09	JMA	Updated miscellaneous text content
AA	05/17/10	JMA	1. Added CLKINFeatures. 2. Updated default spread to be non-spread PCI-Express 3. Updated I2C registers 4. Updated IDD Spec
AA	10/21/10	TRP	Updated miscellaneous text content
AA	11/17/10	TRP	1. Updated IDD condition on trace lenght to 7" 2. Added spread percentage on Byte1 bit6



## ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

[www.silabs.com/CBPro](http://www.silabs.com/CBPro)



Timing Portfolio  
[www.silabs.com/timing](http://www.silabs.com/timing)



SW/HW  
[www.silabs.com/CBPro](http://www.silabs.com/CBPro)



Quality  
[www.silabs.com/quality](http://www.silabs.com/quality)



Support and Community  
[community.silabs.com](http://community.silabs.com)

### Disclaimer

Silicon Laboratories intends to provide customers with the latest, accurate, and in-depth documentation of all peripherals and modules available for system and software implementers using or intending to use the Silicon Laboratories products. Characterization data, available modules and peripherals, memory sizes and memory addresses refer to each specific device, and "Typical" parameters provided can and do vary in different applications. Application examples described herein are for illustrative purposes only. Silicon Laboratories reserves the right to make changes without further notice and limitation to product information, specifications, and descriptions herein, and does not give warranties as to the accuracy or completeness of the included information. Silicon Laboratories shall have no liability for the consequences of use of the information supplied herein. This document does not imply or express copyright licenses granted hereunder to design or fabricate any integrated circuits. The products are not designed or authorized to be used within any Life Support System without the specific written consent of Silicon Laboratories. A "Life Support System" is any product or system intended to support or sustain life and/or health, which, if it fails, can be reasonably expected to result in significant personal injury or death. Silicon Laboratories products are not designed or authorized for military applications. Silicon Laboratories products shall under no circumstances be used in weapons of mass destruction including (but not limited to) nuclear, biological or chemical weapons, or missiles capable of delivering such weapons.

### Trademark Information

Silicon Laboratories Inc.®, Silicon Laboratories®, Silicon Labs®, SiLabs® and the Silicon Labs logo®, Bluegiga®, Bluegiga Logo®, Clockbuilder®, CMEMS®, DSPLL®, EFM®, EFM32®, EFR®, Ember®, Energy Micro, Energy Micro logo and combinations thereof, "the world's most energy friendly microcontrollers", Ember®, EZLink®, EZRadio®, EZRadioPRO®, Gecko®, ISOModem®, Precision32®, ProSLIC®, Simplicity Studio®, SiPHY®, Telegesis, the Telegesis Logo®, USBXpress® and others are trademarks or registered trademarks of Silicon Laboratories Inc. ARM, CORTEX, Cortex-M3 and THUMB are trademarks or registered trademarks of ARM Holdings. Keil is a registered trademark of ARM Limited. All other products or brand names mentioned herein are trademarks of their respective holders.



Silicon Laboratories Inc.  
400 West Cesar Chavez  
Austin, TX 78701  
USA

<http://www.silabs.com>