High Efficiency Power Supply for Small Size Displays

ISL98607R5576

The ISL98607R5576 is a high efficiency power supply for small size displays, such as smart phones, requiring ±supply rails. It integrates a boost regulator, LDO and an inverting charge pump that are used to generate two output rails: +5.6V (default) and -5.6V (default). The output voltages can be adjusted up to ±5.7V with 50mV steps using the I^2C interface.

The device integrates synchronous rectification MOSFETs for the boost regulator and inverting charge pump, which maximizes conversion efficiency.

ISL98607R5576 integrates all compensation and feedback components, which minimizes BOM count and reduces the solution PCB size to $21mm^2$.

The input voltage range, high efficiency operation, and also very low shutdown current make the device ideal for use in single cell Li-ion battery operated applications.

The ISL98607R5576 is offered in a $1.82x2.15mm^2$ WLCSP package, and the device is specified for operation over the -40°C to +85°C ambient temperature range.

Features

- Two outputs:
  - VP = +5.6V (default)
  - VN = -5.6V (default)
- 2.8V to 4.8V input voltage range
- >85% efficiency with 20mA load between VP and VN
- $21mm^2$ Solution PCB area
- Fully integrated FETs for synchronous rectification
- Integrated compensation and feedback circuits
- I^2C adjustable output voltages and settings
- Integrated VP/VN discharge resistors
- 1µA shutdown supply current
- 1.82x2.15mm, 4x5 array WLCSP with 0.4mm pitch
- Pb-Free (RoHS compliant)

Applications

- TFT-LCD smart phone displays
- Small size/handheld displays

Typical Application

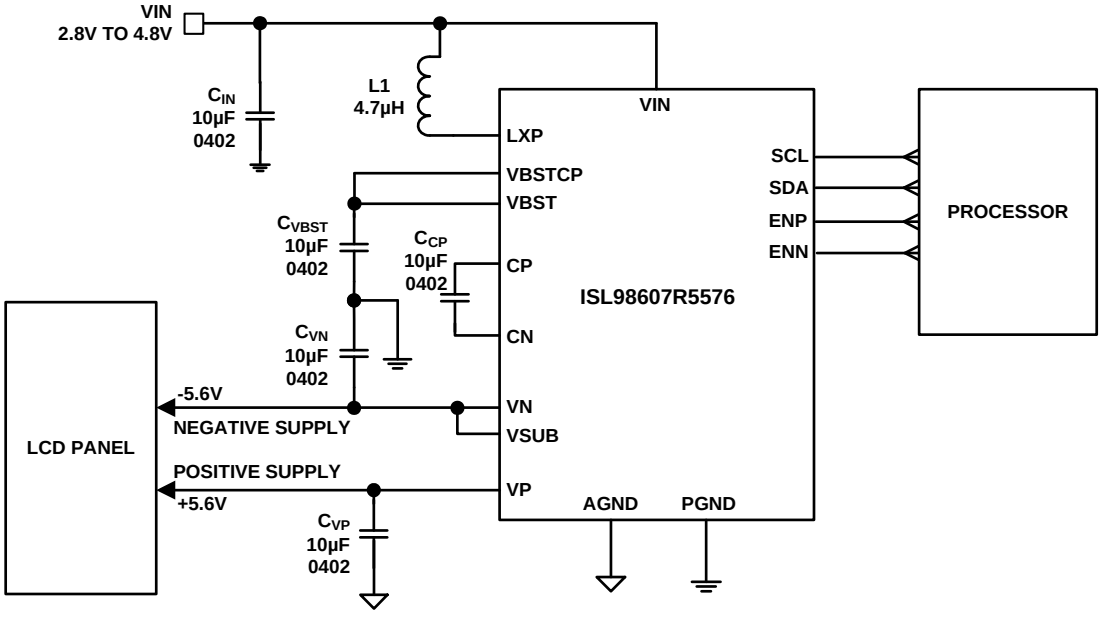

FIGURE 1. TYPICAL APPLICATION CIRCUIT: TFT-LCD SMART PHONE DISPLAY

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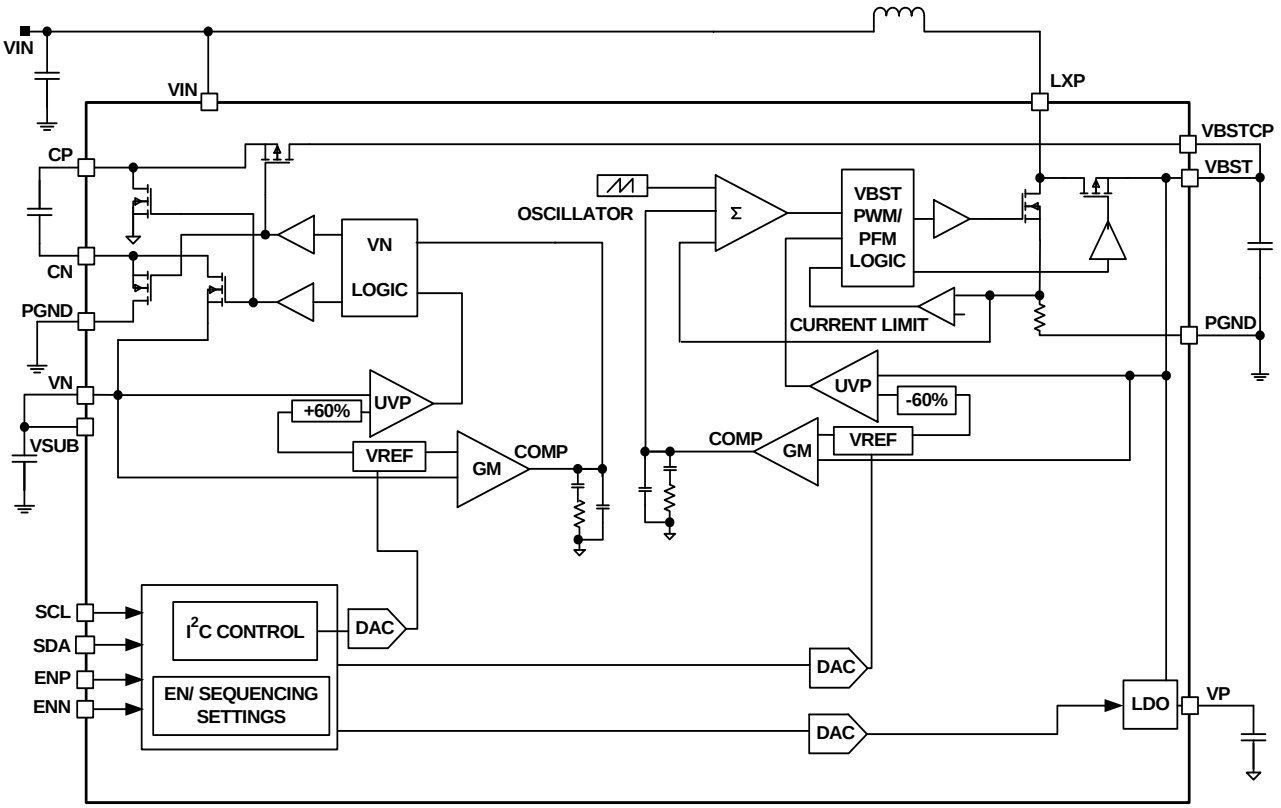
Block Diagram



Ordering Information

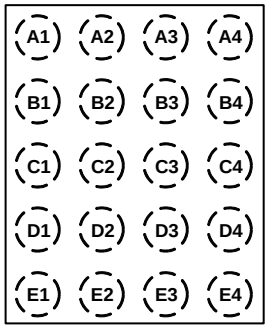
PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE Tape and Reel (Pb-free)	PKG. DWG. #
ISL98607EIAZ-TR5576	5576	-40 to +85	20 Ball (4x5 bump, 0.4mm pitch) WLCSP	W4x5.20E
ISL98607EIAZR5576EVZ	Evaluation Board			

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free WLCSP and BGA packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCu - e1 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free WLCSP and BGA packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For more information on MSL, please see tech brief TB363.

Pin Configuration

ISL98607R5576
(20 BUMP, 4x5 ARRAY, 0.4mm PITCH WLCSP)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
A1, B1	PGND	Power ground for the boost converter.
A2	DNC	Do not connect to external circuitry. This pin should be left floating.
A3, A4	VP	VP Output. Connect a 10µF capacitor to ground. Bumps A3 and A4 must always be shorted together on the PCB.
B2	LXP	Switch node for boost converter. Connect an inductor between the VIN and LXP pins for boost converter operation.
B3	VBST	Boost Converter Output. The boost converter output supplies the power to the negative charge pump and LDO. Connect a 10µF capacitor to ground.
B4	VBSTCP	Charge pump input. This pin must be connected to VBST on the PCB, so that the boost regulator provides the input voltage supply for the charge pump.
C1	AGND	Analog ground.
C2	ENN	VBST and VN enable input. Note, this pin has 200kΩ (typical) pull-down to AGND.
C3	ENP	VBST and VP enable input. Note, this pin has 200kΩ (typical) pull-down to AGND.
C4	CP	Charge pump positive connection. Place a capacitor between CP and CN to create the VN voltage.
D1	VIN	Input Supply. Connect a 10µF to ground.
D2	SDA	Serial Data Connection for I^2C Interface.
D3	SCL	Serial Clock Connection for I^2C Interface.
D4	PGND	Power ground for the negative charge pump.
E1	DNC	Do not connect to external circuitry. This pin should be left floating.
E2	VSUB	Substrate connection. VSUB must be the most negative potential on the IC, connect VSUB to VN.
E3	VN	Negative charge pump output. Connect a 10µF capacitor to ground. Connecting two 10µF capacitors to ground will lower the negative charge pump output voltage ripple.
E4	CN	Charge pump negative connection. Place a capacitor between CP and CN to generate the VN voltage.

Absolute Maximum Ratings

VBST, VBSTCP, CP, VP to AGND . . . . . -0.3V to 7V
VN, VSUB to AGND . . . . . +0.3V to -7V
VIN, SCL, SDA, ENN, ENP to AGND . . . . . -0.3V to 6V
LXP to AGND . . . . . -0.3V to VBST + 0.3V
CN to AGND . . . . . VN - 0.3V to PGND + 0.3V
Maximum Average Current Out of VBST, VP Pin 1A
Maximum Average Current Into LXP Pin 1A
Maximum Average Current Into VN, CN, CP Pin 1A
ESD Rating
Human Body Model (Tested per JESD22-A114) 2000V
Machine Model (Tested per JESD22-A115). 200V
Charged Device Model (Tested per JESD22-C101). 750V
Latch Up (Tested per JESD78; Class II, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
4x5 Bump 0.4mm pitch WLCSP (Notes 4, 5)	66	0.95

Maximum Junction Temperature . . . . . +125°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Ambient Temperature Range . . . . . -40°C to +85°C
V_{IN} . . . . . 2.8V to 4.8V
VP . . . . . +5.6V to +5.7V
VN . . . . . -5.6V to -5.7V
VBST . . . . . +5.75V to +6.0V
Output Current Maximum (between VP and VN) 100mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is taken at the package top center.

Electrical Specifications

V_{IN} = 3.7V, unless otherwise noted. Typical specifications are characterized at T_A = +25°C unless otherwise noted. **Boldface limits apply across the operating temperature range, -40°C to +85°C.**

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
GENERAL						
V_{IN}	V_{IN} Supply Voltage Range		**2.8**		**4.8**	V
I_{IN}	V_{IN} Supply Current	ENP = ENN = 3.7V Enabled, LXP not switching		620	**900**	µA
I_{SHUTDN}	V_{IN} Supply Current When Shutdown	ENP = ENN = 0V		1	**3**	µA
V_{UVLO}	Undervoltage Lockout Threshold	V_{IN} rising	**2.40**	2.52	**2.65**	V
V_{UVLO_HYS}	Undervoltage Lockout Hysteresis	5ms falling		216		mV
BOOST REGULATOR (VBST)						
V_{VBST}	VBST Output Voltage	Register VBST_OUT = 0x00, No Load		5.75		V
I_{LIM_VBST}	Boost nFET Current Limit		**1.2**	1.4	**1.8**	A
r_{ON_VBSTH}	Low-Side Switch ON-Resistance	T_A = +25°C, I_{LOAD_VBST} = 100mA, LXP to PGND		137		mΩ
r_{ON_VBSTL}	High-Side Switch ON-Resistance	T_A = +25°C, I_{LOAD_VBST} = 100mA, LXP to VBST		220		mΩ
I_{L_LXP}	LXP Leakage Current	VLXP = 6V, ENP = ENN = 0V			**10**	µA
D_{MIN}	Boost Minimum Duty Cycle	Boost frequency = 1.45MHz		12.5		%
D_{MAX}	Boost Maximum Duty Cycle	Boost frequency = 1.45MHz		91		%
f_{SWV_VBST}	Boost Switching Frequency	Boost frequency = default	**1.3**	1.45	**1.6**	MHz
t_{SS_VBST}	Boost Soft-start Time	C_{VBST} = 10µF (not derated), V_{IN} > V_{UVLO}		0.7	**2**	ms
NEGATIVE REGULATOR (VN)						
V_{VN}	VN Output Voltage	VN_OUT = 0x00, No Load		-5.6		V
V_{ACC_VN}	VN Output Voltage Accuracy	VN_OUT = 0x00, VBST_OUT = 0x00, -30mA < I_{LOAD_VN} < 0mA	**-1**		**1**	%

Electrical Specifications V_{IN} = 3.7V, unless otherwise noted. Typical specifications are characterized at T_A = +25°C unless otherwise noted. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
f_{SW_VN}	Charge Pump Switching Frequency	CP Frequency = default, 50% duty cycle	**1.3**	1.45	**1.6**	MHz
I_{L_CP}	Charge Pump Leakage Current	CP pin. CP = 6V, ENN = 0V			**10**	µA
R_{DCH_VN}	VN Discharge Resistance	VN = -1V		35		Ω
t_{SS_VN}	VN Soft-start Time			0.7	**2**	ms
POSITIVE REGULATOR (VP)						
V_{VP}	VP Output Voltage	VBST_OUT = 0x00, No Load		5.6		V
V_{ACC_VP}	VP Output Voltage Accuracy	VP_OUT = 0x00, VBST_OUT = 0x00, 0mA < I_{LOAD_VP} < 30mA	**-1**		**1**	%
V_{DRP_VP}	VP Dropout Voltage	I_{LOAD_VP} = 100mA			**100**	mV
I_{LIM_VP}	VP Leakage Current	VP pin. VP = 0V, ENP = 0V			**2**	µA
R_{DCH_VP}	VP Discharge Resistance	VP = 1V		80		Ω
t_{SS_VP}	VP Soft-start			0.7	**2**	ms
PROTECTION						
T_{OFF}	Thermal Shutdown Temperature	Die temperature (rising) when the device will disable/shutdown all outputs until it cools by T_{HYS}°C		130		°C
T_{HYS}	Thermal Shutdown Hysteresis	Die temperature below T_{OFF}°C when the device will re-enable the outputs after shutdown		10		°C
V_{UVP_VP}	VP Undervoltage Protection Threshold			0.6 x VP		V
V_{UVP_VN}	VN Undervoltage Protection Threshold			0.6 x VN		V
LOGIC/DIGITAL						
V_{IL}	Logic Input Low Voltage	ENN, ENP, SCL, SDA			**0.4**	V
V_{IH}	Logic Input High Voltage	ENN, ENP, SCL, SDA	**1.1**			V
f_{CLK}	I^2C SCL Clock Frequency	(Note 7)			**400**	kHz
t_d	Debounce Time	ENN, ENP		10		µs
R_{EN}	Internal Pull-Down Resistance	ENN, ENP		200		kΩ

NOTES:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
7. For more detailed information regarding I^2C timing characteristics refer to Table 1 on page 11.

Typical Performance Curves

T_A = +25°C, V_{IN} = 3.7V, Registers VP_OUT, VN_OUT and VBST_OUT = 0x00, 1239AS-H-4R7M Toko Inductor, C_{VBST} = 10µF/0402, C_{VP} = 10µF/0402 and C_{VN}= 2 x 10µF/0402, unless otherwise noted.

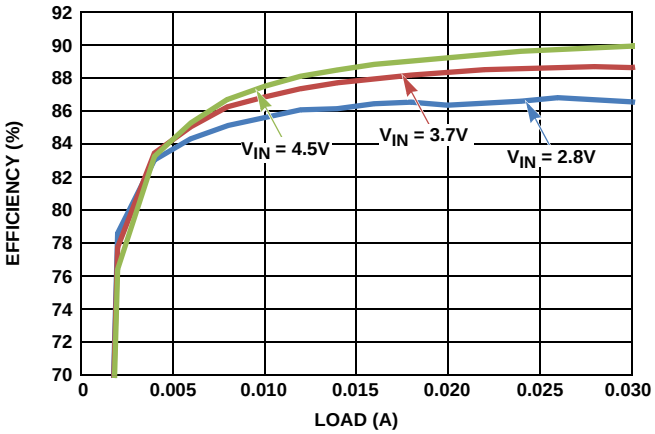


FIGURE 2. EFFICIENCY vs LOAD - REGISTER 0x0D = 0x04, REGISTER 0x0F = 0xDF

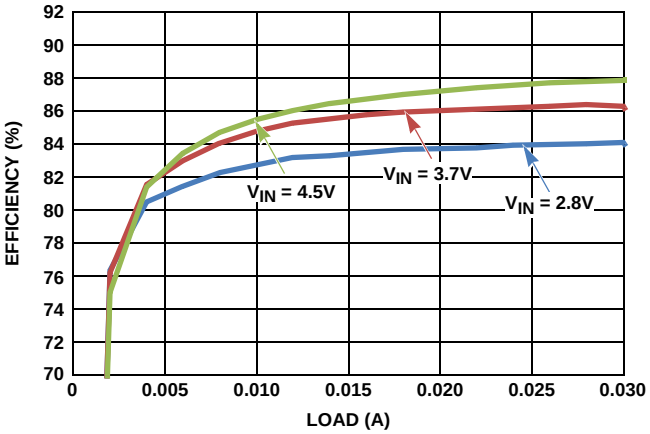


FIGURE 3. EFFICIENCY vs LOAD - REGISTER 0x0D = 0x34, REGISTER 0x0F = 0xDA

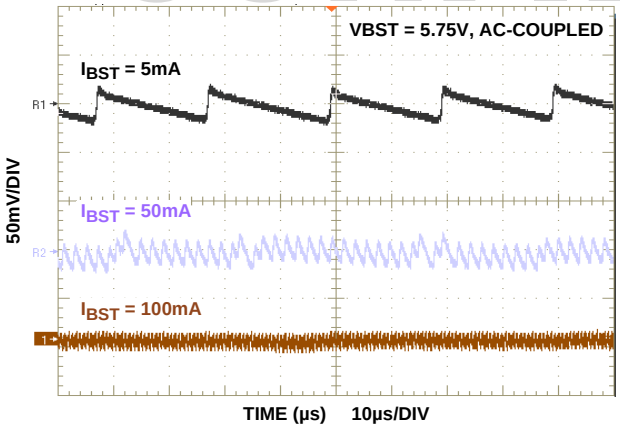


FIGURE 4. VBST OUTPUT VOLTAGE RIPPLE

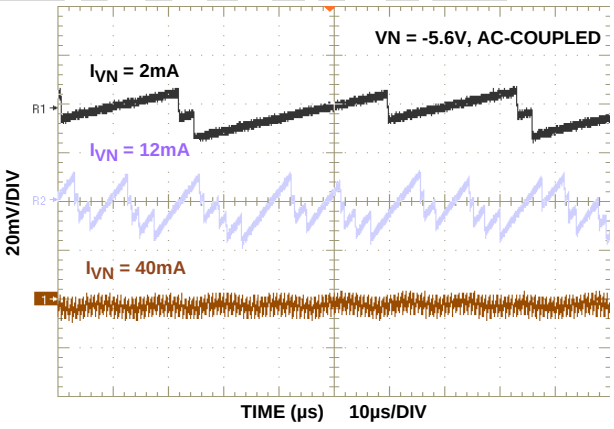


FIGURE 5. VN OUTPUT VOLTAGE RIPPLE REGISTER 0x0D = 0x34, REGISTER 0x0F = 0xDA

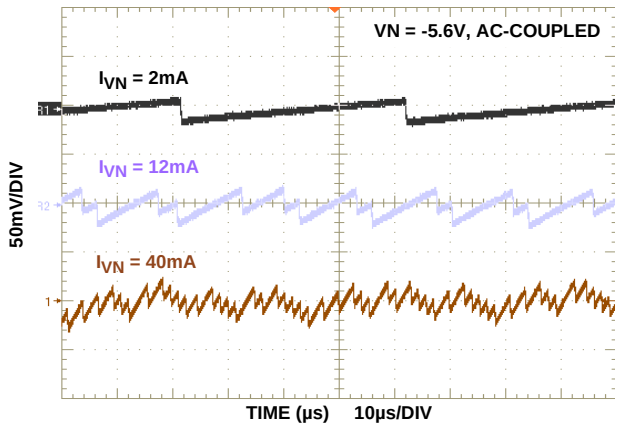


FIGURE 6. VN OUTPUT VOLTAGE RIPPLE REGISTER 0x0D = 0x04, REGISTER 0x0F = 0xDF

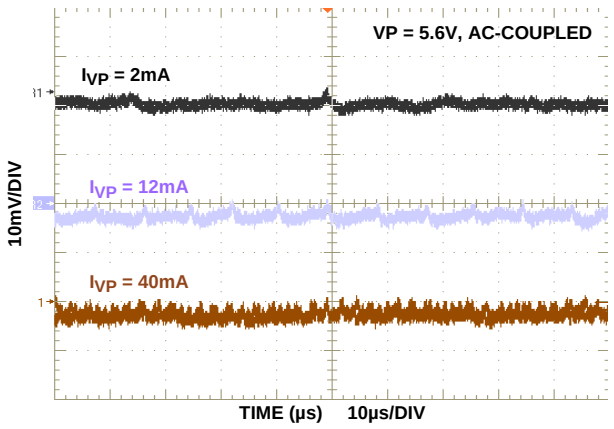


FIGURE 7. VP OUTPUT VOLTAGE RIPPLE REGISTER 0x0D = 0x34, REGISTER 0x0F = 0xDA

Typical Performance Curves

T_A = +25°C, V_{IN} = 3.7V, Registers VP_OUT, VN_OUT and VBST_OUT = 0x00, 1239AS-H-4R7M Toko Inductor, C_{VBST} = 10µF/0402, C_{VP} = 10µF/0402 and C_{VN}= 2 x 10µF/0402, unless otherwise noted. **(Continued)**

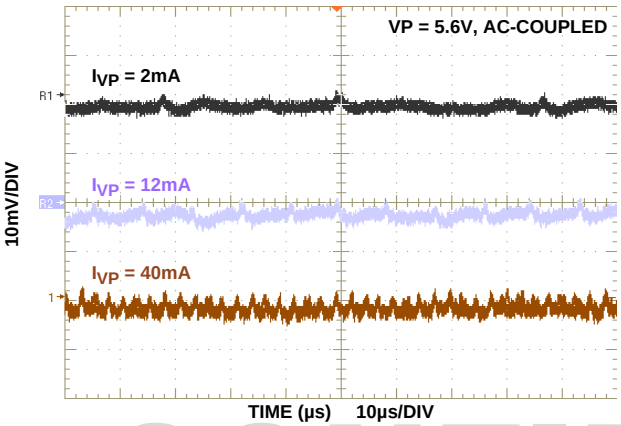


FIGURE 8. VP OUTPUT VOLTAGE RIPPLE REGISTER 0x0D = 0x04, REGISTER 0x0F = 0xDF

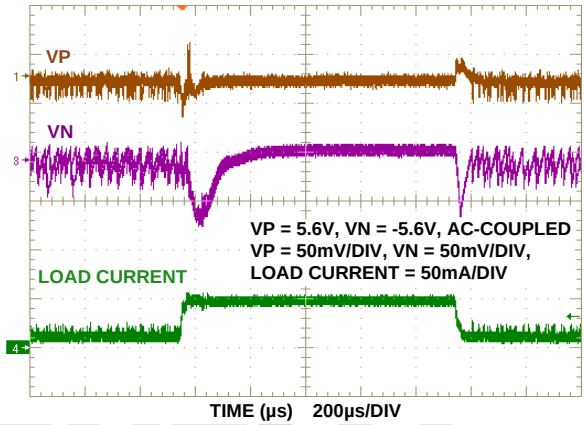


FIGURE 9. VP AND VN LOAD TRANSIENT - V_{IN} 2.8V

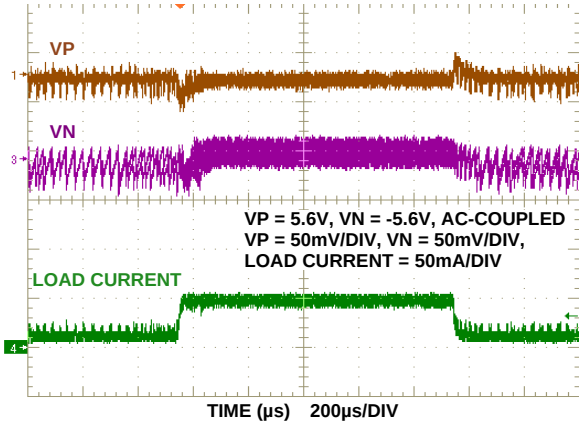


FIGURE 10. VP AND VN LOAD TRANSIENT - V_{IN} 3.7V

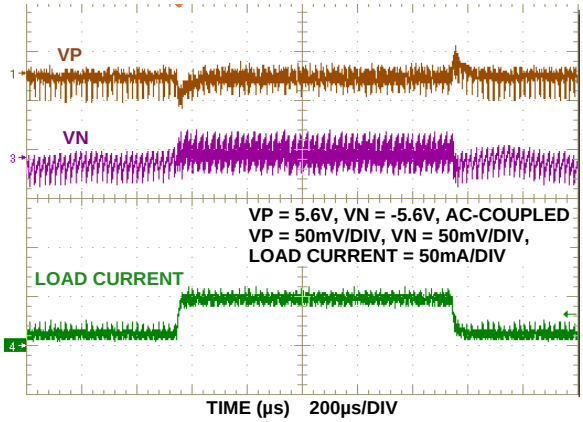


FIGURE 11. VP AND VN LOAD TRANSIENT - V_{IN} 4.5V

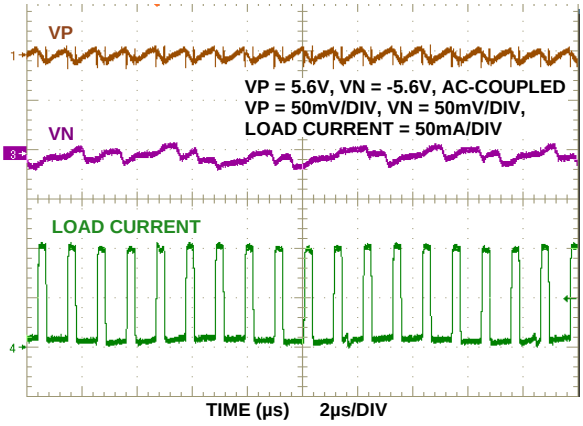


FIGURE 12. VP AND VN LOAD TRANSIENT - ACTUAL DISPLAY CONDITION

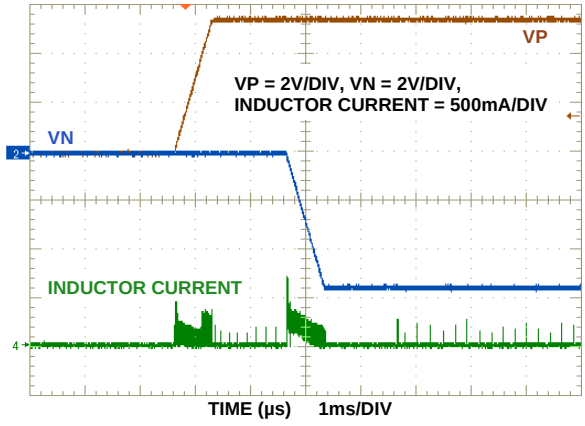


FIGURE 13. IN-RUSH CURRENT - V_{IN} 2.8V

Typical Performance Curves

T_A = +25°C, V_{IN} = 3.7V, Registers VP_OUT, VN_OUT and VBST_OUT = 0x00, 1239AS-H-4R7M Toko Inductor, C_{VBST} = 10µF/0402, C_{VP} = 10µF/0402 and C_{VN}= 2 x 10µF/0402, unless otherwise noted. **(Continued)**

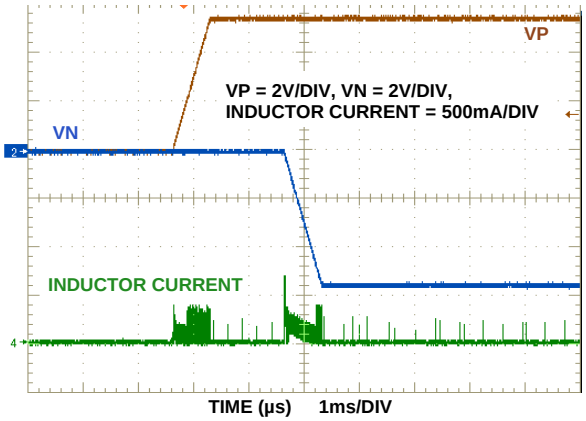


FIGURE 14. IN-RUSH CURRENT - V_{IN} 3.7V

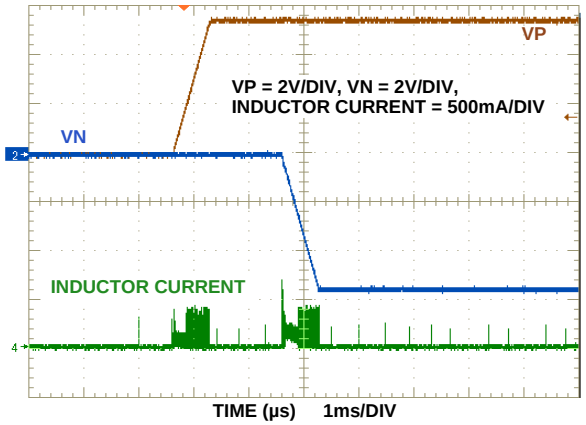


FIGURE 15. IN-RUSH CURRENT - V_{IN} 4.5V

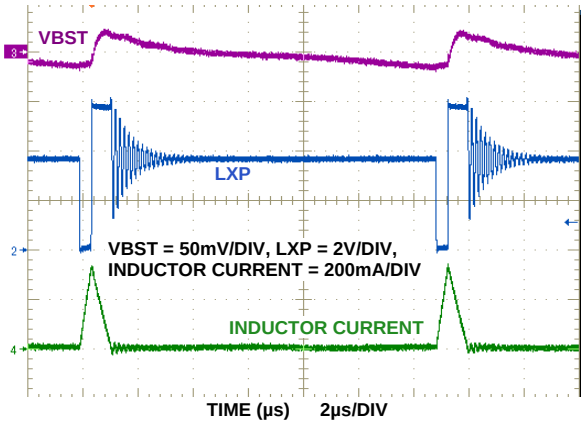


FIGURE 16. VBST OPERATION LIGHT LOAD

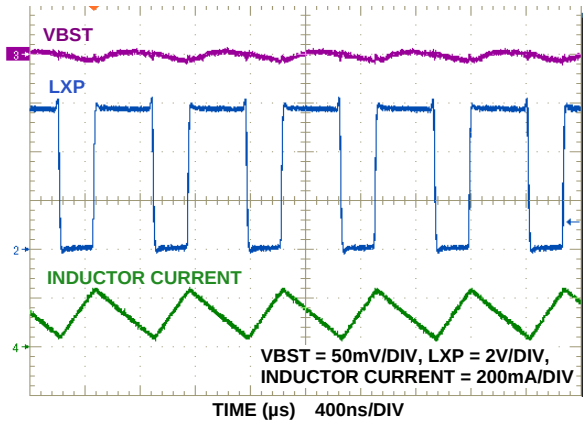


FIGURE 17. VBST OPERATION HEAVY LOAD

Application Information

I²C Digital Interface

The ISL98607R5576 uses a standard I²C interface bus for communication. The two-wire interface links a Master(s) and uniquely addressable Slave devices. The Master generates clock signals and is responsible for initiating data transfers. The serial clock is on the SCL line and the serial data (bidirectional) is on the SDA line. The ISL98607R5576 supports clock rates up to 400kHz (Fast-Mode), and is backwards compatible with standard 100kHz clock rates (Standard-mode).

The SDA and SCL lines must be HIGH when the bus is free - not in use. An external pull-up resistor (typically 2.2kΩ to 4.7kΩ) or current-source is required for SDA and SCL.

The ISL98607R5576 meets standard I²C timing specifications, see Figure 18 and Table 1, which show the standard timing definitions and specifications for I²C communication.

LOW-POWER MODE

The I²C interface of ISL98607R5576 remains active even when both ENN and ENP are LOW for up to 30ms. When ENN and ENP both remain LOW, and no I²C communication occurs for more than 30ms, the ISL98607R5576 enters a low-power mode. This mode disables the I²C interface, but the interface is reactivated as soon as ISL98607R5576 detects a logic LOW on SCL or SDA.

For the ISL98607R5576, when the I²C interface is not used, both the SDA and SCL inputs must be tied HIGH (e.g., to V_{IN}) or pulled-up to a logic HIGH level, to ensure the part enters the Low-Power consumption mode when ENN and ENP are held LOW longer than 30ms. This feature optimizes battery power saving in handheld products, for example, when the display system is put into a standby/sleep mode.

START AND STOP CONDITION

All I²C communication begins with a START condition - indicating the beginning of a transaction, and ends with a STOP condition - signaling the end of the transaction.

A START condition is signified by a HIGH-to-LOW transition on the serial data line (SDA) while the serial clock line (SCL) is HIGH. A STOP condition is signified by a LOW-to-HIGH transition on the SDA line while SCL is HIGH. See timing specifications in Table 1.

The Master always initiates START and STOP conditions. After a START condition, the bus is considered “busy.” After a STOP condition, the bus is considered “free.” The ISL98607R5576 also supports repeated STARTs, where the bus will remain busy for continued transaction(s).

DATA VALIDITY

The data on the SDA line must be stable (clearly defined as HIGH or LOW) during the HIGH period of the clock signal. The state of the SDA line can only change when the SCL line is LOW (except to create a START or STOP condition). See timing specifications in Table 1.

The voltage levels used to indicate a logical ‘0’ (LOW) and logical ‘1’ (HIGH) are determined by the V_{IL} and V_{IH} thresholds, respectively, see the “Electrical Specifications” table on page 6.

BYTE FORMAT

Every byte transferred on SDA must be 8 bits in length. After every byte of data sent by the transmitter there must be an Acknowledge bit (from the receiver) to signify that the previous 8 bits were transferred successfully. Data is always transferred on SDA with the most significant bit (MSB) first. See “Acknowledge (ACK)” on page 11.

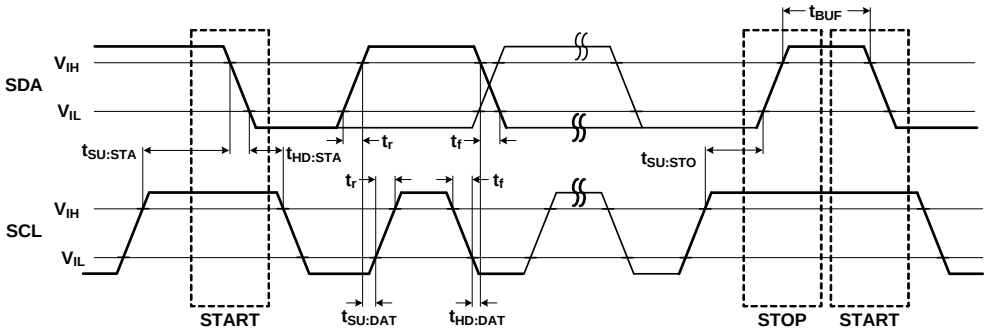


FIGURE 18. I²C TIMING DEFINITIONS

TABLE 1. I^2C TIMING CHARACTERISTICS

PARAMETER	SYMBOL	FAST-MODE		STANDARD-MODE		UNIT
		MIN	MAX	MIN	MAX	
SCL Clock Frequency	f_{SCL}	0	400	0	100	kHz
Set-up Time for a START Condition	$t_{SU:STA}$	0.6	-	4.7	-	µs
Hold Time for a START Condition	$t_{HD:STA}$	0.6	-	4.0	-	µs
Set-up Time for a STOP Condition	$t_{SU:STO}$	0.6	-	4.0	-	µs
Bus Free Time between a STOP and START Condition	t_{BUF}	1.3	-	4.7	-	µs
Data Set-up Time	$t_{SU:DAT}$	100	-	250	-	ns
Data Hold Time	$t_{HD:DAT}$	0	-	0	-	µs
Rise Time of SDA and SCL (Note 8)	t_r	$20 + 0.1C_b$	300	-	1000	ns
Fall Time of SDA and SCL (Note 8)	t_f	$20 + 0.1C_b$	300	-	300	ns
Capacitive Load on Each Bus Line (SDA/SCL)	C_b	-	400	-	400	pF

NOTE:

8. C_b = total capacitance of one bus line in pF.

ACKNOWLEDGE (ACK)

Each 8-bit data transfer is followed by an Acknowledge (ACK) bit from the receiver. The Acknowledge bit signifies that the previous 8 bits of data was transferred successfully (Master-slave or Slave-master).

When the Master sends data to the Slave (e.g., during a WRITE transaction), after the 8^{th} bit of a data byte is transmitted, the Master tri-states the SDA line during the 9^{th} clock. The Slave device acknowledges that it received all 8 bits by pulling down the SDA line, generating an ACK bit.

When the Master receives data from the Slave (e.g., during a data READ transaction), after the 8^{th} bit is transmitted, the Slave tri-states the SDA line during the 9^{th} clock. The Master acknowledges that it received all 8 bits by pulling down the SDA line, generating an ACK bit.

NOT ACKNOWLEDGE (NACK)

A Not Acknowledge (NACK) is generated when the receiver does not pull-down the SDA line during the acknowledge clock (i.e., SDA line remains HIGH during the 9^{th} clock). This indicates to the Master that it can generate a STOP condition to end the transaction and free the bus.

A NACK can be generated for various reasons, for example:

- After an I^2C device address is transmitted, there is NO receiver with that address on the bus to respond.
- The receiver is busy performing an internal operation (e.g., reset, recall, etc), and cannot respond.
- The Master (acting as a receiver) needs to indicate the end of a transfer with the Slave (acting as a transmitter).

DEVICE ADDRESS AND R/$\overline{W}$ BIT

Data transfers follow the format shown in Figures 20 and 21. After a valid START condition, the first byte sent in a transaction contains the 7-bit Device (Slave) Address plus a direction (R/$\overline{W}$) bit. The Device Address identifies which device (of up to 127 devices on the I^2C bus) the Master wishes to communicate with.

After a START condition, the ISL98607R5576 monitors the first 8 bits (Device Address Byte) and checks for its 7-bit Device Address in the MSBs. If it recognizes the correct Device Address it will ACK, and becomes ready for further communication. If it does not see its Device Address, it will sit idle until another START condition is issued on the bus.

To access the ISL98607R5576, the 7-bit Device Address is 0x29 (0101001x), located in MSB bits <b_7:b_1>. The eighth bit of the Device Address byte (LSB bit <b_0>) indicates the direction of transfer, READ or WRITE (R/$\overline{W}$). A “0” indicates a WRITE operation - the Master will transmit data to the ISL98607R5576 (receiver). A “1” indicates a Read operation - the Master will receive data from the ISL98607R5576 (transmitter) (see Figure 19).

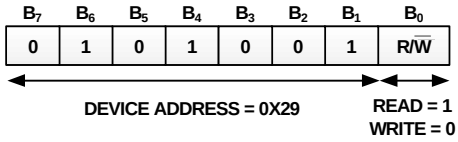


FIGURE 19. DEVICE ADDRESS BYTE FORMAT

Write Operation

A WRITE sequence requires an I²C START condition, followed by a valid Device Address Byte with the R/$\overline{W}$ bit set to '0', a valid Register Address Byte, a Data Byte, and a STOP condition. After each valid byte is sent, the ISL98607R5576 (slave) responds with an ACK. When the Write transaction is completed, the Master should generate a STOP condition. For sent data to be latched by the ISL98607R5576, the STOP condition should occur after a full byte (8-bits) is sent and ACK. If a STOP is generated in the middle of a byte transaction, the data will be ignored. See Figure 20 for the ISL98607R5576 I²C Write protocol.

Read Operation

A READ sequence requires the Master to first write to the ISL98607R5576 to indicate the Register Address/pointer to read from. Send a START condition, followed by a valid Device Address Byte with the R/$\overline{W}$ set to '0', and then a valid Register Address Byte. Next, the Master generates either a Repeat START condition, or a STOP condition followed by a new START condition, and a valid Device Address Byte with the R/$\overline{W}$ bit set to '1'. Then the ISL98607R5576 is ready to send data to the Master from the requested Register Address.

The ISL98607R5576 sends out the Data Byte by asserting control of the SDA pin while the Master generates clock pulses on the SCL pin. When transmission of the desired data is complete, the Master generates a NACK condition followed by a STOP condition, and this completes the I²C Read sequence. See Figure 21 for the ISL98607R5576 I²C Read protocol.

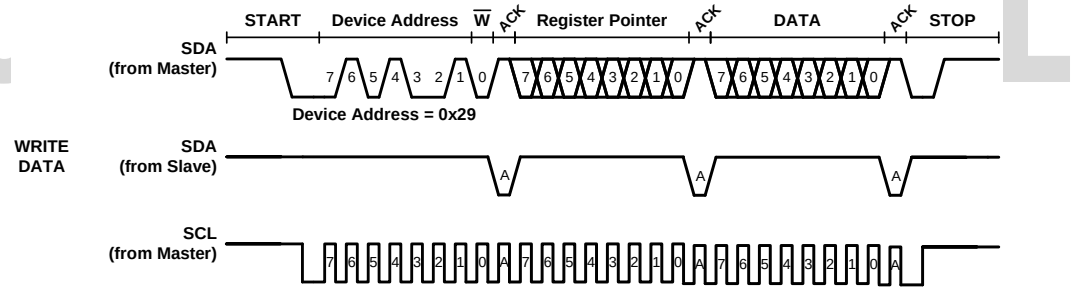


FIGURE 20. I²C WRITE TIMING DIAGRAM

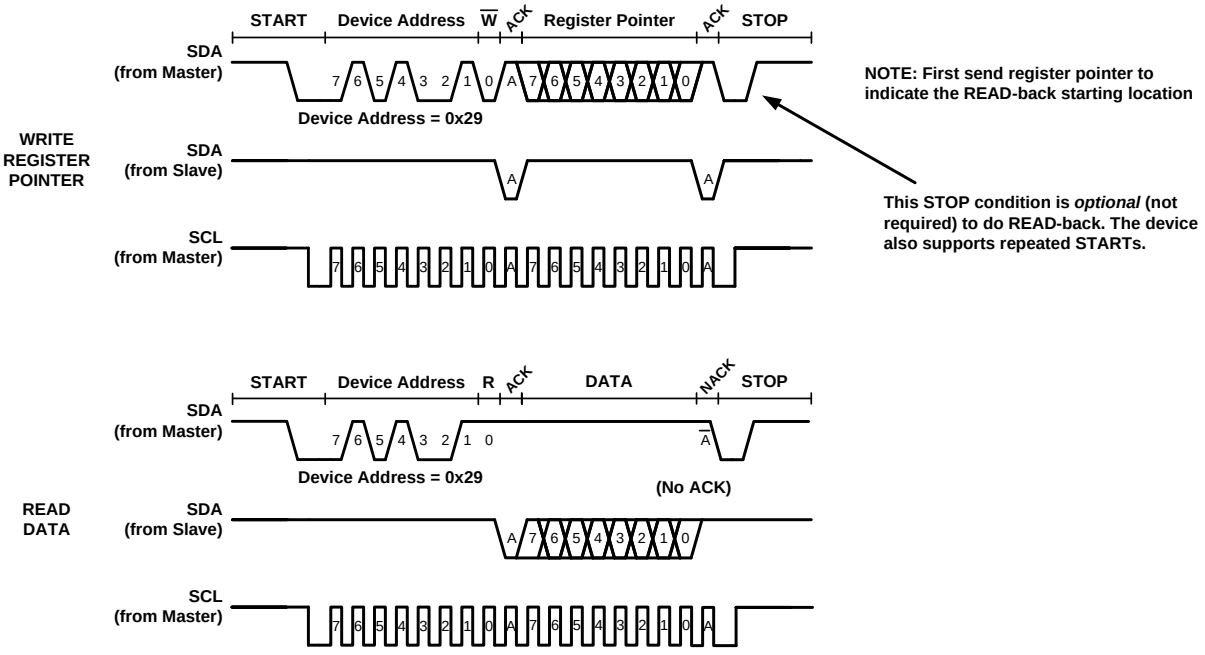


FIGURE 21. I²C READ TIMING DIAGRAM

Register Descriptions and Addresses

Table 2 on page 14 contains the detailed register map, with descriptions and addresses for ISL98607R5576 registers. Each volatile register is one byte (8-bit) in size. When writing data to adjust register settings using I^2C, the data is latched-in after the 8th bit (LSB) is received.

The ISL98607R5576 has default register settings that are always applied at IC power-ON or after a reset. In Table 2, the default register settings are indicated with **BOLD** face text.

Reserved registers should only be written with the bit value indicated in the Register Map. Also, Register Addresses (pointers) not indicated in the Register Map are reserved and should not be written to.

Note, to clear/reset all the volatile registers to the default values, power cycle V_{IN}.

Register Functions

The ISL98607R5576 has various registers that can be used to adjust and control IC operating voltages, modes, thresholds, and sequences.

ENABLE

The “ENABLE” register (Register Address 0x05) can be used to control the enable/disable state of the boost (VBST), positive LDO (VP) and negative charge pump (VN) regulators. This can be used to sequence the regulators.

VBST_OUT, VN_OUT, VP_OUT

The output voltages of VBST, VP and VN regulators can be changed using the registers “VBST_OUT,” “VP_OUT,” and “VN_OUT,” respectively. VBST_OUT is at Register Address 0x06, VN_OUT is at Register Address 0x08, and VP_OUT is at Register Address 0x09.

The output voltages of all three regulators can be changed from their default values using I^2C. The VP regulator can be programmed from +5.6V to +5.7V, the VN regulator can be programmed from -5.6V to -5.7V, and the VBST regulator can be programmed from +5.75V to +6V - each adjustable with 50mV step size. Do not use register settings that result in an expected output voltage above these maximum levels. To determine the expected output voltage for a specific register value, see “Output Voltage Calculation” on page 13.

Note, output voltage registers should not be changed during their respective soft-start sequence.

Output Voltage Calculation

The expected output voltage for each regulator can be determined using Equations 1 through 3. For the calculations: VBST = 5.75V (typ) default, VP = +5.6V (typ) default, VN = -5.6V (typ) default. Note, *VBST_OUT*, *VP_OUT*, and *VN_OUT* are the respective 5-bit register settings in decimal.

- Boost Output Voltage, VBST:

$$VBST(V) = VBST + VBST\_OUT \times 50mV \quad \text{(EQ. 1)}$$

- LDO Output Voltage, VP:

$$VP(V) = VP + VP\_OUT \times 50mV \quad \text{(EQ. 2)}$$

- Negative Charge Pump Output Voltage, VN:

$$VN(V) = VN - VN\_OUT \times 50mV \quad \text{(EQ. 3)}$$

Example Calculations:

If VBST_OUT = 2 (dec):

$$VBST(V) = 5.75V + 2 \times 50mV = 5.85V$$

If VP_OUT = 2 (dec):

$$VP(V) = 5.6V + 2 \times 50mV = 5.7V$$

If VN_OUT = 2 (dec):

$$VN(V) = -5.6V - 2 \times 50mV = -5.7V$$

VBST_CNTRL, VN_CNTRL

In addition to output voltage adjustments, key operation parameters can be changed using I^2C to optimize the ISL98607R5576 performance.

The “VBST_CNTRL” register (Register Address 0x0D) can be used to control and optimize boost PFM mode, boost FET slew rate, and switching frequency of the boost and charge pump.

The “VN_CNTRL” register (Register Address 0x0F) can be used to enable/disable PFM mode, and optimize the charge pump PFM operation with adjustments to the PFM peak current, and pulse length.

FAULT

The “FAULT” register (Register Address 0x04) can be used to read back the current fault status of the IC. The fault conditions that can be read back by I^2C are: VBST undervoltage fault, VP undervoltage fault, VN undervoltage fault, and over-temperature protection (OTP) fault.

FAULT register bits $<b_3:b_0>$ can be reset by cycling the logic voltage on both the ENP and ENN pins simultaneously - set ENN = ENP = LOW, then ENN = ENP = HIGH. Or, to reset the bits power cycle V_{IN}.

If FAULT register bit $<b_0>$ (OTP status bit) is latched HIGH for an OTP fault, it can also be reset after it is read twice by I^2C. A single I^2C read will return the bit value (status), and a second read will reset *only* the OTP bit.

Register Map

TABLE 2. REGISTER MAP

REGISTER ADDRESS (HEX)	REGISTER NAME	R/W	FUNCTION	BIT <b_7>	BIT <b_6>	BIT <b_5>	BIT <b_4>	BIT <b_3>	BIT <b_2>	BIT <b_1>	BIT <b_0>	DEFAULT VALUE (HEX)	IC RESET
0x04	FAULT	R	Fault Status read-back	Reserved (Always set to '0')	Not Used			VP UVP: 0 = Output Voltage OK 1 = UVP Detect	VN UVP: 0 = Output Voltage OK 1 = UVP Detect	VBST UVP: 0 = Output Voltage OK 1 = UVP Detect	OTP: 0 = Temp OK 1 = OTP detected	0x00	Cycle ENN and ENP, or cycle V_{IN}
0x05	ENABLE	R/W	IC Enable/ Sequencing	Reserved (Always set to '0')	VP Pull-down resistor **0 = Enabled** 1 = Disabled	Not Used			VP: 0 = Disable **1 = Enable**	VN: 0 = Disable **1 = Enable**	VBST: 0 = Disable **1 = Enable**	0x07	Cycle V_{IN}
0x06	VBST_OUT	R/W	VBST Voltage Adjustment	Not Used			VBST_OUT <4:0>					0x00	Cycle V_{IN}
0x08	VN_OUT	R/W	VN Voltage Adjustment	Not Used			VN_OUT <4:0>					0x00	Cycle V_{IN}
0x09	VP_OUT	R/W	VP Voltage Adjustment	Not Used			VP_OUT <4:0>					0x00	Cycle V_{IN}
0x0D	VBST_ CNTRL	R/W	VBST - boost regulator control	Reserved (Always set to '00')		Boost LX slew rate **11 = Slowest** 10 = Slow 01 = Fast 00 = Fastest		PFM mode (synchronous PFM) **0 = Enable** 1 = Disable	Boost and Charge Pump Switching Frequency 000 = 0.89MHz 001 = 1.07MHz 010 = 1.23MHz 011 = 1.33MHz **100 = 1.45MHz** 101 = 1.60MHz 110 = 1.78MHz 111 = 2.00MHZ			0x34	Cycle V_{IN}
0x0F	VN_ CNTRL	R/W	VN - negative charge pump control	Reserved (Always set to '11')		PFM Mode **0 = Enabled** 1 = Disabled	PWM min pulse length **1 = 94ns** 0 = 125ns	PFM peak current selection 00 = 4µA 01 = 6µA **10 = 5µA** 11 = 7µA		PFM Pulse length 00 = 188ns 01 = 219ns **10 = 250ns** 11 = 50% selected frequency		0xDA	Cycle V_{IN}

NOTES:

9. Any Register Addresses/Pointers not indicated in the table above are Reserved Registers, and should not be used.
10. Bits labeled "Not Used" can be written and read from the volatile registers, but have no influence on the operation of the IC.

Output Voltage Setting

The VBST, VP and VN output voltages are adjusted (from the default value) by the VBST_OUT, VP_OUT and VN_OUT volatile registers. Equations 1 through 3 on page 13 provide the relation between the value of the I^2C registers and the respective output voltages.

VP and VN Headroom Voltage and Output Current

The VP and VN headroom voltage is defined as the difference between the VBST output voltage and:

- The maximum VP output voltage: VP headroom
- The absolute value of the VN output voltage: VN headroom

The headroom voltage must be set high enough so that both the VP LDO and VN negative charge pump (CP) can maintain regulation. Primarily, the minimum headroom voltage is a function of the maximum application load current that the IC will need to support for at least a few hundred microseconds. Fast output current peaks of only a few microseconds should not be considered - those instantaneous current peaks will be supported by the output capacitors and not by the regulator.

Note, the headroom voltage should not be set overly high, since increasing headroom generally yields lower efficiency performance due to increased conduction losses.

For most applications, the ISL98607R5576 default 150mV headroom voltage setting provides optimal performance for DC output current up to 100mA (max). For DC output current between 100mA and 150mA (max) the headroom voltage should be adjusted to 250mV. For example: if a maximum VP to VN load of 150mA is required, while VP = 5.6V and VN = -5.6V, then the minimum boost voltage should be set to VBST = 5.85V.

Regulator Output Enable/Disable

The boost converter, VBST, will be enabled whenever either ENP *or* ENN is HIGH, and the VBST enable bit <b_0> in the ENABLE register is set to '1'. To disable the boost (and effectively VP and VN), ENN and ENP must be LOW, or its enable bit set to '0'.

The negative charge pump, VN, is enabled whenever ENN is HIGH, and the VN enable bit <b_1> in the ENABLE register is set to '1'. To disable, ENN must be LOW, or its enable bit set to '0'.

The LDO, VP, is enabled whenever ENP is HIGH, and the VP enable bit <b_2> in the ENABLE register is set to '1'. To disable, ENP must be LOW, or its enable bit set to '0'.

All the ENABLE register bits <b_2:b_0> are set to '1' by default.

Various options to control the regulator output ON/OFF sequencing are possible with ISL98607R5576, refer to the "Enable Timing Control Options" on page 17 for more information.

Note, ENP and ENN are logic level inputs with HIGH/LOW thresholds defined by the V_{IH}/V_{IL} specifications, respectively. These inputs also have 200kΩ (typ) internal pull-down resistance to ground. If the pins are left hi-impedance, they will default to a LOW logic state. Refer to the "Logic" section of the "Electrical Specifications" table on page 6 for more information.

Negative Charge Pump Operation (VN)

The ISL98607R5576 uses a negative charge pump with internal switches to create the VN voltage rail. The charge pump input voltage VBSTCP comes from the boost regulator output, VBST. The VBST voltage must be greater than the absolute value of the VN regulation voltage (i.e., the headroom voltage has to be >0V).

Regulation is achieved through a classic voltage mode architecture where an internally compensated g_m amplifier compares the VN output voltage to the internal reference and sets a duty cycle. The duty cycle controls the amount of time the output capacitor is charged during each switching cycle. The maximum duty cycle is 50%. The charge pump output capacitor (placed on the VN pin) is charged and discharged through internal 450mA current sources to minimize system noise.

PFM

The ISL98607R5576 features light load pulse frequency modulation (PFM) mode for both the boost regulator and charge pump, to maximize efficiency at light loads.

The device always uses PWM mode at heavy loading, but when the PFM mode is enabled using the respective PFM mode enable/disable register bit, the device will automatically switch to PFM mode at light loads to optimize efficiency.

There is hysteresis built-in with the PFM transition, when the transition is from light to heavy or heavy to light loading. This is to prevent inadvertently going back and forth between PWM and PFM modes.

Fault Protection and Monitoring

The ISL98607R5576 features extensive protections to automatically handle failure conditions, and protect the IC and application from damage.

OVERCURRENT PROTECTION (OCP)

The overcurrent protection limits the VBST nMOSFET current on a cycle-by-cycle basis. When the nMOSFET current reaches the current limit threshold, the nMOSFET is turned off for the remainder of that cycle. Overcurrent protection does not disable any of the regulators. Once the fault is removed, the IC will continue with normal operation.

UNDERVOLTAGE LOCKOUT (UVLO)

If the input voltage (V_{IN}) falls below the V_{UVLO_HYS} level of ~2.3V (typ), the VBST, VP, and VN regulators will be disabled. All the rails will restart with normal soft-start operation when the V_{IN} input voltage is applied again (rising $V_{IN} > V_{UVLO}$). Refer to the "Electrical Specifications" table on page 5 for the UVLO specifications.

Note, the I^2C registers (logic) are not cleared/reset to default by the falling V_{IN} UVLO. The logic states are retained if V_{IN} remains above 2V (typ). Once V_{IN} falls below 2V, all logic is reset. V_{IN} should fall below 2V (ideally to GND) before power is reapplied to ensure a full power cycle/reset of the device.

OVER-TEMPERATURE PROTECTION (OTP)

The ISL98607R5576 has a hysteretic over-temperature protection threshold set at +130°C (typ). If this threshold is reached, the VBST, VP, and VN regulators are disabled immediately. As soon as temperature falls by 10°C (typ) then all the regulators automatically restart.

All register bits, except for bit <b_0> of the FAULT register (Register Address 0x04), remain unaffected during an OTP fault event. When an OTP event occurs, FAULT register bit <b_0> is latched to '1'. This bit is reset/cleared by cycling both ENN and ENP (set LOW, then HIGH) at the same time, or by cycling V_{IN} power. Bit <b_0> can also be reset after it is read twice by I^2C. A single I^2C read will return the bit value (status), and a second read will reset *only* the OTP bit.

Output undervoltage protection is disabled during an OTP event. Since the output voltages decrease during an OTP event because the regulators are disabled, this will not trigger a UVP fault.

UNDERVOLTAGE PROTECTION (UVP)

The ISL98607R5576 includes output undervoltage protection. Undervoltage protection disables the regulator whenever the output voltage of VBST or VP falls below 60% of its set/regulated voltage, or the output voltage of VN goes above 60% of its set/regulated voltage, for 100µs or more. If the output voltage exceeds the 60% condition for less than 100µs, no fault will occur.

Depending on which regulator(s) fault, bit(s) <b_3>, <b_2>, or <b_1> in the FAULT register will be latched to '1' for VP, VN, and VBST faults, respectively. The bit(s) are reset/cleared by cycling both ENN and ENP (set LOW, then HIGH) at the same time, or by cycling V_{IN} power.

Power-ON/OFF Sequence

The boost regulator is activated when the V_{IN} input voltage is higher than the UVLO threshold, and either ENP or ENN are HIGH. The VP output is activated if ENP is HIGH and VBST has completed its soft-start. The VN charge pump is activated 2ms after VBST has completed soft-start, and the ENN has been pulled high - whichever comes later (see Figure 22).

Figure 23 shows power-ON timing for the case when ENN is pulled HIGH after ENP, and after the VBST soft-start is complete. Figure 24 shows power-ON timing for the case when ENN is pulled HIGH after ENP, but before VBST has completed its soft-start.

ENP or ENN going LOW shuts down VP or VN, respectively. If both ENP and ENN are pulled LOW, then VP, VN and VBST are all turned off even if V_{IN} is still above UVLO, see Figure 25. If V_{IN} falls below UVLO while ENP and ENN are HIGH, then VP, VN and VBST will be turned off at the same time (see Figure 26).

The integrated discharge resistors on the VP and VN outputs are 80Ω (typ) and a 35Ω (typ), respectively. If the same output capacitor (value, size, rating) is used for VN and VP, the VN rail will discharge faster than VP if they are both turned off at the same time. This is ideal for applications that require the VN rail to go down before VP at power-OFF.

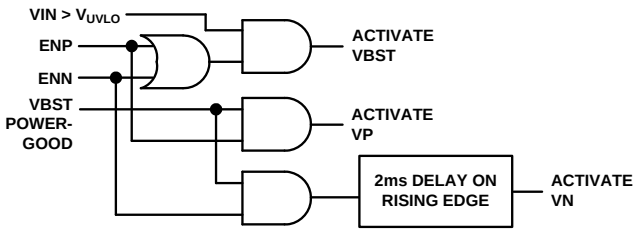


FIGURE 22. POWER-ON LOGIC OPERATION

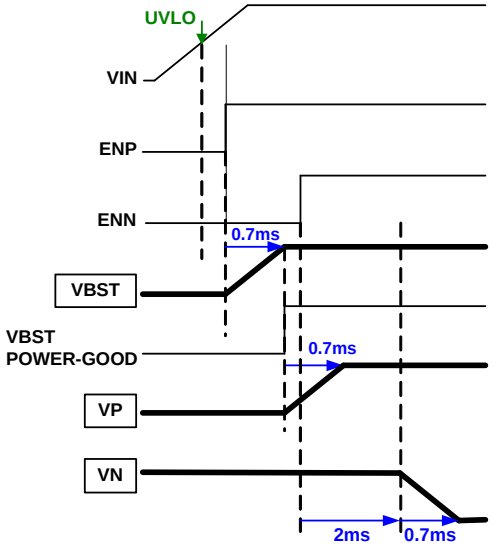


FIGURE 23. POWER-ON SEQUENCE - ENN RISING AFTER VP SOFT-START FINISHED

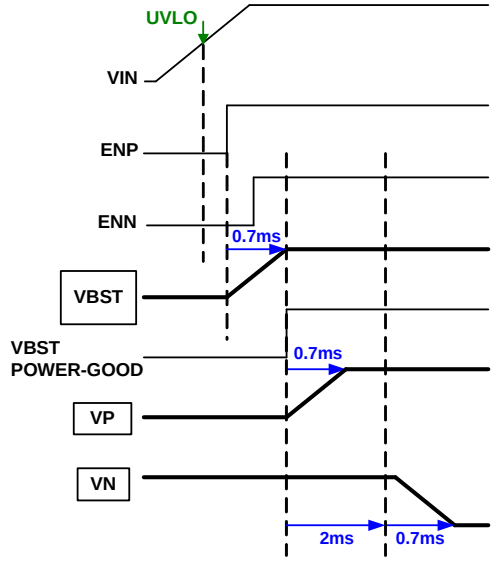


FIGURE 24. POWER-ON SEQUENCE - BOTH ENP AND ENN RISING BEFORE VBST SOFT-START FINISHED

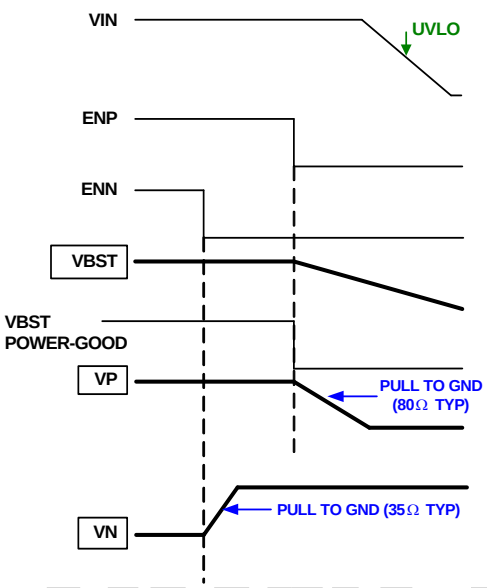


FIGURE 25. POWER-OFF SEQUENCE - ACTIVATED BY ENP AND ENN WHEN V_{IN} IS ABOVE UVLO

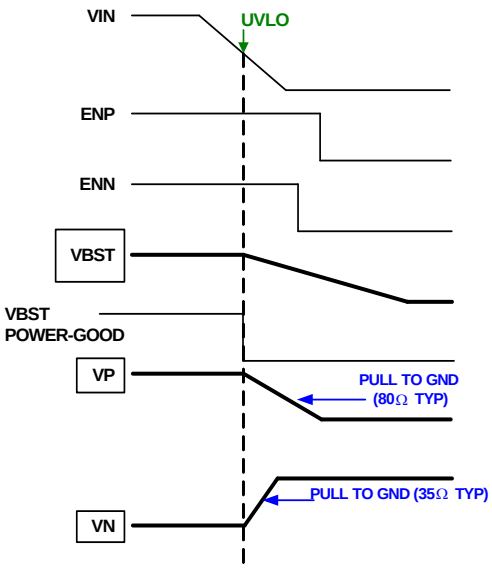


FIGURE 26. POWER-OFF SEQUENCE - ACTIVATED BY V_{IN} FALLING BELOW UVLO

Enable Timing Control Options

There are several ways to control enable sequencing of the VP and VN regulators: I^2C control, and dual or single GPIO control.

I^2C CONTROL

By using I^2C, the sequencing of the VP and VN regulator can be controlled by writing to the register 0x05. Bit $<b_1>$ controls the VN regulator and $<b_2>$ controls the VP regulator. Setting the bits to '1' will enable the regulator and setting to '0' will shut off/disable the regulator. Delaying the writes for setting bit $<b_1>$ and $<b_2>$ (using separate I^2C transactions) will delay the turn on/off sequence of VP and VN accordingly.

Figure 27 shows a 4ms delay between when VP and VN turn on. The 4ms time is an example delay to show the power-ON sequencing possibility through I^2C. This delay is set between the separate I^2C writes to set the enable bits in register 0x05. If both enable bits were set to '1' in the same I^2C transaction (same byte), and ENN and ENP are HIGH, then both VP and VN regulators will start at the same time - when the data is latched at the STOP condition.

Figure 28 shows a 2.5ms delay between the VP and VN turn off. The 2.5ms time is an example delay to show the power-OFF sequencing possibility using I^2C.

Figures 29 (zoom in) and 30 (zoom out) show a typical I^2C data transfer to the ENABLE register. In this example, VP and VN regulators are enabled by writing data 0x07 to register address 0x05. The VP regulator will be enabled first after the I^2C STOP condition, followed by the VN regulator after the internal 2ms delay.

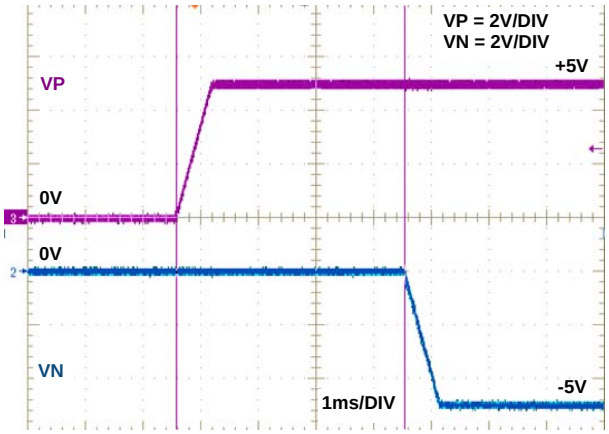


FIGURE 27. ON SEQUENCE - I^2C CONTROL

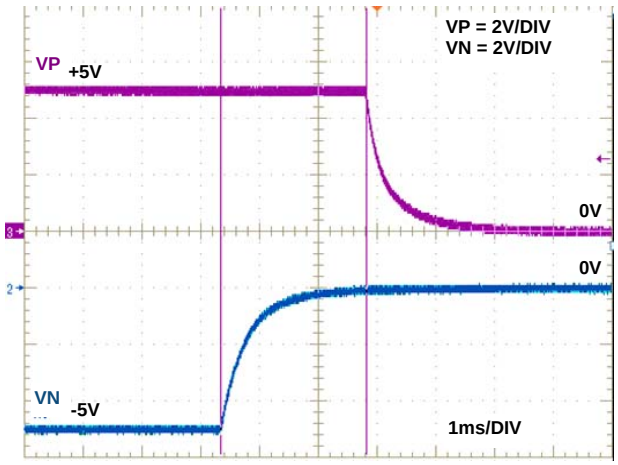


FIGURE 28. OFF SEQUENCE - I²C CONTROL

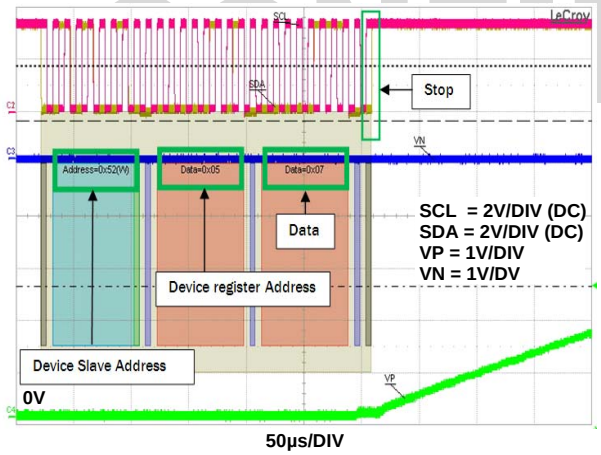


FIGURE 29. I²C SEQUENCE AND VP RESPONSE

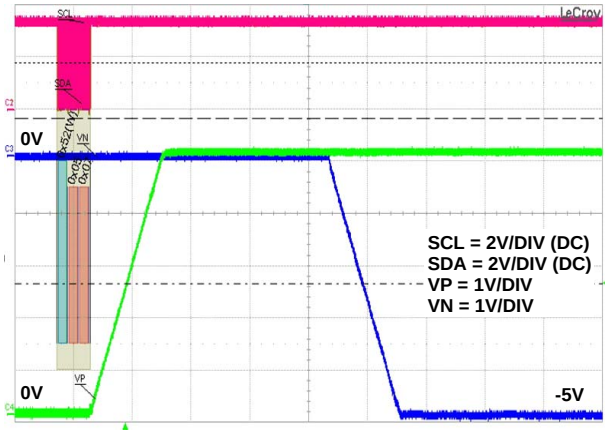


FIGURE 30. I²C SEQUENCE AND VP/VN RESPONSE

SEPARATE ENP AND ENN PINS (2 GPIO CONTROL)

Using two separate GPIO's, and controlling the timing between the ENP and ENN pins, the turn on/off events can be controlled. The method to control turn on/off by GPIO is valid when the respective enable bits in the ENABLE register at Register Address 0x05 are set to '1' (default). So, this method can be used at IC power-ON - no I²C communication is required.

By design, the VN regulator will turn on 2ms after the ENN signal goes HIGH.

Figure 31 shows a 5ms delay (example) between the ENP and ENN rise. VN turns on 2ms after ENN.

Figure 32 shows a 5ms delay (example) between the ENP and ENN fall.

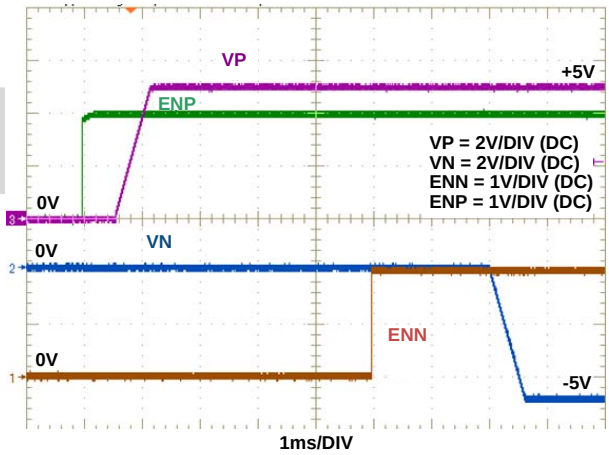


FIGURE 31. ON SEQUENCE - 2 GPIO CONTROL

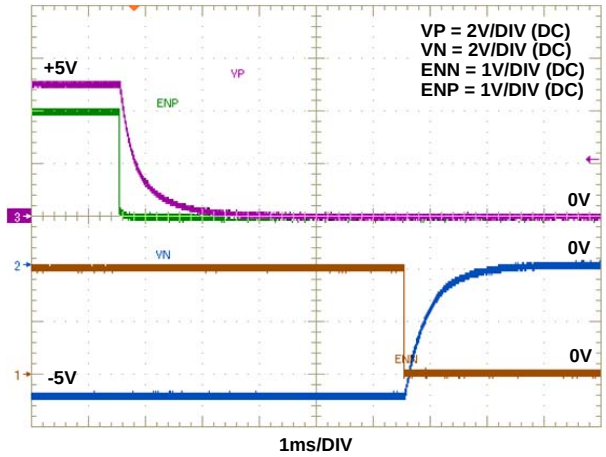


FIGURE 32. OFF SEQUENCE - 2 GPIO CONTROL

TIE ENP AND ENN TOGETHER (1 GPIO CONTROL)

There is also an option to sequence the VN and VP regulators if there is only a single GPIO available in the system. The method to control turn on/off by GPIO is valid when the respective enable bits in the ENABLE register at Register Address 0x05 are set to '1' (default). Therefore, this method can be used at IC power-ON - no I^2C communication is required.

If the ENP and ENN are tied together and both pulled HIGH, there is a default delay sequence in the IC. VP will come up first and after 2ms VN will soft-start. For turn-off, both VN and VP start to shut down together but the decay in the VP and VN voltage can be controlled using the output capacitance value.

Figure 33 shows turn-on when the ENN and ENP pins tied together. There is 2ms delay between VP and VN turning on.

Figure 34 shows turn-off when the ENN and ENP are tied together.

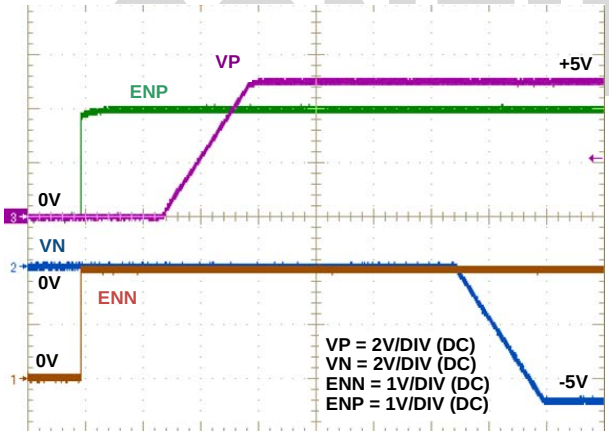


FIGURE 33. ON SEQUENCE - 1 GPIO CONTROL

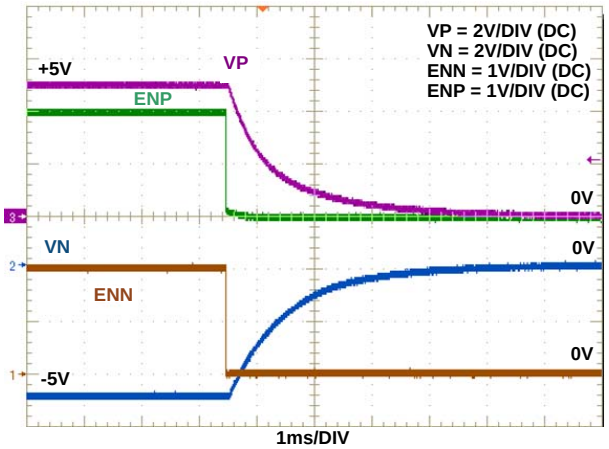


FIGURE 34. OFF SEQUENCE - 1 GPIO CONTROL

VP Output Hi-Z Mode

The ISL98607R5576 VP regulator can be configured in a Hi-Z mode for when the regulators are turned off. Using I^2C, bit <b_6> in the ENABLE register can be set to '1' to disable the internal pull-down resistor - this is "Hi-Z Mode."

Configuring the VP regulator in Hi-Z mode will prevent any leakage current flowing between VP and VN when the TFT-LCD is in sleep/standby mode. This is ideal to minimize system power consumption.

Component Selection

The design of the boost converter is simplified by an internal compensation scheme, which allows easy system design without complicated calculations. Select component values using the following recommendations.

INPUT CAPACITOR

It is recommended that a 10µF X5R/X7R or equivalent ceramic capacitor is placed on the V_{IN} input supply.

INDUCTOR

First, determine the minimum inductor saturation current required for the application.

The ISL98607R5576 operates in continuous conduction mode (CCM) at higher load current, and in discontinuous conduction mode (DCM) and PFM mode at lighter loads.

In CCM, we can calculate the peak inductor current using Equations 4 through 8.

Given these parameters:

a. Input Voltage = V_{IN}
b. Output Voltage = V_O
c. Duty Cycle = D
d. Switching Frequency = f_{SW}
e. $t_{SW} = 1/f_{SW}$

Then the inductor ripple can be calculated as:

$$\Delta I_{P-P} = (V_{IN})*(D)/(L*f_{SW}) \quad \text{(EQ. 4)}$$

where $D = 1 - (V_{IN}/V_O)$, then rewrite Equation 4:

$$\Delta I_{P-P} = (V_{IN})*(V_O - V_{IN})/(L*f_{SW}*V_O) \quad \text{(EQ. 5)}$$

The average inductor current is equal to the average input current, where I_{IAVG} can be calculated from the efficiency of the converter.

$$I_{IAVG} = (V_O*I_O)/(V_{IN}*\text{Efficiency}) \quad \text{(EQ. 6)}$$

To find the peak inductor current write the expression as:

$$I_{Pk} = \Delta I_{P-P}/2 + I_{IAVG} \quad \text{(EQ. 7)}$$

Substituting Equations 5 and 6 in Equation 7 to calculate I_{Pk}.

$$I_{PK} = 0.5*V_{IN}*(V_O - V_{IN})/(L*f_{SW}*V_O) + (V_O*I_O)/(V_{IN}*EFF) \quad \text{(EQ. 8)}$$

Example:

Consider the following parameters in the steady state boost regulator operating in CCM mode.

V_{IN} = 2.8V

V_O = 5.65V

f_{SW} = 1.45MHz

Output load current = 100mA

Efficiency = 80%

L = 4.7µH

Substituting previous parameters in Equation 8 gives us:

I_{Pk} = 355mA

The ISL98607R5576 boost regulator operates in DCM and PFM mode at light load. In PFM mode, it uses a fixed peak inductor current of ~340mA.

In order to avoid the inductor core saturation, the saturation current of the inductor selected should be higher than the greater of the peak inductor current (for CCM) and the 340mA peak current in PFM mode.

The 340mA peak inductor current in PFM mode is optimized to provide maximum efficiency with a 4.7µH inductor value. If a smaller inductor is used, less energy will be delivered per cycle, the ISL98607R5576 will switch at a higher frequency, and the efficiency will reduce. Increasing the inductor will increase the energy delivered per pulse. But for a given inductor size the DC-resistance (DCR) increases with inductor value, so the conduction losses will increase. L = 4.7µH is the optimal value for ISL98607R5576.

Table 3 shows the recommended inductors for typical ISL98607R5576 applications - small size, handheld TFT-LCD display power.

TABLE 3. RECOMMENDED INDUCTOR

INDUCTOR PART NUMBER	INDUCTANCE (µH)	DCR (mΩ)	I_{SAT} (A)	FOOTPRINT SIZE
1239AS-H-4R7M (Toko)	4.7	200	1.90	2520

OUTPUT CAPACITOR

The output capacitor supplies current to the load during transient conditions, and reduces the ripple voltage at the output. Output ripple voltage consists of two components:

1. The voltage drop due to the inductor ripple current flowing through the ESR of the output capacitor.
2. Charging and discharging of the output capacitor.

For low ESR ceramic capacitors, the output ripple is dominated by the charging and discharging of the output capacitor. The voltage rating of the output capacitor should be greater than the maximum output voltage.

Note: Capacitors have a voltage coefficient. The effective capacitance will reduce (derate) as the operating voltage/bias increases. Always refer to the manufacturer's derating information to determine effective capacitance for the operating conditions.

The effective capacitance at the nominal output voltage should be 2.2µF for VBST and VP regulator, and 4.4µF for VN. It is recommended to use a 10µF X5R 10V or equivalent ceramic output capacitor for both VBST and VP outputs to provide a minimum of 2.2µF effective capacitance. For the VN output, it is recommended to use one or two 10µF X5R 10V or equivalent ceramic output capacitors. Using two VN output capacitors results in <50mV peak-to-peak output voltage ripple with input voltages from 2.8V to 4.4V.

TABLE 4. RECOMMENDED OUTPUT CAPACITORS

CAPACITOR PART NUMBER	VALUE (µF)	SIZE	QUANTITY
GRM155R61A106ME11 (Murata)	10	0402	x5: C_{IN}, C_{VBST}, C_{VP}, C_{VN}, C_{CP} x1: C_{VN} (x2 for minimum ripple)
GRM188R61C475KAAJ (Murata)	4.7	0603	x5: C_{IN}, C_{VBST}, C_{VP}, C_{VN}, C_{CP} x1: C_{VN} (x2 for minimum ripple)

General Layout Guidelines

When designing the printed circuit board (PCB) layout for the ISL98607R5576, it is very important to understand the power requirements of the system. Some general best practices should be adhered to in order to create an optimal PCB layout:

1. Careful consideration should be taken with any traces carrying AC signals. AC current loops should be kept as short and as tight as possible. The current loop generates a magnetic field, which can couple to another conductor, inducing unwanted voltage. Components should be placed such that current flows through them in a straight line as much as possible. This will help reduce the size of loops and reduce the EMI from the PCB.
2. If trace lengths are long, the resistance of the trace increases and can cause some reduction in IC efficiency, and can also cause system instability. Traces carrying power should be made wide and short.
3. In discontinuous conduction mode, the direction of the current is interrupted every few cycles. This may result in large di/dt (transient load current). When injected in the ground plane the current may cause voltage drops, which can interfere with sensitive circuitry. The analog ground and power ground of the IC should be connected very close to the IC to mitigate this issue.
4. One plane/layer in the PCB is recommended to be a dedicated ground plane. A large area of metal will have lower resistance, which reduces the return current impedance. More ground plane area minimizes parasitics and avoids corruption of the ground reference.
5. Low frequency digital signals should be isolated from any high frequency signals generated by switching frequency and harmonics. PCB traces should not cross each other. If they must cross due to the layout restriction, then they must cross perpendicularly to reduce the magnetic field interaction.

6. The amount of copper that should be poured (thickness) depends upon the power requirement of the system. Insufficient copper will increase resistance of the PCB, which will increase heat dissipation.
7. Generally, vias should not be used to route high current paths.
8. While designing the layout of switched controllers, do not use the auto routing function of the PCB layout software. Auto routing connects the nets with the same electrical name and does not account for ideal trace lengths and positioning.

ISL98607R5576 Specific Layout Guidelines

1. The input capacitor should be connected to the VIN pin with the smallest trace possible. This helps reject high frequency disturbances and promotes good regulation of the VBST, VP and VN regulators.
2. The boost inductor should be connected to the LXP pin with a short and wide trace. Careful consideration should be made in selecting the inductor as it may cause electromagnetic interference, which could affect IC functionality. A shielded inductor is recommended.
3. The device has two VBST pins. The CSP bumps for VBST pins are B3 and B4. B3 is the output of the boost regulator and B4 is the input for the negative charge pump. B3 and B4 should be connected/shorted to each other on the PCB with short and thick trace to avoid parasitic inductance and resistance. A 10µF/10V capacitor should be used on B3. The distance of the capacitor from the B3 and B4 bumps is critical - it should be placed very close to the IC with a short and thick trace.
4. Bump E3 is output of the negative charge pump (VN) and bump E2 is its substrate connection (VSUB). It is highly recommended that E2 and E3 are shorted together with a short and thick trace. It is recommended that 2x10µF/10V capacitors are placed on VN to minimize output ripple. Additionally, it will help minimize noise that may be coupled from the high frequency ripple of the charge pump.
5. Bumps A3 and A4 are the output of the VP regulator. It is important to connect A3 and A4 CSP bumps with short and thick trace.
6. Analog ground (AGND) and power ground (PGND) of the IC should be connected to each other. It is crucial to connect these two grounds at the location very close to the IC. Bump C1 is AGND and bumps A1, B1 are PGND. These bumps are very close and should be shorted together.
7. Digital input pins, ENN and ENP, should be isolated from the high di/dt and dv/dt signals. Otherwise, it may cause a glitch on those inputs.
8. I^2C signals, if not used, should be tied to V_{IN}.

Figure 35 shows the recommended PCB layout for a typical ISL98607R5576 application.

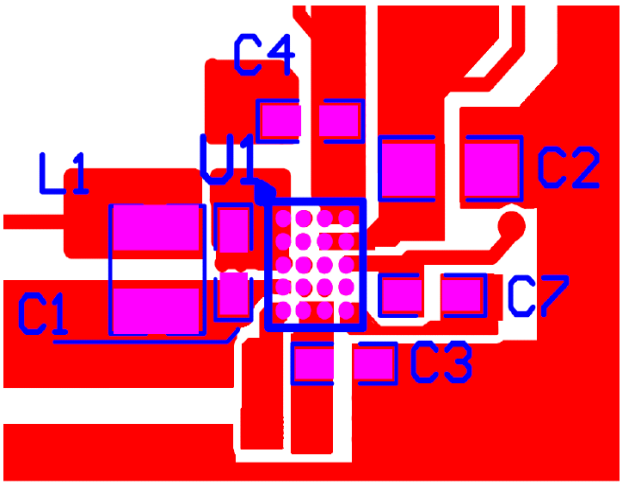


FIGURE 35. ISL98607R5576 RECOMMENDED PCB LAYOUT

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
May 7, 2014	FN8628.0	Initial Release.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

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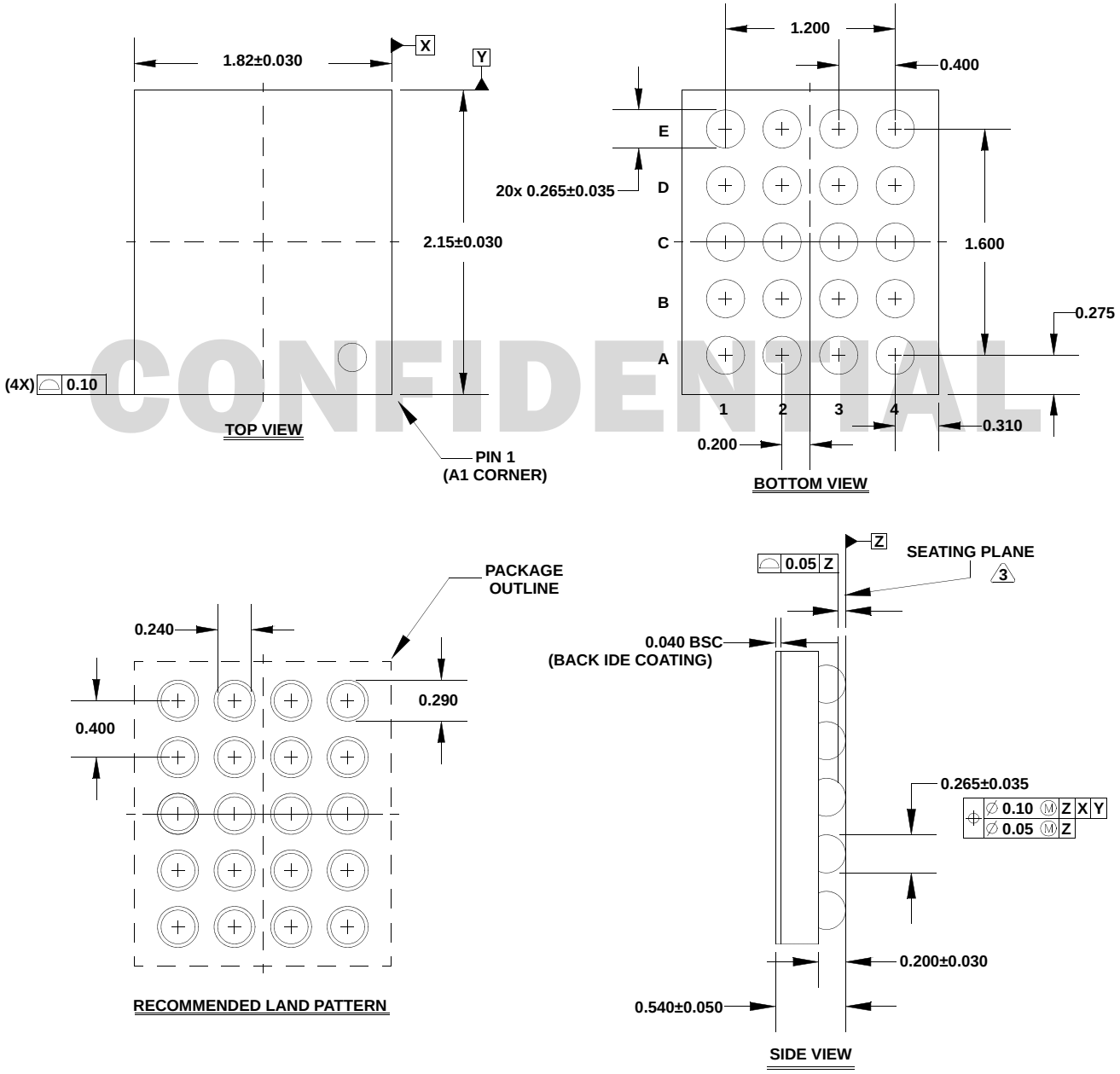
Package Outline Drawing

W4x5.20E

20 BALL WAFER LEVEL CHIP SCALE PACKAGE (WLCSP) (BSC)

Rev 1, 1/13



NOTES:

1. Dimensions and tolerance per ASME Y 14.5M - 1994.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
3. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
4. Bump position designation per JESD 95-1, SPP-010.
5. There shall be a minimum clearance of 0.10mm between the edge of the bump and the body edge.