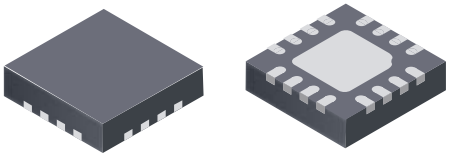
Low Voltage DC Motor Driver

Features and Benefits

- 2.5 to 9 V operation
- Internal PWM current control
- Synchronous rectification for reduced power dissipation
- Peak current output flag
- Undervoltage lockout
- Low $R_{DS(on)}$ outputs
- Small package
- Brake mode for DC motor
- Sleep function
- Crossover-current protection
- Thermal shutdown

Package: 16-contact QFN (suffix ES)



3 × 3 mm
0.75 mm overall height

Approximate size

Description

Designed for pulse width modulated (PWM) control of a low voltage DC motor, the A3918 is capable of output currents up to 1.5 A and operating voltages from 2.5 to 9 V.

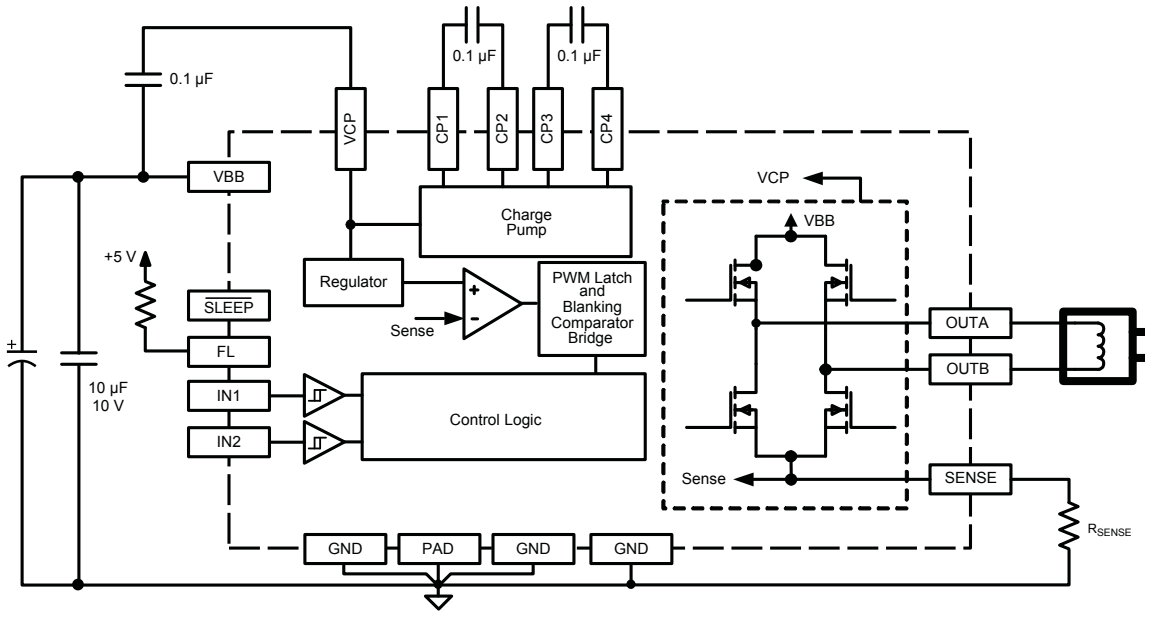
The A3918 has an internal fixed off-time PWM timer that sets a peak current based on the selection of a current sense resistor. An overcurrent output flag is provided that notifies the user when the current in the motor winding reaches the peak current determined by the sense resistor. The fault output does not affect driver operation.

The A3918 is provided in a 16-contact, 3 mm × 3 mm, 0.75 mm nominal overall height QFN, with exposed pad for enhanced thermal dissipation. It is lead (Pb) free, with 100% matte tin leadframe plating.

Applications include the following:

- Digital still cameras (DSC)
- Cell phone cameras
- USB powered devices
- Battery powered devices

Functional Block Diagram



Selection Guide

Part Number	Packing	Package
A3918SESTR-T	1500 pieces per 7-in. reel	16-pin QFN with exposed thermal pad

Absolute Maximum Ratings

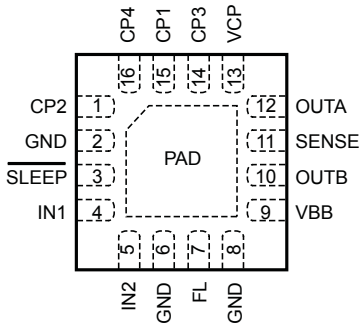
Characteristic	Symbol	Notes		Rating	Units
Load Supply Voltage	V_{BB}			9.6	V
Logic Input Voltage Range	V_{IN}			–0.3 to 7	V
Sense Voltage	V_{SENSE}	Continuous		0.5	V
		Pulsed, t_w < 1 µs		1	V
Output Current	I_{OUT}	May be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or a junction temperature of 150°C.	Continuous	1	A
			Peak, DC < 30%	1.5	A
Operating Temperature Range	T_A	Range S		–20 to 85	°C
Junction Temperature	$T_{J(max)}$			150	°C
Storage Temperature Range	T_{stg}			–40 to 150	°C

Thermal Characteristics may require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	4-layer PCB based on JEDEC standard	42	ºC/W

*Additional thermal information available on the Allegro website.

Pin-out Diagram



Terminal List Table

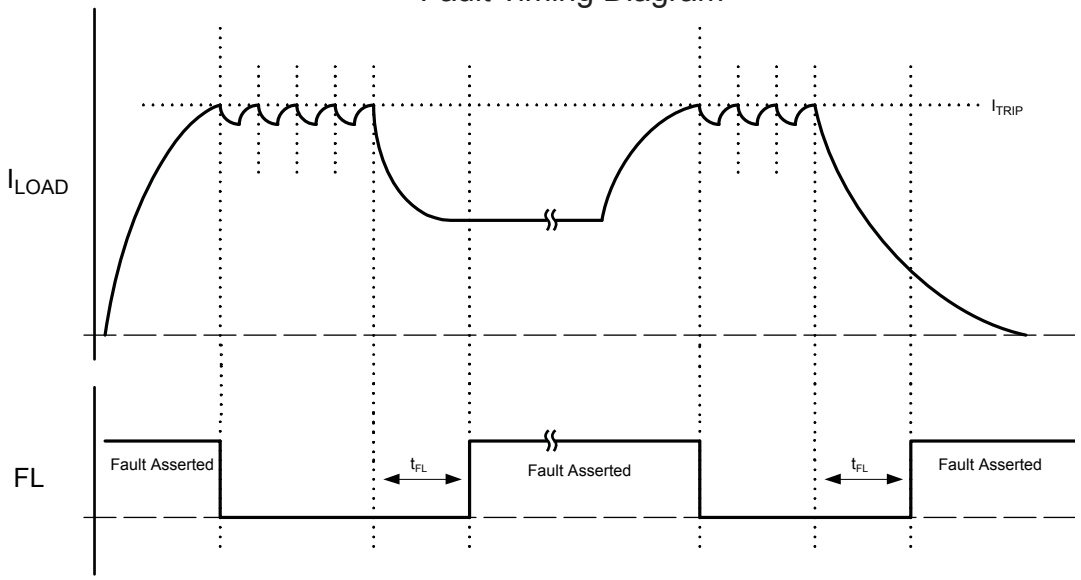
Name	Number	Function
CP1	15	Charge pump capacitor terminal 1
CP2	1	Charge pump capacitor terminal 2
CP3	14	Charge pump capacitor terminal 3
CP4	16	Charge pump capacitor terminal 4
FL	7	Current limit flag
GND	2, 6, 8	Ground
IN1	4	Control input 1
IN2	5	Control input 2
OUTA	12	DMOS full-bridge output A
OUTB	10	DMOS full-bridge output B
PAD	–	Exposed thermal pad
SENSE	11	Current sense resistor terminal
$\overline{\text{SLEEP}}$	3	Sleep logic input, active low
VBB	9	Supply Voltage
VCP	13	Reservoir capacitor terminal

ELECTRICAL CHARACTERISTICS[1,2] valid at T_A = 25°C and V_{BB} = 2.5 to 9 V, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Operating Voltage Range	V_{BB}		2.5	–	9	V
VBB Supply Current	I_{BB}	I_{OUT} = 0 mA, PWM = 50 kHz, Duty Cycle = 50%	–	5	–	mA
		I_{OUT} = 0 mA, outputs disabled, V_{BB} = 9.6 V	–	3	–	mA
		Sleep mode, V_{IN} < 0.4 V	–	150	500	nA
Output Resistance	$R_{DS(on)}$	Source driver, I_{OUT} = 400 mA , V_{BB} = 3 V, T_J = 25°C	–	0.52	0.60	Ω
		Source driver, I_{OUT} = 400 mA , V_{BB} = 3 V, T_J = 85°C	–	0.78	–	Ω
		Sink driver, I_{OUT} = 400 mA, V_{BB} = 3 V, T_J= 25°C	–	0.62	0.74	Ω
		Sink driver, I_{OUT} = 400 mA, V_{BB} = 3 V, T_J= 85°C	–	0.93	–	Ω
Current Trip Sense Voltage	V_{SENSE}	FL falling edge	160	200	240	mV
Clamp Diode Voltage	V_f	I = 400 mA	–	–	1	V
Output Leakage Current	I_{DSS}	Outputs, V_{OUT} = 9 V	–20	–	20	µA
Control Logic						
Logic Input Voltage	$V_{IN(1)}$		2.0	–	5.5	V
	$V_{IN(0)}$		–	–	0.8	V
Logic Input Current	$I_{IN(1)}$	V_{IN} = 5.5 V	–	<100	500	nA
	$I_{IN(0)}$	V_{IN} = 0.8 V	–	<–100	–500	nA
Input Hysteresis	V_{INhys}		–	150	–	mV
$\overline{\text{SLEEP}}$ Input	$V_{SLEEP(0)}$		–	–	0.4	V
	$V_{SLEEP(1)}$		2	–	–	V
Fault Output	V_{FL}	Flag asserted, I_{FL} = 1 mA	–	–	200	mV
Fault Output Leakage Current	I_{FL}	V_{FL} = 5 V	–	–	1	µA
Fault Output Timer	t_{FL}	Reset of PWM latch	–	300	–	µs
Blank Time	t_{BLANK}		2.1	3	3.9	µs
Fixed Off-Time	t_{OFF}		–	30	–	µs
Propagation Delay Time	$t_{pd(on)}$	Input high to source on, input low to source off	100	235	350	ns
	$t_{pd(off)}$	Input low to sink off, input high to sink on	50	100	200	ns
Protection Circuitry						
Crossover Delay	t_{COD}		200	425	650	ns
VBB Undervoltage Lockout Threshold	V_{BBUVLO}	V_{BB} rising	2.2	2.31	2.45	V
VBB Undervoltage Lockout Hysteresis	$V_{BBUVHYS}$		200	300	400	mV
Thermal Shutdown Temperature	T_{JTSD}		–	165	–	°C
Thermal Shutdown Hysteresis	$T_{JTSDHYS}$		–	15	–	°C

[1]For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.
[2]Specifications over the operating temperature range are assured by design and characterization.

Fault Timing Diagram



NOTE: Timer resets after each reset of the PWM latch.

Control Logic

DC Motor Operation

IN1	IN2	OUTA	OUTB	Function
0	0	Off	Off	Disabled
1	0	High	Low	Forward
0	1	Low	High	Reverse
1	1	Low	Low	Brake

Functional Description

Device Operation The A3918 is a full-bridge low voltage motor driver capable of operating one high current DC motor. MOSFET output stages substantially reduce the voltage drop and the power dissipation of the outputs of the A3918, compared to typical drivers with bipolar transistors.

Output current can be regulated by pulse width modulating (PWM) the inputs. In addition supporting external PWM of the driver, the A3918 limits the peak current by internally PWMing the source driver when the current in the winding exceeds the peak current, which is determined by a sense resistor. A fault output notifies the user that peak current was reached. If internal current limiting is not needed, the sense pin should be shorted to ground.

Internal circuit protection includes thermal shutdown with hysteresis, undervoltage lockout, internal clamp diodes, and crossover current protection.

The A3918 is designed for portable applications, providing a power-off low current sleep mode and an operating voltage of 2.5 to 9 V.

External PWM Output current regulation can be achieved by pulse width modulating the inputs. Slow decay mode is selected by holding one input high while PWMing the other input. Holding one input low and PWMing the other input results in fast decay. Refer to the Applications Information section for further information.

Blanking This function blanks the output of the current sense comparator when the outputs are switched. The comparator output is blanked to prevent false overcurrent detections due to reverse recovery currents of the clamp diodes or to switching transients related to the capacitance of the load. The blank time, t_{BLANK}, is approximately 3 µs.

Sleep Mode An active-low control input used to minimize power consumption when the A3918 is not in use. This disables much of the internal circuitry including the output drivers, internal regulator, and charge pump. A logic high allows normal operation. When coming out of sleep mode, wait 1.5 ms before issuing a command, to allow the internal regulator and charge pump to stabilize.

Enable When all logic inputs are pulled to logic low, the outputs of the bridges are disabled. The charge pump and internal circuitry continue to run when the outputs are disabled.

Charge Pump (CP1, CP2, CP3, and CP4) When supply voltages are lower than 3.5 V, the two-stage charge pump triples the input voltage to a maximum of 7 V above the supply. The charge pump is used to create a supply voltage greater than V_{BB}, to drive the source-side DMOS gates. For pumping purposes, a 0.1 µF ceramic capacitor should be connected between CP1 and CP2, and between CP3 and CP4. A 0.1 uF ceramic capacitor is required between VCP and VBB, to act as a reservoir to operate the high-side DMOS devices.

Thermal Shutdown The A3918 will disable the outputs if the junction temperature reaches 165°C. When the junction temperature drops 15°C, the outputs will be enabled.

Brake Mode When driving DC motors, the A3918 goes into brake mode (turns on both sink drivers) when both of its inputs are high (IN1 and IN2). There is no protection during braking, so care must be taken to ensure that the peak current during braking does not exceed the absolute maximum current.

Internal PWM Current Control The bridge is controlled by a fixed off-time PWM current control circuit that limits the load current to a desired value, I_{TRIP}. Initially, a diagonal pair of source and sink DMOS outputs are enabled and current flows through the motor winding and the current sense resistor, R_{SENSE}. When the voltage across R_{SENSE} equals the internal reference voltage, the current sense comparator resets the PWM latch, which turns off the source driver.

The maximum value of current limiting, $I_{TRIP}(max)$, is set by the selection of the sense resistor, R_{SENSE}, and is approximated by a transconductance function:

$$I_{TRIP}(max) = 0.2 / R_{SENSE} \quad .$$

It is critical to ensure the maximum rating on the SENSE pin (0.5 V) is not exceeded.

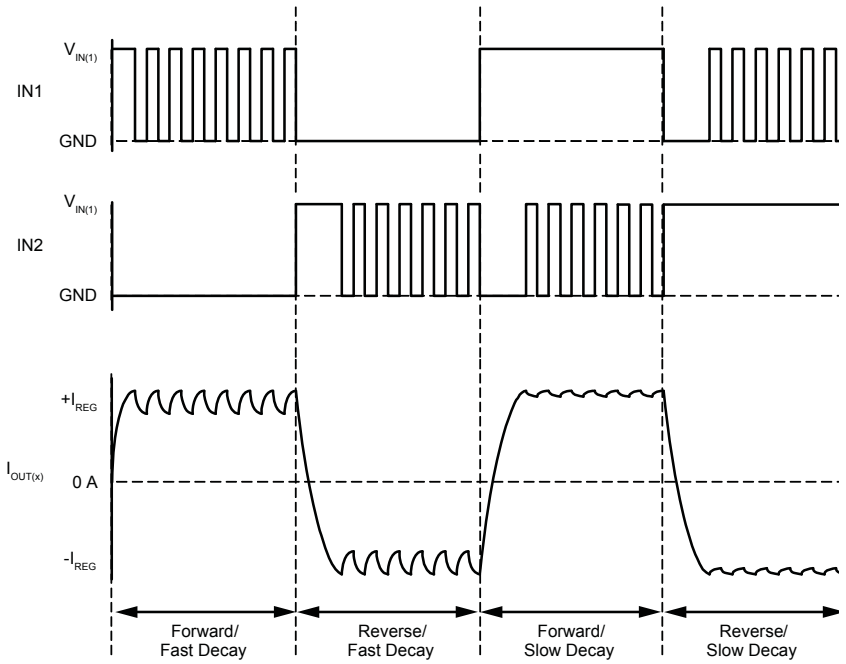
Synchronous Rectification When a PWM off-cycle is triggered by an internal fixed off-time cycle, load current recirculates in slow decay SR mode. During slow decay, current recirculates through the sink-side FET and the sink-side body diode. The SR feature enables the sink-side FET, effectively shorting out the body diode. The sink driver is not enabled until the source driver is turned off and the crossover delay has expired. This feature helps lower the voltage drop during current recirculation, lowering power dissipation in the bridge.

Overcurrent Output Flag When the peak current (set by the external resistor) is reached, the fault pin, FL, is pulled low. When a reset of the PWM latch occurs, the fault timer begins. At each PWM latch reset, the timer is reset to zero. After approximately 300 µs, if no peak current event was triggered, the timer expires and the fault is released. This ensures that during PWM current limiting, the fault pin remains in a fault state.

Applications Information

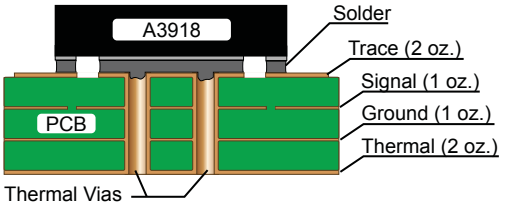
External PWM If external PWM is used, the internal current control can either be disabled by shorting the SENSE pin to ground, or it can be used to limit the peak current to a value under the stall current to prevent motor heating. External PWM of IN1/IN2 control is shown in the figure below.

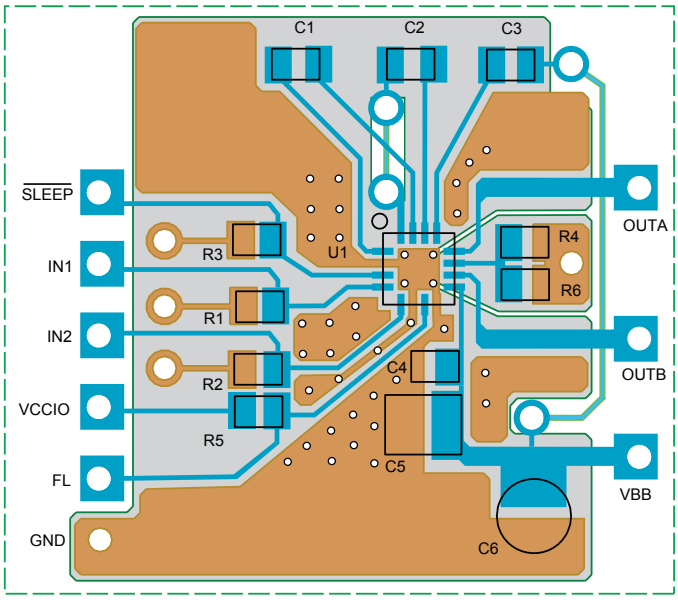
PWM current control in fast and slow decay modes



Layout The printed circuit board should use a heavy ground-plane. For optimum electrical and thermal performance, the A3918 must be soldered directly onto the board. On the underside of the A3918 package is an exposed pad, which provides a path for enhanced thermal dissipation. The thermal pad should be soldered directly to an exposed surface on the PCB. Thermal vias are used to transfer heat to other layers of the PCB.

Grounding In order to minimize the effects of ground bounce and offset issues, it is important to have a low impedance single-point ground, known as a *star ground*, located very close to the device. By making the connection between the exposed thermal pad and the ground plane directly under the A3918, that area becomes an ideal location for a star ground point. A low impedance ground will prevent ground bounce during high current operation and ensure that the supply voltage remains stable at the input terminal. The recommended PCB layout shown in the diagram below, illustrates how to create a star ground under the device, to serve both as low impedance ground point and thermal path.

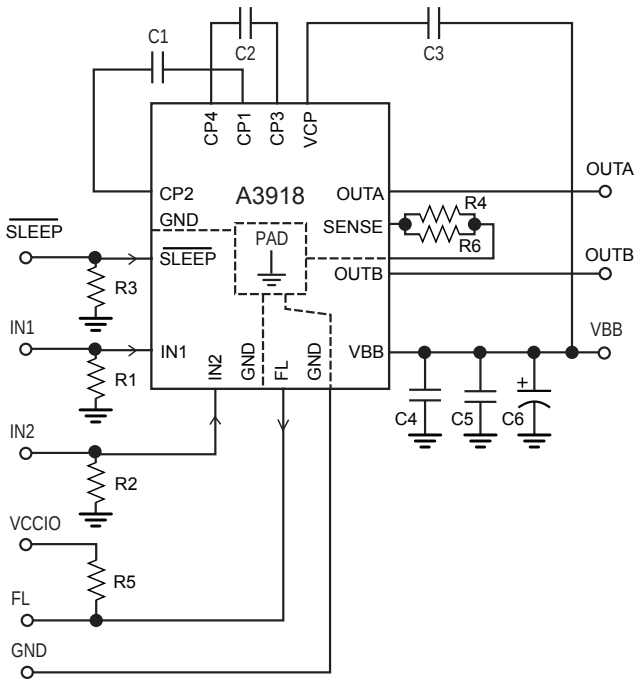




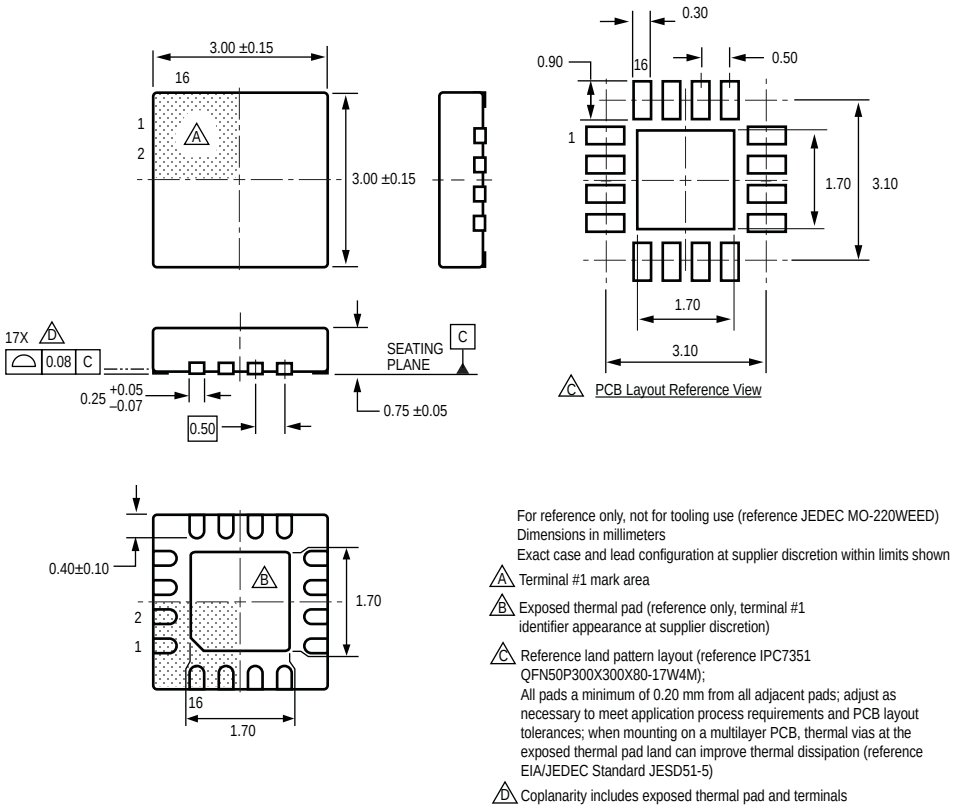
The two input capacitors should be placed in parallel, and as close to the device supply pin as possible. The ceramic capacitor should be closer to the pin than the bulk capacitor. This is necessary because the ceramic capacitor will be responsible for delivering the high frequency current components.

Sense Pin The sense resistor, R_{SENSE}, should have a very low impedance path to ground, because it must carry a large current while supporting very accurate voltage measurements by the current sense comparator. Long ground traces will cause additional voltage drops, adversely affecting the ability of the comparator to accurately measure the current in the winding. As shown in the layout below, the SENSE pin has very short traces to the R_{SENSE} resistor and very thick, low impedance traces directly to the star ground underneath the device. If possible, there should be no other components on the sense circuit.

Note: When selecting a value for the sense resistor, be sure not to exceed the maximum voltage on the SENSE pin of ±500 mV.



ES Package, 16-Contact QFN with Exposed Thermal Pad



For reference only, not for tooling use (reference JEDEC MO-220WEED)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P300X300X80-17W4M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

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