Integrated Over Voltage Protection Circuit

General Description

The RT9709 is an integrated circuit (IC) optimized to protect low voltage system from abnormal high voltage input up to 28V. The IC monitors the input voltage, battery voltage and the charging current to make sure all three parameters are operated in normal range. It also monitors its own temperature and turns the MOSFET off when the chip temperature exceeds 140°C.

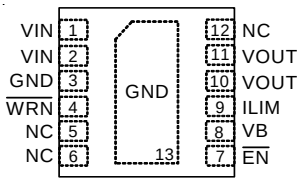
The RT9709 can support AC charger or USB charger. When the input voltage exceeds the OVP threshold, the IC turns off the MOSFET within 1us to remove the power before any damage occurs.

The current in the MOSFET is also limited to prevent charging the battery with an excessive current. The current limit can be programmed by an external resistor between ILIM and GND. The OCP function has a 4-bit binary counter that accumulates during an OCP event. When the total count reaches 16 times, the MOSFET will be turned off permanently unless the input power is recycled.

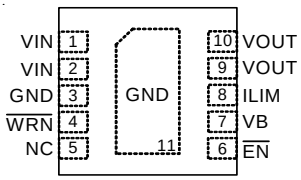
The IC also monitors the battery voltage VB. When the battery voltage exceeds 4.4V and last for more than 180us the RT9709 will turn off the MOSFET. The internal logic control will turn off and latch the MOSFET when the battery over-voltage event reaches 16 times.

Pin Configurations

(TOP VIEW)



WDFN-12L 4x3



WDFN-10L 3x3

Features

- **Fully Integrated Protection Circuit for Three Protection Variables**
  - **User Programmable OCP Threshold**
  - **Input OVP Less than 1us**
  - **Battery OVP**
- **Up to 30V Over Voltage Protection**
- **High Accuracy Protection Threshold**
- **High Immunity of False Triggering Under Transients**
- **Warning Indication Output**
- **Enable Input**
- **Thermally Enhanced WDFN Package**
- **RoHS Compliant and Halogen Free**

Applications

- Cellular Phones
- Digital Cameras
- PDAs and Smart Phones
- Portable Instruments

Ordering Information

RT9709□□□

- Package Type
  - QW : WDFN-12L 4x3 (W-Type)
  - QWB : WDFN-10L 3x3 (W-Type)
- Lead Plating System
  - G : Green (Halogen Free and Pb Free)
- OVP
  - Default : 6.8V
  - A : 5.85V
  - B : 6.25V

Note :

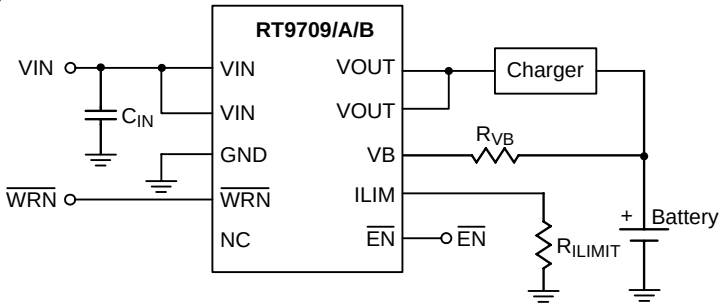
Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

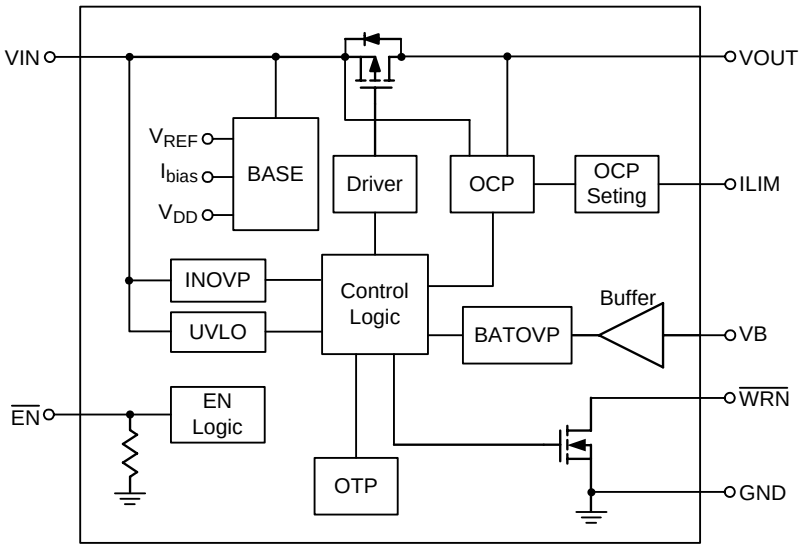
Typical Application Circuit



Functional Pin Description

Pin No.		Pin Name	Pin Function
WDFN-12L 4x3	WDFN-10L 3x3		
1, 2	1, 2	VIN	Input Power Source Pin.
3	3	GND	Ground Pin.
4	4	$\overline{WRN}$	This is an open-drain logic output that turns LOW when any protection event occurs.
5, 6, 12	5	NC	No Internal Connection.
7	6	$\overline{EN}$	Enable Input Pin. Pull this pin to low or leave it floating to enable the IC. Force this pin to high to disable the IC.
8	7	VB	Battery Voltage Monitoring Input Pin. This pin is connected to the battery pack positive terminal via resistor.
9	8	ILIM	Over-Current Protection Threshold Setting Pin. Connect a resistor between this pin and GND to set the OCP threshold.
10, 11	9, 10	VOUT	Output Voltage Pin. Output through the MOSFET.
13 (Expose Pad)	11 (Exposed Pad)	GND	The exposed pad must be soldered to a large PCB and connected to GND for maximum thermal dissipation.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V_{IN} ---------- –0.3V to 30V
- VOUT, VB ---------- –0.3V to 7V
- Other Pins ---------- –0.3V to 5.5V
- Power Dissipation, P_D @ T_A = 25°C
  - WDFN-10L 3x3 ---------- 1.429W
  - WDFN-12L 4x3 ---------- 1.667W
- Package Thermal Resistance (Note 2)
  - WDFN-10L 3x3, θ_{JA} ---------- 70°C/W
  - WDFN-10L 3x3, θ_{JC} ---------- 7°C/W
  - WDFN-12L 4x3, θ_{JA} ---------- 60°C/W
  - WDFN-12L 4x3, θ_{JC} ---------- 7°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Mode) ---------- 3kV
  - MM (Machine Mode) ---------- 250V

Recommended Operating Conditions (Note 4)

- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 5V, C_{IN} = 1uF, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Units
Power- On Reset							
Operation Voltage	RT9709	V_{IN}		4.3	--	6.5	V
	RT9709A			4.3	--	5.5	V
	RT9709B			4.3	--	5.9	V
Under Voltage Lockout Threshold		V_{UVLO}	V_{IN} Rising	2.4	2.6	2.7	V
			Hysteresis	--	100	--	mV
Quiescent Current		I_Q	When Enable, V_{EN} < 0.4V	--	0.5	1	mA
Shutdown Current		I_{Q_SD}	When Disable, V_{EN} > 1.5V	30	60	100	uA
Protections							
Input OVP Reference Voltage	RT9709	V_{OVP}		6.65	6.8	7.0	V
	RT9709A			5.65	5.85	6.0	V
	RT9709B			6	6.25	6.5	V
Input OVP Hysteresis				--	60	100	mV
Input OVP Propagation Delay			V_{OUT} = V_{IN} x 80%	--	--	1	us
Over Current Protection		I_{OCP}		0.93	1	1.07	A
Over Current Protection Blanking Time		BT_{OCP}		--	170	--	us

To be continued

Parameter		Symbol	Test Conditions	Min	Typ	Max	Units
Battery Over Voltage Protection		VB_{OVP}	Threshold	4.3	4.35	4.4	V
			Hysteresis	--	30	--	mV
Battery OVP Blanking time		BT_{OVP}		--	180	--	us
VB Pin Leakage Current			V_{VB} = 4.4V	--	--	100	nA
OTP Threshold		T_{SD}	Rising	--	140	--	°C
			Falling	--	90	--	°C
Logic							
EN/ Threshold	Logic-High Voltage	V_{IH}		1.5	--	--	V
	Logic-Low Voltage	V_{IL}		--	--	0.4	V
EN/ Internal Pull Down Resistor				100	200	400	kΩ
WRN/ Output Logic Low			Sink 5mA	--	0.35	0.8	V
WRN Output Logic High Leakage Current				--	--	1	uA
Power MOSFET							
On Resistance (P-MOSFET)		R_{ON1}	I_{OUT} = 500mA, 4.3V < V_{IN} < 6.5V	--	200	400	mΩ

Note 1. Stresses beyond those listed under **"**Absolute Maximum Ratings**"** may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

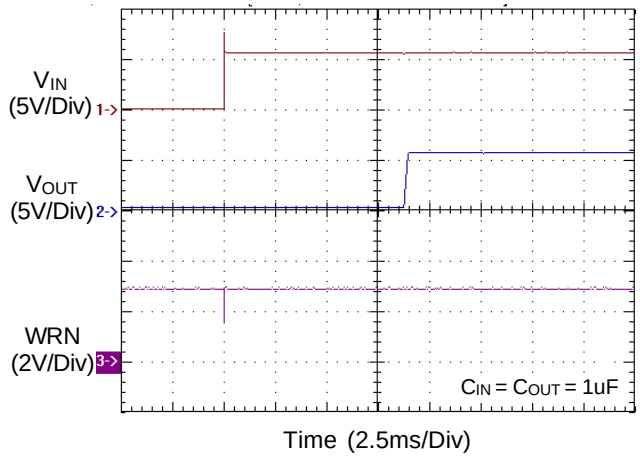
Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective four layers thermal conductivity test board of JEDEC 51-7 thermal measurement standard. The case position of θ_{JC} is on the exposed pad of the packages.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

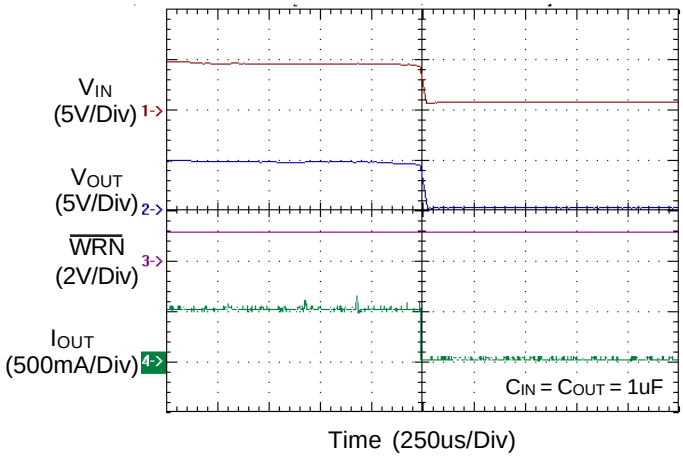
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

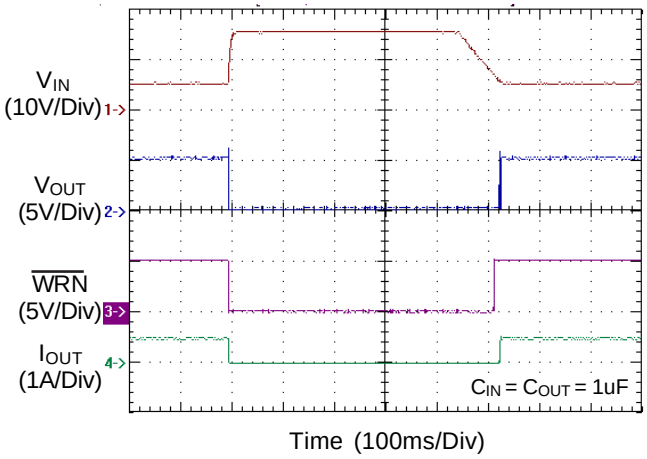
Power On from V_{IN}



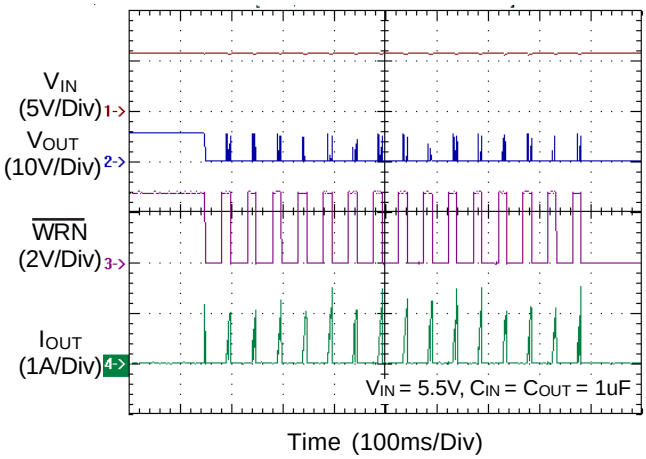
Power Off from V_{IN}



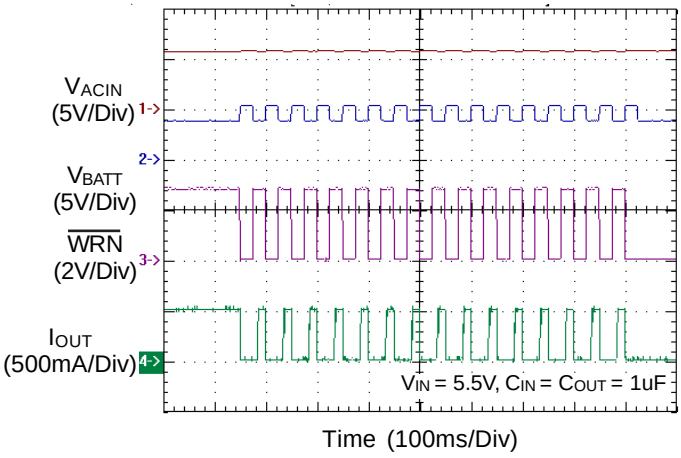
Input OVP



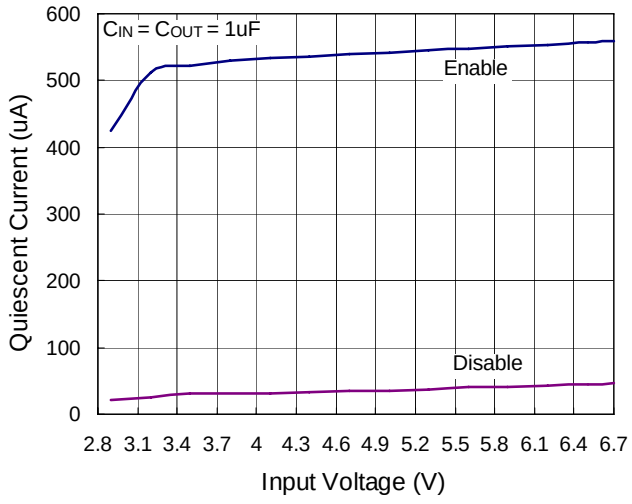
OCP



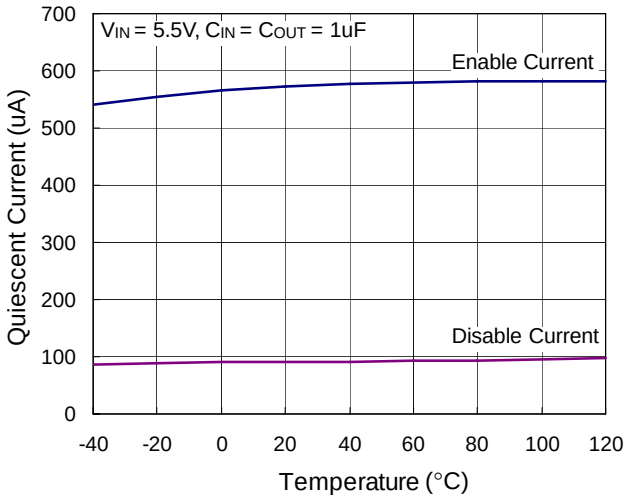
Battery OVP



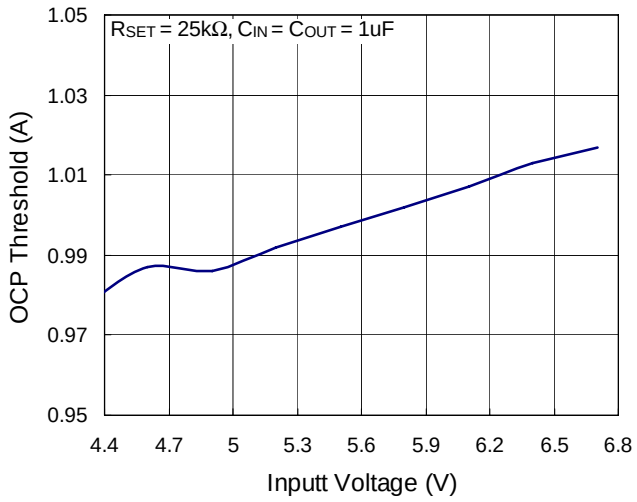
Quiescent Current vs. Input Voltage



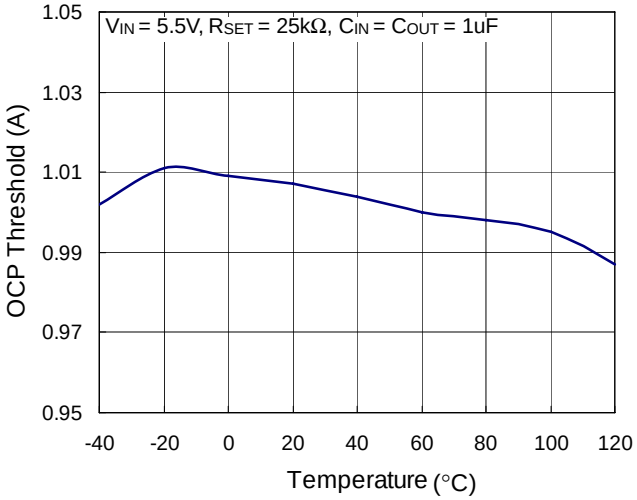
Quiescent Current vs. Temperature



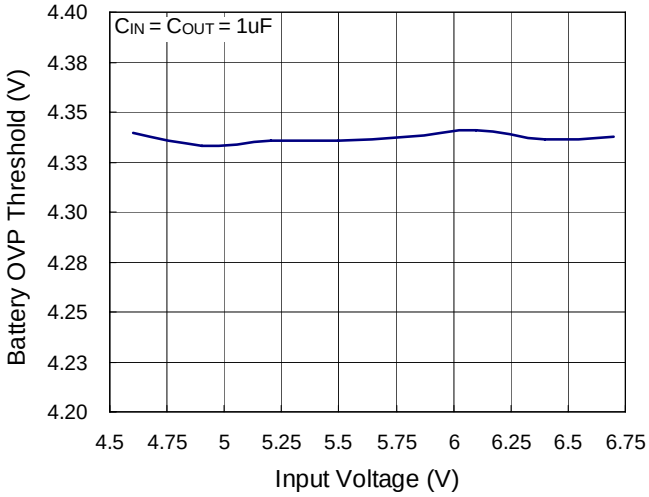
OCP Threshold vs. Inputt Voltage



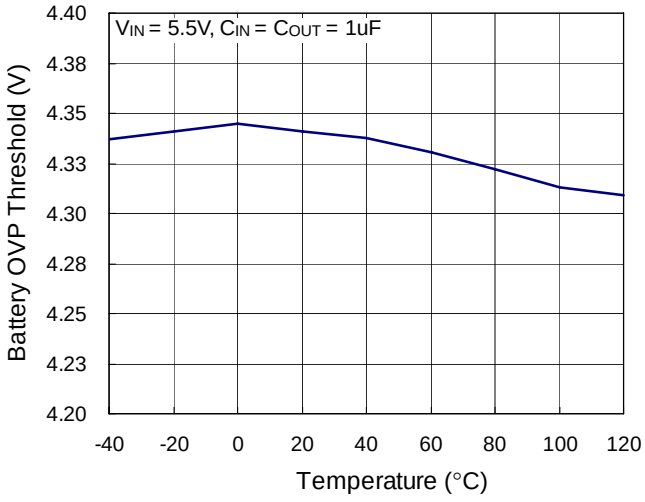
OCP Threshold vs. Temperature



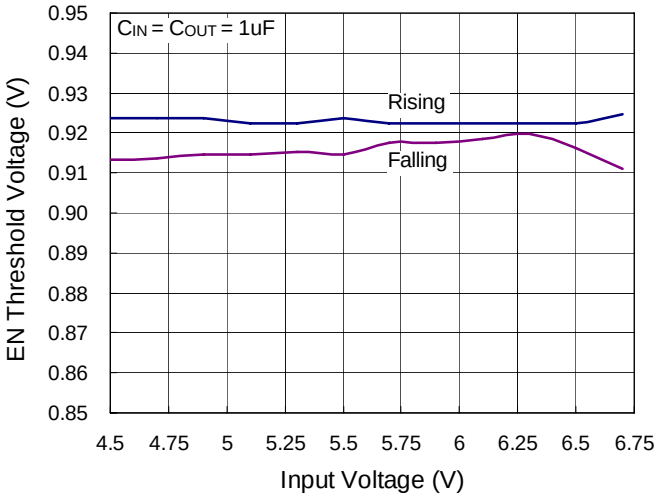
Battery OVP Threshold vs. Input Voltage



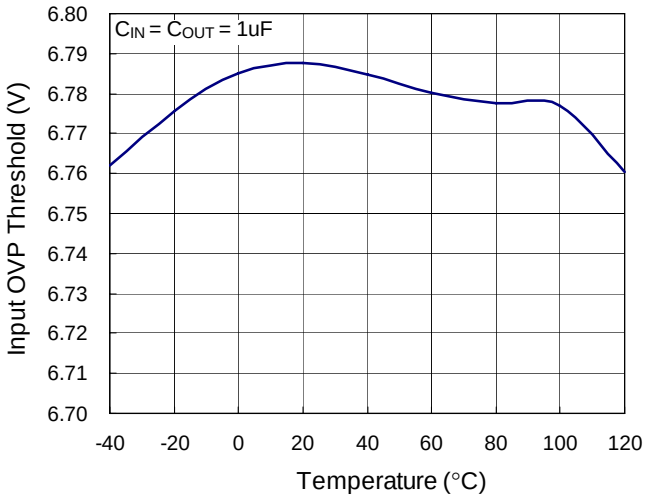
Battery OVP Threshold vs. Temperature



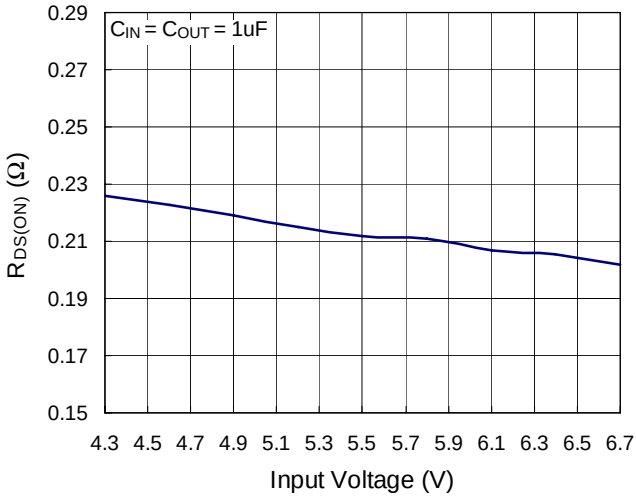
EN Threshold Voltage vs. Input Voltage



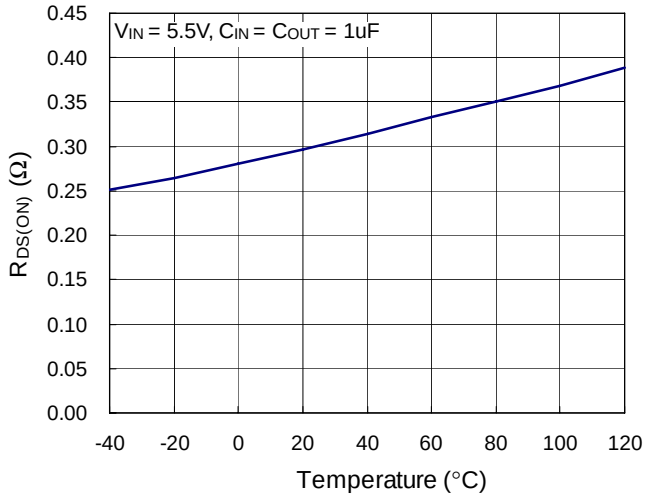
Input OVP Threshold vs. Temperature



$R_{DS(ON)}$ vs. Input Voltage



$R_{DS(ON)}$ vs. Temperature



Applications Information

Power Up

The RT9709 has an input under voltage lockout (UVLO) threshold of 2.6V with a built-in hysteresis of 100mV. Before the input voltage reaches the UVLO threshold, the RT9709 is off. When the input voltage is over the UVLO threshold; the RT9709 will delay for 10ms and after the 10ms delay, the soft-start will be activated. The 10ms delay allows any transients at the input during a hot insertion of the power supply to settle down before the IC starts to operate.

During the soft-start transition, the RT9709 slowly turns on the internal MOSFET to reduce the inrush current.

Enable Control

The RT9709 offers an enable ($\overline{EN}$) input. When the $\overline{EN}$ pin is pulled to logic high (>1.5V), the RT9709 will be shut down. When the $\overline{EN}$ pin is pulled to logic low (<0.4V), the RT9709 will be powered on.The $\overline{EN}$ pin has an internal pull-down resistor so that leaving the $\overline{EN}$ pin floating can enable the IC.

Warning Indication Output

The $\overline{WRN}$ pin is an open-drain output that indicates a LOW signal when any protection event occurs (Input OVP, Output OCP, OTP and Battery OVP). When the protection events are released and then the $\overline{WRN}$ pin indicates a HIGH signal. The 4-bit binary counters for the battery OVP and the OCP are reset to zero when the IC is re-enabled.

Over Temperature Protection (OTP)

The RT9709 monitors its own internal temperature to prevent thermal failures. The chip turns off the MOSFET when the internal temperature reaches 140°C with a built-in hysteresis of 50°C. The IC will resume to normal operation until the internal temperature falls to 90°C.

Input Over Voltage Protection

The RT9709 monitors the input voltage to prevent the input over voltage leading to output system failures. The input OVP threshold is set to 6.8V for the RT9709. When the input voltage exceeds the threshold, the RT9709 outputs a logic signal to turn off the internal MOSFET within 1us to prevent the device in the handheld system from damaging. The hysteresis of the input OVP threshold is 100mV. When the input voltage is reduced to the normal operation voltage range, the RT9709 will re-enable the MOSFET.

Battery Over Voltage Protection

The RT9709 monitors the battery voltage by the VB pin. When the battery voltage exceeds the 4.35V battery OVP threshold, the RT9709 has a built-in 180us blanking time to prevent any transient voltage from triggering the battery OVP. If the OVP situation still exists after 180us, the internal MOSFET will be turned off and the $\overline{WRN}$ pin indicates a LOW signal. The battery OVP threshold has a 30mV built-in hysteresis. The control logic contains a 4-bit binary counter. If the battery over voltage event occurs for consecutive 16 times, the MOSFET will be turned off permanently. The OVP latch status can be reset by the $\overline{EN}$ pin.

Selecting R_{VB}

The RT9709 monitors the battery voltage by the VB pin. The RT9709 will be turned off when the battery voltage exceeds the 4.4V battery OVP threshold. The VB pin is connected to the battery pack positive terminal via an isolation resistor (R_{VB}) and the resistor is an important component. The R_{VB} determines some parameters such as battery OVP threshold error and VB pin leakage current. Generally, it is necessary to decrease the R_{VB} for reducing the battery OVP threshold error. However, this will increase the VB pin leakage current. So, it is an important issue to get a trade-off between the battery OVP threshold error and the VB pin leakage current, the allowable resistance of the R_{VB} is 200kΩ to 1MΩ.

Over Current Protection (OCP)

The RT9709 monitors the output current to prevent the output short or the charging of the battery with an excessive current. The OCP (Over Current Protection) threshold can be set by the ILIM pin. The RT9709 has a built-in 170us delay time to prevent any transient noise triggering from the OCP. If the OCP situation still exists for 170us, the internal MOSFET will be turned off and the $\overline{WRN}$ pin indicates a LOW signal. When the OCP happens for consecutive 16 times, the internal MOSFET will be turned off permanently unless the input power is recycled or the enable pin is toggled.

OCP (Over Current Protection) Setting

The OCP (Over Current protection) threshold can be set by the ILIM pin. The resistor is connected between the ILIM pin and GND to set the OCP threshold. The OCP threshold can be calculated using the following equation :

$$I_{OCP} = \frac{K}{R_{ILIM}} = \frac{25000}{R_{ILIM}}$$

Selecting Capacitors

To get the better performance of the RT9709, it is very important to select peripherally appropriate capacitors. These capacitors determine some parameters such as input inrush current and input over shoot voltage. Generally, it is necessary to increase the input capacitance C_{IN} for reducing the input over shoot voltage. However, this will increase the inrush current of input. There are two scenarios that can cause the input over shoot voltage. The first one is that when the AC adapter is hot-plugged and the second one is when the RT9709 has a step-down change. The cable between the AC adapter output and the handheld system input has a parasitic inductor and resistor causing the input over shoot voltage.Generally, the input over shoot voltage range is 1.5 to 2 times the input voltage. It is recommended to use 1uF C_{IN} and C_{OUT} capacitance and the C_{IN} rated voltage should be at 1.5 to 2 time of the input voltage.

Thermal Considerations

For continuous operation, do not exceed absolute maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of RT9709, where $T_{J(MAX)}$ is the maximum junction temperature of the die (125°C) and T_A is the maximum ambient temperature. The junction to ambient thermal resistance θ_{JA} is layout dependent. The thermal resistance θ_{JA} for the WDFN-12L 4x3 packages is 60°C/W and the WDFN-10L 3x3 packages is 70°C/W on the standard JEDEC 51-7 four layers thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)}$ =(125°C – 25°C) / (60°C/W) = 1.429W for WDFN 3x3 packages

$P_{D(MAX)}$ =(125°C – 25°C) / (60°C/W) = 1.667W for WDFN 4x3 packages

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. For the RT9709 packages, the Figure 1 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

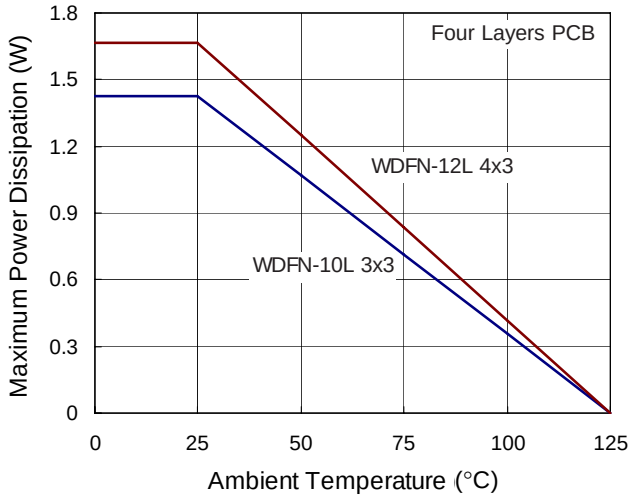


Figure 1. Derating Curves for RT9709/A Package

Layout Consideration

The RT9709 is a protection device. So, a careful PCB layout is necessary. For best performance, place all peripheral components as close to the IC as possible.

- Place C_{IN}, C_{OUT}, R_{VB}, and R_{ILIM} near to VIN, VOUT, VB, ILIM and GND pin respectively. A short connection is highly recommended. The following guidelines should be strictly followed when designing a PCB layout for the RT9709.
- The exposed pad, GND, must be soldered to a large ground plane for heat sinking and noise prevention. The through-hole vias located at the exposed pad is connected to ground plane of internal layer.

- VIN traces should be wide enough to minimize inductance and handle the high currents. The trace running from input to chip should be placed carefully and shielded strictly.
- Input and output capacitors must be placed close to the part. The connection between pins and capacitor pads should be copper traces without any through-hole via connection.

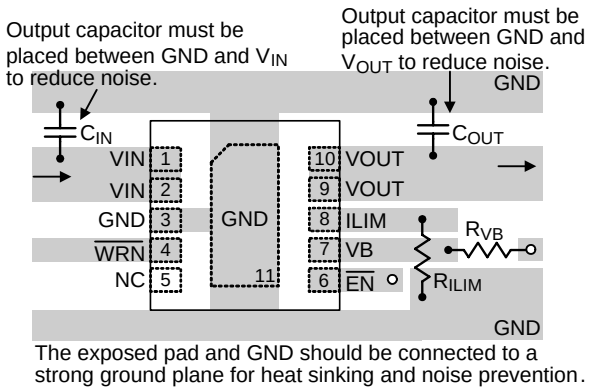
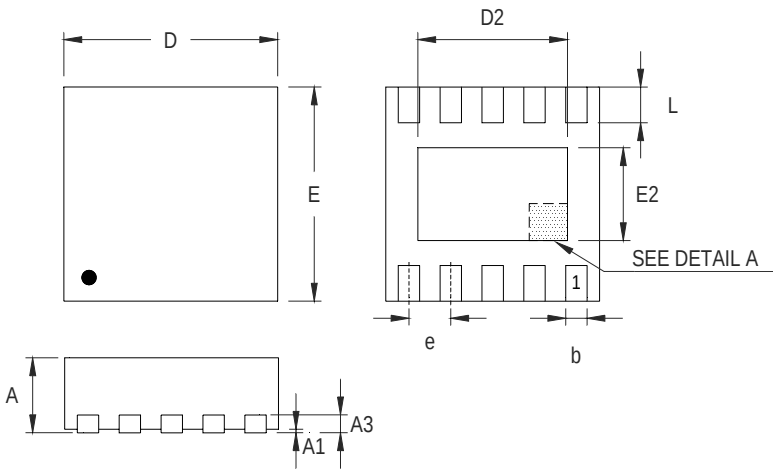
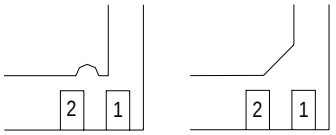


Figure 2. Recommended PCB Layout

Outline Dimension





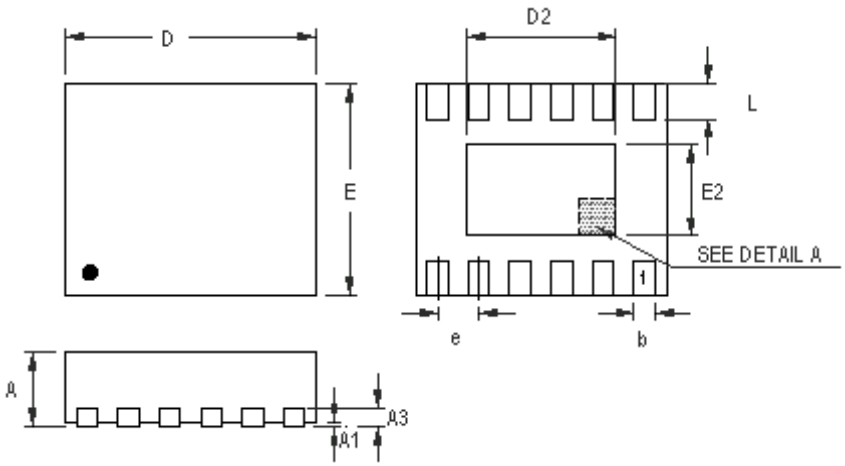
DETAIL A

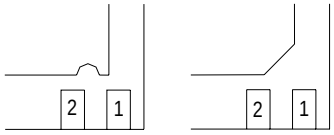
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 10L DFN 3x3 Package





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	3.950	4.050	0.156	0.159
D2	3.250	3.350	0.128	0.132
E	2.950	3.050	0.116	0.120
E2	1.650	1.750	0.065	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 12L DFN 4x3 Package

Richtek Technology Corporation

Headquarter

5F, No. 20, Taiyuen Street, Chupei City

Hsinchu, Taiwan, R.O.C.

Tel: (8863)5526789 Fax: (8863)5526611

Richtek Technology Corporation

Taipei Office (Marketing)

5F, No. 95, Minchiuan Road, Hsintien City

Taipei County, Taiwan, R.O.C.

Tel: (8862)86672399 Fax: (8862)86672377

Email: marketing@richtek.com