

NLX3G16

Triple Non-Inverting Buffer

The NLX3G16 MiniGate™ is an advanced high-speed CMOS triple non-inverting buffer in ultra-small footprint.

The NLX3G16 input and output structures provide protection when voltages up to 7.0 V are applied, regardless of the supply voltage.

Features

- High Speed: $t_{PD} = 1.8 \text{ ns}$ (Typ) @ $V_{CC} = 5.0 \text{ V}$
- Designed for 1.65 V to 5.5 V V_{CC} Operation
- Low Power Dissipation: $I_{CC} = 1 \mu\text{A}$ (Max) at $T_A = 25^\circ\text{C}$
- 24 mA Balanced Output Source and Sink Capability
- Balanced Propagation Delays
- Overvoltage Tolerant (OVT) Input and Output Pins
- Ultra-Small Packages
- These are Pb-Free Devices

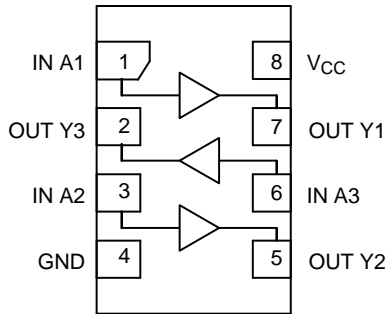


Figure 1. Pinout (Top View)

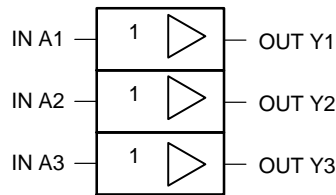


Figure 2. Logic Symbol

PIN ASSIGNMENT

1	IN A1
2	OUT Y3
3	IN A2
4	GND
5	OUT Y2
6	IN A3
7	OUT Y1
8	V_{CC}

FUNCTION TABLE

A	Y
L	L
H	H



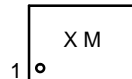
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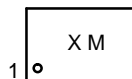
MARKING DIAGRAMS



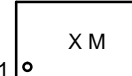
UDFN8
1.45 x 1.0
CASE 517BZ



UDFN8
1.6 x 1.0
CASE 517BY



UDFN8
1.95 x 1.0
CASE 517CA



J or AD = Specific Device Code
M = Date Code
▪ = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

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MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	-0.5 to +7.0	V
V_{IN}	DC Input Voltage	-0.5 to +7.0	V
V_{OUT}	DC Output Voltage	-0.5 to +7.0	V
I_{IK}	DC Input Diode Current $V_{IN} < GND$	-50	mA
I_{OK}	DC Output Diode Current $V_{OUT} < GND$	-50	mA
I_O	DC Output Source/Sink Current	±50	mA
I_{CC}	DC Supply Current Per Supply Pin	±100	mA
I_{GND}	DC Ground Current per Ground Pin	±100	mA
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T_J	Junction Temperature Under Bias	150	°C
MSL	Moisture Sensitivity	Level 1	
F_R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
$I_{LATCHUP}$	Latchup Performance Above V_{CC} and Below GND at 125 °C (Note 5)	±500	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace no air flow.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/UESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA / JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Positive DC Supply Voltage	1.65	5.5	V
V_{IN}	Digital Input Voltage	0	5.5	V
V_{OUT}	Output Voltage	0	5.5	V
T_A	Operating Free-Air Temperature	-55	+125	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate $V_{CC} = 1.8 V \pm 0.18$ $V_{CC} = 2.5 V \pm 0.2 V$ $V_{CC} = 3.3 V \pm 0.3 V$ $V_{CC} = 5.0 V \pm 0.5 V$	0 0 0 0	20 20 10 5	ns/V

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DC ELECTRICAL CHARACTERISTICS

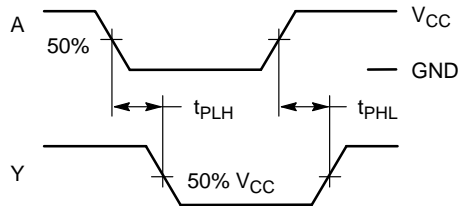
Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25 °C			T _A = +85°C		T _A = -55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	Low-Level Input Voltage		1.65 to 5.5	0.70 x V _{CC}			0.70 x V _{CC}				V
V _{IL}	Low-Level Input Voltage		1.65 to 5.5			0.30 x V _{CC}		0.30 x V _{CC}		0.30 x V _{CC}	V
V _{OH}	High-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OH} = -100 μA	1.65 to .5	V _{CC} - 0.1	V _{CC}		V _{CC} - 0.1		V _{CC} - 0.1		V
		V _{IN} = V _{IH} or V _{IL} I _{OH} = -4 mA	1.65	1.4	1.50		1.4		1.4		
		I _{OH} = -8 mA	2.3	1.9	2.1		1.9		1.9		
		I _{OH} = -12 mA	2.7	2.2	2.4		2.2		2.2		
		I _{OH} = -16 mA	3.0	2.4	2.7		2.4		2.4		
		I _{OH} = -24 mA	3.0	2.3	2.5		2.3		2.3		
I _{OH} = -32 mA	4.5	3.8	4.0		3.8		3.8				
V _{OL}	Low-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OL} = 100 μA	1.65 - 5.5			0.1		0.1		0.1	V
		V _{IN} = V _{IH} or V _{IL} I _{OH} = 4 mA	1.65		0.2	0.24		0.24		0.24	
		I _{OH} = 8 mA	2.3		0.2	0.3		0.3		0.3	
		I _{OH} = 12 mA	2.7		0.22	0.4		0.4		0.4	
		I _{OH} = 16 mA	3.0		0.28	0.4		0.4		0.4	
		I _{OH} = 24 mA	3.0		0.38	0.55		0.55		0.55	
I _{OH} = 32 mA	4.5		0.42	0.55		0.55		0.55			
I _{IN}	Input Leakage Current	0 ≤ V _{IN} ≤ 5.5 V	0 to 5.5			±0.1		±1.0		±1.0	μA
I _{OFF}	Power-Off Output Leakage Current	V _{IN} or V _{OUT} = 5.5 V	0			1.0		10		10	μA
I _{CC}	Quiescent Supply Current	0 ≤ V _{IN} ≤ V _{CC}	5.5			1.0		10		10	μA

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AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ nS)

Symbol	Parameter	V _{CC} (V)	Test Condition	T _A = 25 °C			T _A = +85°C		T _A = -55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t _{PLH} , t _{PHL}	Propagation Delay Input A to Output	1.65–1.95	R _L = 1 MΩ, C _L = 15 pF	1.8	6.0	7.9	1.8	8.8	1.8	12	ns
		2.3–2.7	R _L = 1 MΩ, C _L = 15 pF	1.0	3.0	5.2	1.0	5.8	1.0	9.1	
		3.0–3.6	R _L = 1 MΩ, C _L = 15 pF	0.8	2.3	3.6	0.8	4.0	0.8	6.5	
			R _L = 500 Ω, C _L = 50 pF	1.2	3.0	4.6	1.2	5.1	1.2	7.6	
		4.5–5.5	R _L = 1 MΩ, C _L = 15 pF	0.5	1.8	2.9	0.5	3.2	0.5	5.5	
			R _L = 500 Ω, C _L = 50 pF	0.8	2.4	3.8	0.8	4.2	0.8	6.4	
C _{IN}	Input Capacitance	5.5	V _{IN} = 0 V or V _{CC}		7.0					pF	
C _{PD}	Power Dissipation Capacitance (Note 6)	3.3	10 MHz V _{IN} = 0 V or V _{CC}		9					pF	
		5.5			11						

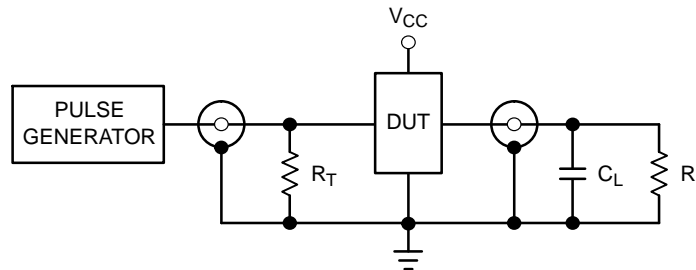
6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}$. C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.



PROPAGATION DELAYS

$$t_R = t_F = 2.5 \text{ ns, } 10\% \text{ to } 90\%; f = 1 \text{ MHz; } t_W = 500 \text{ ns}$$

Figure 3. Switching Waveforms



$$R_T = Z_{OUT} \text{ of pulse generator (typically } 50 \Omega \text{)}$$

Figure 4. Test Circuit

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ORDERING INFORMATION

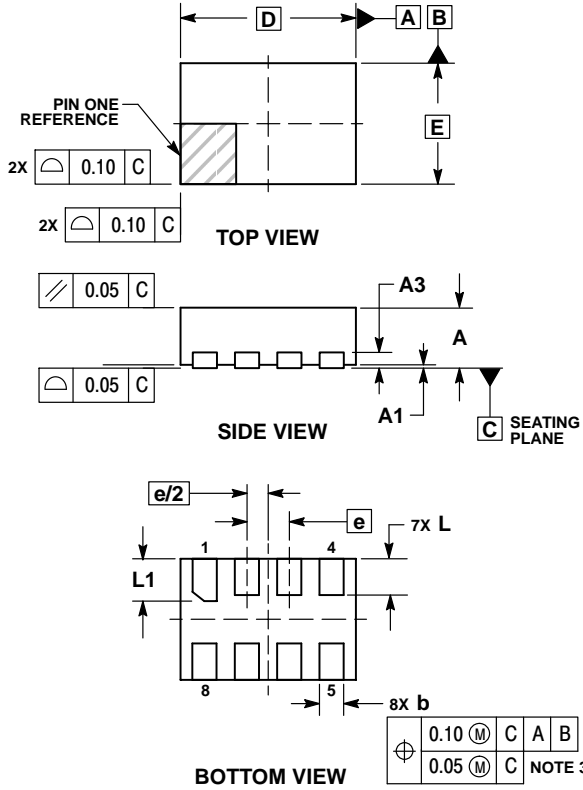
Device	Package	Shipping†
NLX3G16DMUTCG	UDFN8, 1.95 x 1.0, 0.5P (Pb-Free)	3000 / Tape & Reel
NLX3G16EMUTCG	UDFN8, 1.6 x 1.0, 0.4P (Pb-Free)	3000 / Tape & Reel
NLX3G16FMUTCG	UDFN8, 1.45 x 1.0, 0.35P (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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PACKAGE DIMENSIONS

UDFN8 1.45x1.0, 0.35P
CASE 517BZ
ISSUE O

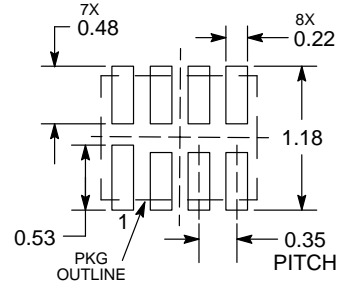


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
D	1.45 BSC	
E	1.00 BSC	
e	0.35 BSC	
L	0.25	0.35
L1	0.30	0.40

RECOMMENDED SOLDERING FOOTPRINT*

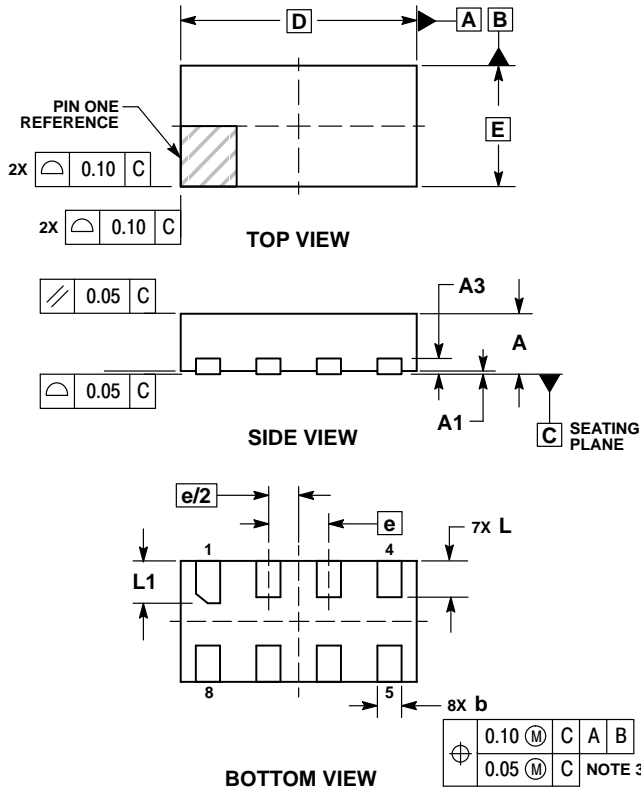


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PACKAGE DIMENSIONS

UDFN8 1.95x1.0, 0.5P
CASE 517CA
ISSUE O

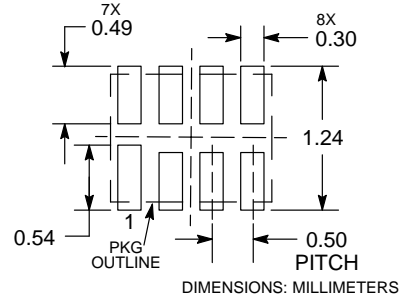


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4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13	REF
b	0.15	0.25
D	1.95	BSC
E	1.00	BSC
e	0.50	BSC
L	0.25	0.35
L1	0.30	0.40

RECOMMENDED SOLDERING FOOTPRINT*



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